

An Ultra-Low Power Physical Layer Design for Biomedical Application

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ABSTRACT

The wireless body area network (WBAN) is a wireless network used for communication among sensor nodes operating on, in or around the human body in order to monitor vital body parameters and movements. The pursuit of higher quality of life motivates people to be more concerned about their health and potential diseases. At the same time, many patients can benefit from continuous monitoring of their diagnostic procedures. All these require a convenient healthcare surveillance system to monitor people's health status anytime anywhere, especially when people suffer an acute event, such as a sudden heart attack. The tracking capability of such a system should also be able to provide optimal maintenance after a surgical procedure and support early detection of abnormal health conditions. This project investigates the efficient design of the PHY layer architecture for wireless body area networks (WBAN), which targets on ultra-low power consumption with reliable quality of service (QoS). A low cost baseband transceiver specification and a data processing flow are proposed with a comparatively low-complexity control state machine. A multifunctional digital timing synchronization scheme is also proposed, which can achieve packet synchronization and data recovery.

Index Terms—Digital circuit design, low power, wireless body area network (WBAN), wireless communication.

1. INTRODUCTION

With recent advances in wireless sensor networks and embedded computing technologies, miniaturized pervasive health monitoring devices have become practically feasible. In addition to providing continuous monitoring and analysis of physiological parameters, the recently proposed Body Sensor Networks (BSN) incorporates context aware sensing for increased sensitivity and specificity. To facilitate research and development in BSN and multi-sensor data fusion, a BSN hardware development platform is presented. With its low power, flexible and compact design, the BSN nodes provide a versatile environment for wireless sensing research and development.

The last decade has witnessed rapid growth of high power, low cost mobile sensing platforms, finding successful application in a range of environments - from industrial process monitoring to structure management. To date, the most challenging area is that of the human body and extensive research is focused on biocompatibility, signal propagation and power management to permit pervasive sensing of detailed physiological signals from implantable, wearable and ambient sensors. By involving users in the management of their own wellbeing they aid in the delivery of preventative care, facilitating capture of the onset and systematic deterioration of "lifestyle" diseases. When used for sports

performance monitoring, BSNs can also record long-term progress whilst providing real-time training information that can be used to maximize the effectiveness of training sessions.

Rapid advance in science and technology are paving the way for improvement of human life. It, in turn, will change the way in which we think about medicine, sports and entertainment and how we experience them. Advances in sensors, integrated circuits, and wireless communication are paving the way for developing miniature, lightweight, ultra-low power physiological healthcare surveillance and monitoring devices for the improvement of human lives. These devices can be integrated into wireless body area networks (WBANs) for health monitoring [1]. Wireless Body Area Networks (WBANs) are networks whose nodes are usually placed close to the body on or in clothing every day. A WBAN topology comprises a series of miniature sensor/actuator nodes, each of which is able to communicate with other sensor nodes or with a central node worn on the body [2]. The central node communicates with the outside world by using a standard telecommunication infrastructure, such as wireless local area and cellular phone networks, and is with the higher computation capability.

The WBAN can deliver the services, including management of chronic disease, medical diagnostics, home-monitoring, biometrics, and sports and fitness tracking, [3],[4] etc. The power budget is quite strict for WBAN applications since the wireless device is battery supplied. To sustain longer battery life, ultra-low power transceiver should be developed with the relaxed range coverage 1-3m. Recently, transceivers for wireless personal area networks (WPANs) have been developed [5]–[7]. For example, the CC2420 from Texas Instruments in [5] can cover a 20–30 m range at a power consumption of 60~70mW. However, such operation range and power consumption are not the optimal choice for WBAN applications, where the transceiver design target is a 1~3 m operation range to achieve ultra-low power. WBAN transceivers are proposed in [8]. Most of these transceivers have high data rate transmission, resulting in comparatively high power consumption. This article describes the modeling of ultra wideband wireless propagation channels, especially for the simulation of personal area networks. The IEEE 802.15.3a standards task group has established a standard channel model to be used for the evaluation of PAN physical layer proposals. We discuss the standard model, the measurements that form its basis, and the possibilities for future improvements. The article points out the important differences between UWB channels and narrowband wireless channels, especially with respect to fading statistics and time of arrival of multipath components. The impacts of the different propagation conditions on system design, like Rake receiver performance, are elaborated.

In, wireless technology and the system integration in body area network for m-health applications the challenging issues are need for extremely low power operation, low weight, and small size, non-invasive and unobtrusive operation, sensor flexibility necessary to adapt to the user's state and changes in the environment, seamless connectivity necessary for sensor integration into the monitoring system, system awareness of environmental and patient factors associated with the use of wearable sensors in normal living conditions, secure and reliable communication and data storage, fault tolerant system operation, capable of adapting to faults of individual sensors and retransmission of lost. The Zigbee modulator/demodulators which are used in transceivers for wireless personal area networks[6] have a power consumption of about 251 μ w. A low power 2.45GHz Zigbee transceiver for wearable personal area devices in WPAN which is mentioned in [7] shows a power consumption of 271 μ w.

Even though in [8],[9] proposed an OFDMA base wireless body area network proposed a reduced power WBAN, they have high data rate transmission of about 480 kbps resulting in increase in the power consumption. The dual mode transceiver which was proposed in [10] also have high data rate transmission. However, such operation range and power consumption are not the optimal choice for WBAN applications, where the transceiver design target is a 1~ 3 m operation range to achieve ultra-low power. So here an optimized low power low data rate digital baseband IC is proposed.

2. PROPOSED BASEBAND TRANSCEIVER

The complete system diagram of a WBAN radio transceiver is shown in Fig. 1. In the transmitter block, the physical layer service data unit (PSDU) from the MAC layer is processed in the proposed transmitter (TX) baseband processor module to generate a physical layer protocol data unit (PPDU) packet. The channel coding and signal processing are performed on the PPDU in the TX baseband processor module, and the raw data rate of the TX baseband processor module output is 250 kb/s. The baseband raw data is modulated by FSK and then directly up-converted to a 2.45 GHz RF signal. In the receiver (RX) block, the received RF signal is down-converted to a 2 MHz intermediate frequency (IF) signal and then demodulated by a low power FSK demodulator. The demodulated signal is processed by the RX baseband processor module. Following that, the received PSDU is fed into the MAC layer.

To achieve ultra-low power consumption, a low-complexity PHY specification is proposed. The signal processing flow for TX and RX are presented in Figs. 2 and 3, respectively. In the TX module, the baseband processor receives the PSDU from the MAC layer constructs the PPDU, whose structure is illustrated in Fig. 4. The permitted length of the PSDU within one packet should be no larger than 127 octets, and this information is contained in the PHY header (PHR) in octets. Once one packet of the PSDU is generated by the MAC layer, it is fed into TXFIFO and ready for transmission. There is a Prefix MUX block controlled by the TX state control block to

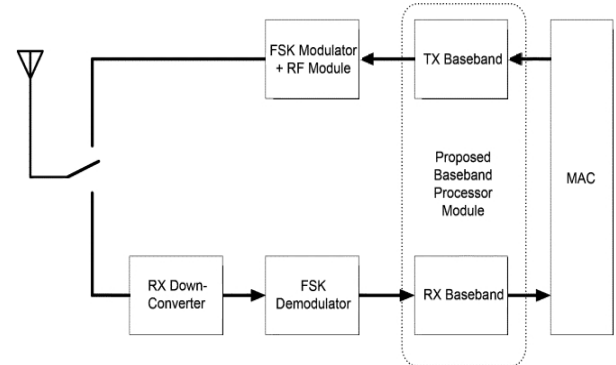


Fig:1 Block diagram of a complete WBAN radio transceiver

select the input of the low density parity check (LDPC) encoder block. When a transmission command is sent from the MAC layer, the PHR is prefixed to the PSDU and sent into encoder block first. The input data of the LDPC encoder block is in serial sequence with 1 bit word-length. In our design, (15, 7) LDPC coding [11] is used as forward error correction (FEC).

LDPC codes have a limited number of 1's in each row and column of the matrix; this limit guarantees limited complexity in their associated detectors and correctors making them fast and light weight. For each consecutive 7 bits of input data, the LDPC encoder block generates 15 bits of output data simultaneously, and thus the word-length of the LDPC block output is 15 bits. The output data of LDPC encoder block is fed into the interleaving block to suppress the burst error. To eliminate long strings of like bits that might impair receiver synchronization and to eliminate most periodic bit patterns that could produce undesirable frequency components (including the dc component), the interleaved data payload is first fed into a scrambling block and then coded by a Manchester encoder. The scrambling block generates the scrambling code in serial sequence with 1 bit word-length. The output data of the interleaving block is in serial sequence with 1 bit word-length and is XORed with the generated scrambling code. The scrambled data payload is fed into the Manchester encoder. The Manchester encoder converts the bit "0" to bits "01" and converts the bit "1" to bits "10," and thus the total number of "0" and "1" can be balanced. The output of the Manchester encoder is prefixed with the synchronization header (SHR) and is sent to the FSK modulator for transmission.

In the receiver module, the received data stream is the demodulated binary signals from the FSK demodulator. We use the D flip-flop provided by the technology library to sample and to restore the analog input. If the voltage of the input signal is higher than of the D flip-flop, the output of the D flip-flop will be "1." If the voltage of the input signal is lower than of the D flip-flop, the output of the D flip-flop will be "0." As illustrated in Fig. 3, the signals are first serially fed into the synchronization and data recovery (SDR) block to achieve synchronization and to recover the received data. The SDR block over-samples the incoming signal using a shift register matrix block and calculates the correlation between the incoming data and preamble sequence to achieve bit synchronization. The peak of the calculated correlation is continuously detected. Once the peak value is found, the start-of-frame delimiter (SFD) Correlator block calculates the correlations between the incoming data and the predefined

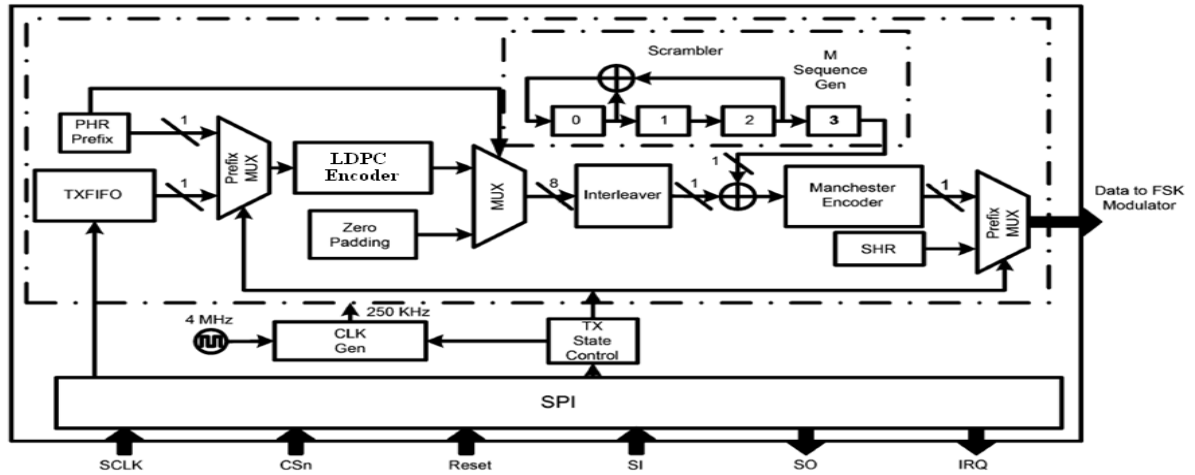


Fig:2 Block diagram of baseband TX.

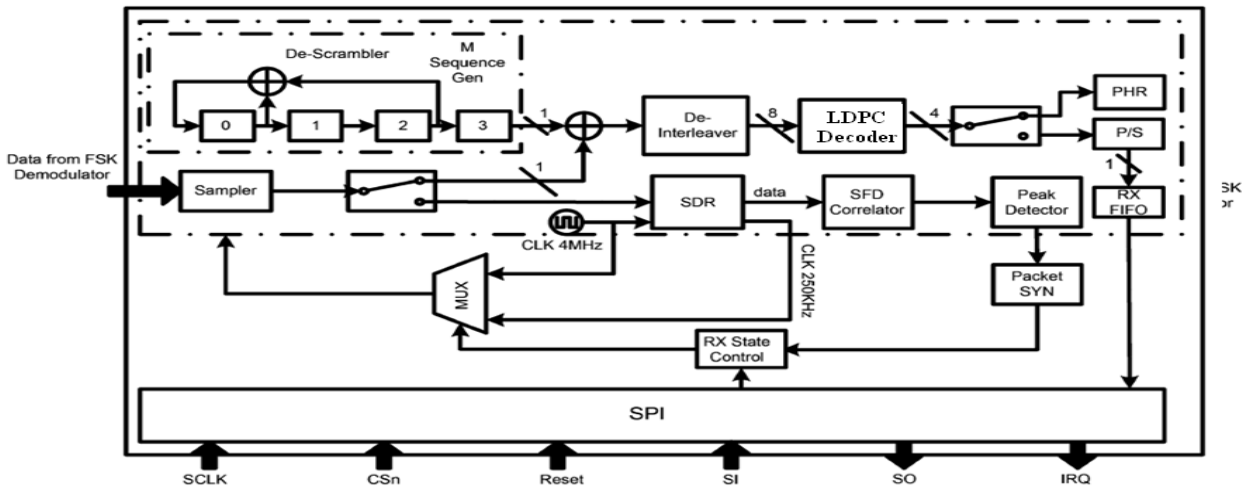


Fig:3 Block diagram of baseband RX.

SFD sequence, and the peak value is searched by the following peak detector block.

Once the peak value is found, the packet synchronization is confirmed. The preamble sequence and SFD are removed and the Packet SYN block indicates to the RX State Control block that the PHR and PSDU can be received. The SDR block also generates the 250 kHz clock, and the RX State Control block selects the operation clock frequency of the RX baseband processor module which can be between 4 MHz clock and 250 kHz clock. Manchester decoding is first performed on the received PHR and PSDU data stream by detecting the first bit or every two continuous received bits. If the LDPC decoder block detects an error but cannot correct it, the receiver will stop receiving any data and the MAC layer will request a retransmission of this packet. The PHR is decoded first and thus length information about the PSDU can be obtained by the RX state control block. The word-length of the LDPC decoder block output is 7 bits, and there is a parallel to serial buffer, so that bits in the PSDU are fed into the RXFIFO in

serial sequence with 1 bit word-length, and is read by the MAC-layer.

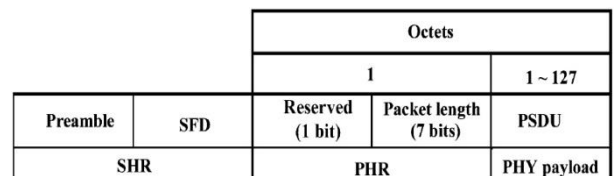


Fig:4 PPDU packet form

3. MODULE DESIGN

In this section, block architectures for the major signal processing modules are introduced in detail. The channel coding module will be introduced first, followed by the synchronization and data recovery module.

3.1 Channel Coding Module for Robustness

In a wireless transceiver system design, the performance of PER is one of the key concerns as it drives the specification of the system parameters, such as packet length, transmission power, working range, receiver sensitivity, and etc. To improve the PER performance, it is necessary to utilize a channel coding scheme that improves noise suppression and reduces Inter Symbol Interference (ISI).

Therefore, the channel model for potential applications can be considered as frequency-nonselective fading, and thus the Inter-Symbol Interference (ISI) may not be very critical. Based on these considerations and to achieve an acceptable balance between performance and complexity throughput, we avoid the spreading technique. Instead, we adopt FEC coding and interleaving to improve the capability of suppressing noise and ISI and keep the complexity low.

The block diagram of the LDPC encoder is illustrated in Fig. 6. $C_0 \sim C_6$ where are the original information bits and $C_7 \sim C_{14}$ are the parity bits. The 15 bits output from the deinterleaving block are fed into the LDPC decoder. Decoder converts 15 bit information to 7 bits. Finally, the correct 7-bit information codewords are selected and fed into the RXFIFO. The interleaving block is implemented to provide additional error correction capability in burst error circumstances.

The 15×7 matrix interleaving is employed, which means that as long as the burst error does not last longer than 7 bits, the burst error can be corrected after decoding at the receiver.

3.1.1 Low density parity check codes

In information theory, a low-density parity-check (LDPC) code is a linear error correcting code, a method of transmitting a message over a noisy transmission channel, and is constructed using a sparse bipartite graph. LDPC codes are capacity-approaching codes, which means that practical constructions exist that allow the noise threshold to be set

very close (or even arbitrarily close on the BEC) to the theoretical maximum (the Shannon limit) for a symmetric memory-less channel. The noise threshold defines an upper bound for the channel noise, up to which the probability of lost information can be made as small as desired. Using iterative belief propagation techniques, LDPC codes can be decoded in time linear to their block length.

LDPC codes are finding increasing use in applications requiring reliable and highly efficient information transfer over bandwidth or return channel-constrained links in the presence of data-corrupting noise. Although implementation of LDPC codes has lagged behind that of other codes, notably turbo codes, the absence of encumbering software patents has made LDPC attractive to some. Low density parity-check codes specified by a matrix containing mostly 0's are relatively few 1's. In particular, an (n, j, k) low density code is a code of block length n , where each column contains a small fixed number j of 1's and each row contains a small fixed number k of 1's as shown in Fig. 5. Low density codes are not optimum in the somewhat artificial sense of minimizing the probability of decoding error for a given block length, and it can be shown that maximum rate at which they can be used is bounded below channel capacity. However, the existence of a simple decoding scheme more than compensates for these disadvantages.

1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	1	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0
0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1

Fig: 5 Example of a low density code matrix for $n=20, j=3$ and $k=4$

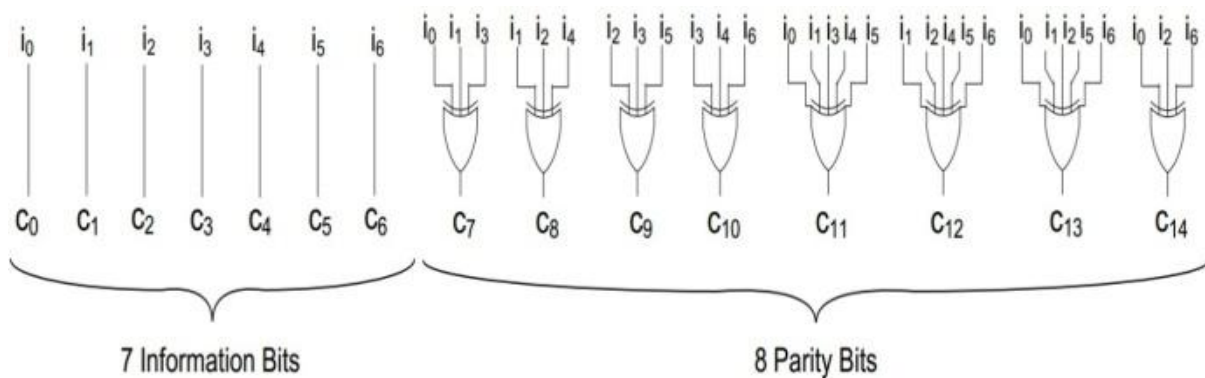


Fig: 6 Block diagram of LDPC encoder

3.2 Synchronization and Data Recovery Module

In the TX module, the output from the Manchester encoder is prefixed with the SHR, which contains the preamble sequence and SFD, as shown in Fig. 2. They are formed by pseudo-noise (PN) sequences and utilized so that the receiver can achieve synchronization and reduce the false alarm rate (FAR) of synchronization when receiving data. The preamble sequence is formed from a 32-bit PN sequence [11011001110000110101001000101110] and repeats four times. Whereas SFD is given by a 64-bit PN sequence [001011101101100111000011010100101100001101010010010111011011001]. This pre-amble and SFD format leads to reliable synchronization performance.

In the RX module, the packet synchronization scheme detects peaks of correlation between the received data sequence and the local SHR sequence. For a preamble sequence without considering noise and other interference, there should be four equal peaks among all the correlation values. We set a preamble threshold thh_pre and specify that if two continuous peaks of preamble correlation that are higher than thh_pre have been detected and the interval between these two peaks is 32 bits, then the acquisition of the preamble can be confirmed. The reason that we only detect two continuous peaks instead of four peaks is to achieve a tradeoff between reliable performance and low power consumption. Following that, we start to calculate the correlation between the received data sequence and the local SFD. An SFD threshold thh_sfd is set, and it is specified that if there is a peak that is higher than thh_sfd , the acquisition of SFD can be confirmed, and thus packet synchronization is achieved. The thh_pre and thh_sfd thresholds should be selected carefully to reduce the FAR of synchronization.

Another function of the SDR module is bit synchronization. This SDR module provides the stable 250 kHz clock source and recovered data sequences for further baseband signal processing. At each negative edge of the 250 kHz clock cycle, the SDR module samples the analog input such that the following signal processing block is able to obtain a stable sampled data input at each positive edge of the 250 kHz clock cycle. Fig. 7(a) shows the ideal output from the analog FSK demodulator. It can be observed that for the ideal input data, the sampled sequences from any specified sampling position can be used as the recovered data sequence. However, for a practical output signal, as shown in Fig. 7(b), as the result of the interference and the non-ideality of the receiver front-end, the transition between them is comparatively slow and the time duration of each received bit may vary within μs .

In other words, the guaranteed constant period within one bit is only $2.5\mu s$. Consequently, the corresponding sampled sequences from different specified sampling positions may not be identical and cannot be directly used for further baseband processing. Therefore, it is necessary to develop a reliable scheme to determine the appropriate sampling position for accurate data recovery.

In some applications, Manchester coding can be used for self synchronization by detecting the transition at the middle or start a bit period. However, due to the non-ideality of the analog input, there may be a glitch when the transition occurs, and thus the performance of self-synchronization by using Manchester coding may be greatly degraded. Fortunately, there is a 4 MHz clock source for the analog FSK

demodulator. We can take advantage of this clock source to oversample the analog data input. Since the raw data rate is 250 kb/s, a 4 MHz clock can achieve $4\text{ M}/250\text{ k}=16$ possible sampling positions within one bit period, as shown in Fig. 7 (sampling from point a to p)

3.2.1 Synchronization

For clear illustration, let us first consider a simplified circumstance. It is assumed that the preamble sequence pattern is [010110] and thh_pre is 5. The $16\times$ oversampling is adopted on the practical FSK demodulator output. Fig. 8 shows the corresponding sampled data sequence from different sampling points. The samples are contained in a 6×16 registers matrix, where the elements in each column correspond to the sample sequences from identical sampling points. We calculate the correlation between the local preamble sequence and each column of the register block. As mentioned before, the guaranteed constant period per bit is $2.5\mu s$. Accordingly, if there are at least nine correlation values corresponding to nine continuous columns (from points to for example) that are larger than the threshold, we confirm that the preamble is acquired. At the same time, we will choose the middle point these nine points as the sampling point (point in this case).

The block diagram of this proposed SDR module is shown in Fig. 9, where the synchronization block is in the upper part. The input data from the FSK demodulator is sampled at 4 MHz to obtain 16 samples per bit. In our design, the length of one preamble sequence is 32, and thus the sampled sequence serially shifts into a 32×16 registers block ($R_{1,1}\sim R_{32,16}$) all of which are driven by the 4 MHz clock. At each clock cycle, the data stored in the right-most column registers will be fed into the correlator module, which is illustrated in the right hand side of Fig. 9, and the corresponding result will be compared with the threshold thh_pre . If the correlation result is higher than thh_pre , an indication bit will be generated and sent to the control module. In the control module, a counter will calculate the number of continuously received indication bits. If the total number of indication bits is larger than 9, a preamble sequence is confirmed to be received, and the control module will enable the data recovery module.

3.2.2 Digital Data Recovery

The digital data recovery block diagram is illustrated in the lower part of Fig. 9. There is a counter driven by a 4 MHz clock source and enabled by the control module in the synchronization part after the central sampling point is confirmed. The output of this counter is 3 bits, and thus the counting range is. When the counter output becomes 7, the clock source output CLK_250 reverses its value. Every time at the negative edge of CLK_250, the analog input data will be sampled to generate the recovered data. This proposed SDR module requires considerable power consumption as the result of the over-sampling procedure, which involves the 4 MHz clock driving the 32×16 registers block. However, we use the clock gating in this block.

Once we find the accurate central sampling point, the clock of this oversampling block is disabled by the control module and the sampling rate will be reduced by a factor of 16 to 1 sample/bit. The clock gating of the register block will dramatically reduce the power consumption.

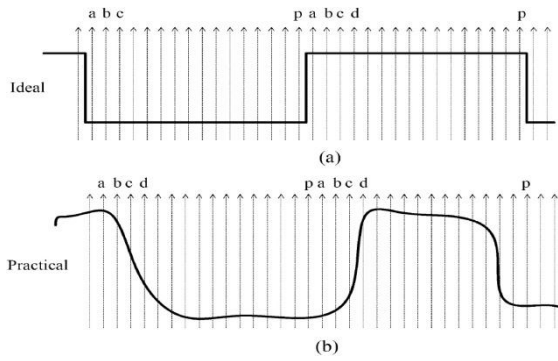


Fig:7(a) Ideal and (b) practical output from FSK demodulator.

When the first preamble peak is confirmed, the accurate sampling position will also be confirmed. During this period, all the following baseband processors are not active. Therefore, the duration of power supply for the registers block is quite short, and the overall receiver baseband processor still maintains comparatively low power consumption.

In practice, the TX and RX clock frequency may be slightly different. Assuming that the accuracy of the oscillators for the transceiver system is ± 100 ppm, the maximum frequency offset between the transmitter and the receiver is ± 200 ppm. Therefore, the sampling point drifts 1 clock cycle on every 5000 clock cycles for the worst case, and thus the receiver cannot decode the correct information bits. To solve this problem, we need to realign the sampling point of the receiver periodically. The realignment scheme is similar to that of the synchronization scheme using the registers matrix block shown in Fig.8. During the realignment period, we 16x oversample the received signal and feed the oversampled

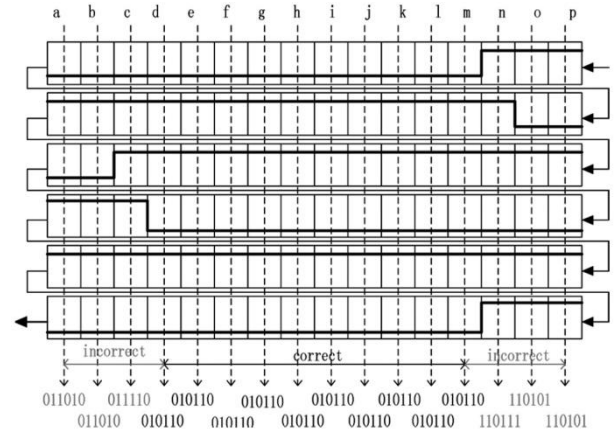


Fig: 8 Proposed shift registers matrix block.

data into the registers matrix block shown in Fig.8. If nine continuous columns of the "0110" or "01010" pattern is found (from points to for example), we realign the sampling point to the middle point of these nine points (point in this case). The reason for searching the patterns "0110" and "01010" is that the Manchester coding is used in the data payload. Therefore the 4-bit data pattern "0110" and 5-bit data pattern "01010" can be easily captured. At the same time, both of these two patterns have transitions from "0" to "1" and from "1" to "0" which makes the patterns easier to be recognized. In our design, the realignment scheme will be activated every 1000 received data bits, which guarantees that the maximum sampling point drift is less than 1/4 of a clock cycle. This realignment scheme can adaptively adjust the sampling point without any external control and can process long transmitted data without additional synchronization bits.

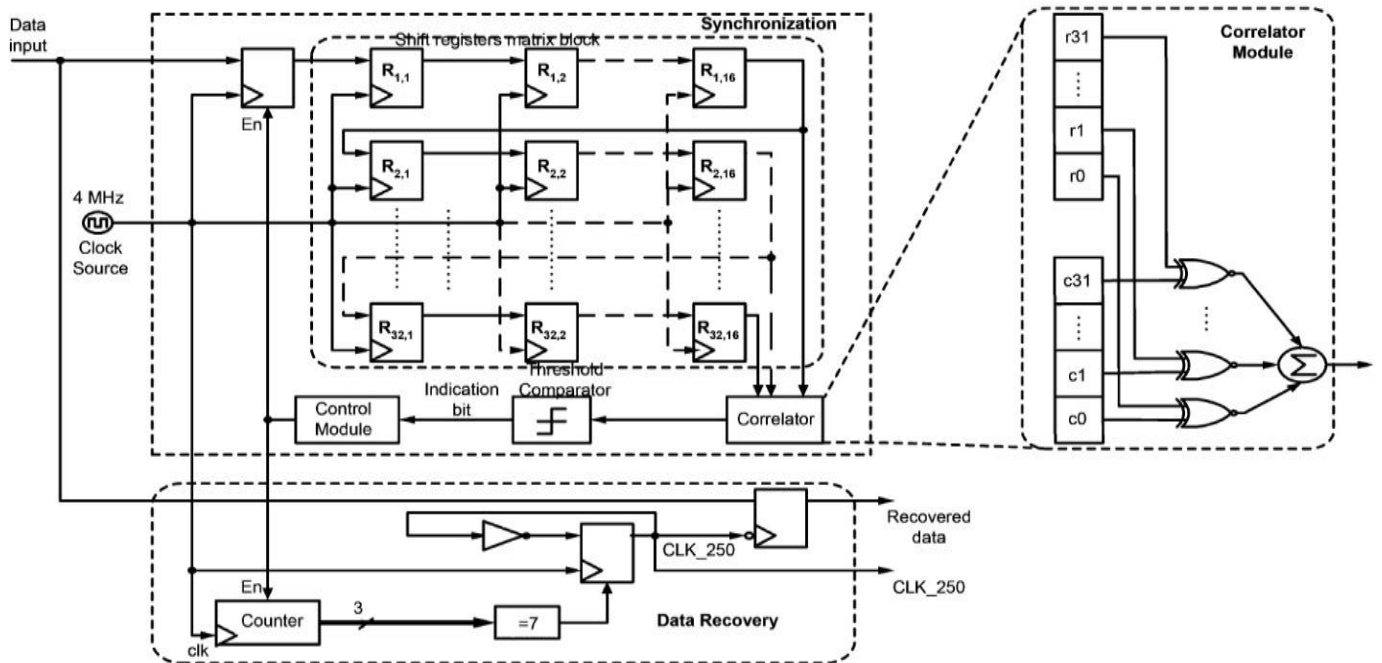


Fig:9 Block diagram of the proposed SDR module

Under this scheme, we can achieve timing alignment without tuning the receiver clock frequency using a PLL circuit, resulting in This proposed realignment scheme can adaptively adjust the low complexity. The proposed realignment scheme shares the same structure and circuits with the synchronization scheme, resulting in hardware efficiency. The clock of the oversampling and registers matrix block will be enabled only during this period, and will be disabled after the realignment period. In case that there are some distortions as the result of noise, the realignment procedure continuously searches until it finds the "0110" or "01010" patterns. Since these two patterns can be easily acquired, this proposed realignment procedure will not consume much additional power. Probably, these two patterns may also be found even in the distorted received signals.

3.2.3 SPI between MAC and PHY Baseband

The above baseband transceiver is interfaced with the MAC layer via a four-wire SPI module (pins SI, SO, SCLK, and CSn), as shown in Figs. 2 and 3, where the baseband processor is the slave. The baseband processor buffers the transmitted data from the microcontroller (MCU) and received data to the MCU in two 128 bytes first-in-first-out (FIFOs) (TXFIFO and RXFIFO, respectively). The SPI module enables the serial (one bit at a time) exchange of data between the MCU and the baseband processor. The TX/RX state control module and transmit/receive FIFOs of the baseband processor are also accessed via the SPI. The SPI clock (SCLK) provided by the MCU is 1 MHz. The SCLK is generated from the MCU and does not need to be synchronized to the system clock used in the PHY baseband chip. The SI, SCLK, and CSn (chip select, active low) pins are inputs from the MCU. The SO pin is used as the data output from the baseband processor. The baseband processor has an interrupt pin (IRQ) to the MCU. The IRQ will notify the MCU of the interrupt.

4. RESULT AND DISCUSSION

Some other coding and decoding schemes that appear extremely promising for achieving low error probabilities and high data rates at reasonable cost are the following: first, convolutional codes with sequential decoding as developed by Wozener, Fano and Reiffin, second, convolutional codes with Massey's thresholding decoding, and third, the Bose-Choudhary codes with the decoding schemes developed by Peterson and Gorenstein. It has been shown by Fano that the arbitrary discrete memory less channels, sequential decoding has a probability of decoding error that is upper bounded by a function of the form $e^{-\alpha n}$. Here n is the constraint length of the code and α is a function of both the channel and the code; α is positive for rates below channel capacity C . Fano also shows that for rates below a certain quantity called $R_{comp} < C$, the average amount of computation in decoding a digit is bounded by a quantity independent of constraint length.

An experimental sequential decoder built at Lincoln Laboratories, Lexington, Massachusetts. By using this decoder in a system with a feedback link and an appropriately designed modulator and demodulator, reliable transmission has been achieved experimentally over telephone circuit at about 7500 bits per second rather than the

1200 or 2400 bits per second possible without coding. The two principle weakness of sequential decoding are as follows: First the amount of computation required per digit is a random variable, and this creates a waiting line problem at the decoder; second, if the decoder once makes an error, a large block of errors can be made before the decoder gets back on the proper track. If a feedback link is available these problem are not serious, but considerable more study is required for cases in which no feedback exists. Threshold decoding is the simplest scheme to implement. It involves only shift register, a few binary adders, and a threshold device. It is most effective at relatively short constraint lengths, and has a somewhat high error probability and less flexibility than sequential decoding.

The computation per digit associated with the Base-Choudhary codes on the BSC increases roughly as the cube of the block length but does not fluctuate widely. The decoding scheme guarantees correction of all combinations of upto some fixed number of errors and corrects nothing beyond. For moderately long block lengths, this restriction in the decoding procedure causes a large increase in P_e . No way is known to make use of the a posteriori probabilities at the output of more general binary input channels. This inability to make use of a posteriori probabilities appears to be a characteristic limitation of algebraic as opposed to probabilistic decoding technique.

The computation per digit associated with low density parity check codes appears to increase at most logarithmically with block length and not to fluctuate widely with the noise. The probability of decoding error is unknown, but is believed to decrease exponentially with block length at a reasonable rate. The ability to decode the digit of a block in parallel makes it possible to handle higher data rates than is possible with other schemes. For many channels with memory, retaining the a posteriori probabilities from the channel makes it practically unnecessary to take account of the memory in any other way. For instance, on a fading channel when the fade persists for several baud lengths, the posterior probabilities will indicate the presence of fade. If the channel were used a BSC however, it would be necessary for the decoder to account for the fact that bursts of errors are more probable than isolated errors. Then, using a posteriori probabilities gives low density decoding and sequential decoding a great flexibility in handling channels with dependent noise. For channels noise is rigidly constrained to occur in short, severe bursts, on the other hand there is a particularly simple procedure for decoding the Bose-Choudhary codes.

When transmitting over channel subject to long fades or long noise bursts, it is often impractical to correct errors in these noisy periods. In such cases it is advantageous to use a combination of error correction and error detection with feedback and retransmission. All of the coding and decoding schemes being considered here fit naturally into such a system, but in case where little or no error correction is attempted, low density codes appear at a disadvantage.

In conclusion all these schemes have their own disadvantage, and clearly no scheme is optimum for all communication situations. It appears that enough coding and decoding alternatives now exist for serious consideration of the use of coding on particular channel.

Table 1. Power Report

	HAMMING CODER	LDPC CODER
TRANSMITTER		
power	54 mw	50 mw
power delay product	653.4 mwns	605 mwns
RECEIVER		
power	57 mw	43 mw
power delay product	1117.2 mwns	361.2 mwns

5. CONCLUSION

Low-density parity-check (LDPC) codes, a class of linear block LDPC codes are used as a replacement to hamming codes which provide a performance advantage with reduced complexity. The power consumed by transmitter and the receiver using hamming encoder are 54mw and 57mw respectively. By using LDPC encoder power consumption of transmitter and receiver is reduced to 50mw and 43mw respectively. Using LDPC the power delay product of the transceiver is also reduced.

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