

Design and Simulation of New Efficient Bridgeless AC-DC CUK Rectifier for PFC Application

Thomas Mathew .T
PG Student,
St. Joseph's College of Engineering,

C.Naresh, M.E.(P.hd)
Associate Professor,
St. Joseph's College of Engineering,

ABSTRACT

This project proposes a new AC-DC bridgeless CUK rectifier. The new bridgeless single-phase AC-DC power factor correction (PFC) rectifiers based on CUK topology are proposed. The absence of an input diode bridge and the presence of only two semiconductor switches in the current flowing path during each interval of the switching cycle result in less conduction losses compared to the conventional CUK power factor correction (PFC) rectifier. The proposed topology is designed to work in discontinuous conduction mode (DCM) to achieve almost a unity power factor and low total harmonic distortion (THD) of the input current. The DCM operation gives additional advantages such as zero-current turn-ON in the power switches, zero-current turn-OFF in the output diode, and simple control circuitry. The circuit is being simulated using MATLAB, the modes of operation are analyzed, the analysis of the circuit parameters will also be performed. The hardware implementation will also be performed.

General Terms

Simulation, MATLAB, rectifier,

Keywords

CUK converter, DCM (discontinuous conduction mode), Power factor correction (PFC)

1. INTRODUCTION

Power supplies with active power factor correction (PFC) techniques are becoming necessary for many types of electronic equipment to meet harmonic regulations and standards, such as the IEC 61000-3-2. Power supply is a buffer circuit that provides power, required by the load from a primary power source with characteristics incompatible with the load. It makes the load compatible with its power source. A Power supply is also known as a power converter and the process is called power conversion. It is also called a power conditioner and the process is called power conditioning. Power supply can be defined as a device that converts the available power of one set of characteristics to another set of characteristics to meet the specified requirements. Typical application of power supplies includes the conversion of a raw input voltage to a controlled or stabilized voltage for the operation of electronic equipment. Switch mode power supplies (SMPS) can be used in applications of high current drain which require a low stable supply voltage. Switching power supplies are of highly efficient devices. The essential feature of a switch mode regulation of DC voltages is that the load is connected to the power source at regular intervals by a semiconductor switch, and then disconnected. The mean value of the voltage applied to the load is maintained at a nearly constant level by an automatic regulation circuit that varies the duration of On and Off periods of the power switch. Most of the PFC rectifiers utilize a boost converter at their front end. However, a conventional PFC scheme has lower

efficiency due to significant losses in the diode bridge. The current flows through two rectifier bridge diodes and the power switch during the switch ON-time, and through two rectifier bridge diodes and the output diode during the switch OFF-time. Thus, during each switching cycle, the current flows through three power semiconductor devices. As a result, a significant conduction loss, caused by the forward voltage drop across the bridge diode, would degrade the converter's efficiency, especially at a low line input voltage. In an effort to maximize the power supply efficiency, considerable research efforts have been directed toward designing bridgeless PFC circuits, where the number of semiconductors generating losses is reduced by essentially eliminating the full bridge input diode rectifier. A bridgeless PFC rectifier allows the current to flow through a minimum number of switching devices compared to the conventional PFC rectifier. Accordingly, the converter conduction losses can be significantly reduced and higher efficiency can be obtained, as well as cost savings.

This paper is organized as follows. Section II presents the conventional CUK rectifier. Section III presents the proposed bridgeless CUK rectifier. Detailed analysis of the converter is presented in this section and Simulation results are provided in Section IV. Section V concludes the paper.

2. CONVENTIONAL CUK RECTIFIER

The circuit diagram of the Cuk converter is shown in Fig.1 consists of AC input voltage source, bridge rectifier with diodes (D_1, D_2, D_3, D_4), input inductor L_1 , controllable switch M_1 , energy transfer capacitor C_1 , diode D_0 , filter inductor L_2 , filter capacitor C_0 , and load resistance R_L . An important advantage of this topology is that continuous current is present at both the input and the output of the converter. Disadvantages of the Cuk converter are a high number of reactive components and high current stresses on the switch, the diode, and the capacitor C_1 . The main waveforms of the converter are presented in Fig. 2 and Fig 3. When the switch is ON, the diode D_0 is reverse biased and the capacitor C_1 is discharged through the switch. With the switch in the OFF state, the diode conducts and currents flow through inductors L_1 and L_2 , whereas capacitor C_1 is charged by the inductor L_1 current. The DC transfer function for the buck, boost, and Cuk PWM DC-DC converters in continuous conduction mode are, D , $1 / (1 - D)$, and $-D / (1 - D)$ respectively, where D is the duty cycle. Therefore the Cuk PWM DC-DC converter circuit can be synthesized by cascading boost and buck converter circuits. The circuit of Fig 4 is the Cuk converter which can be considered as a boost converter cascade with a buck converter, realized with minimum amount of components.

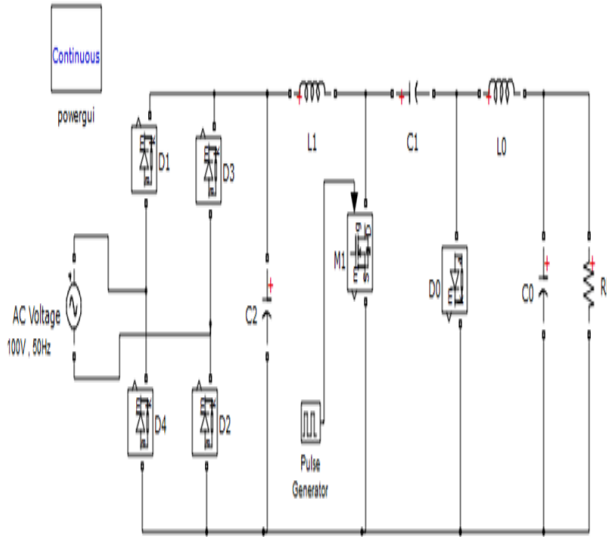


Figure 1: Conventional AC-DC CUK rectifier

The input voltage is given to the converter is 100Vac, 50 Hz.

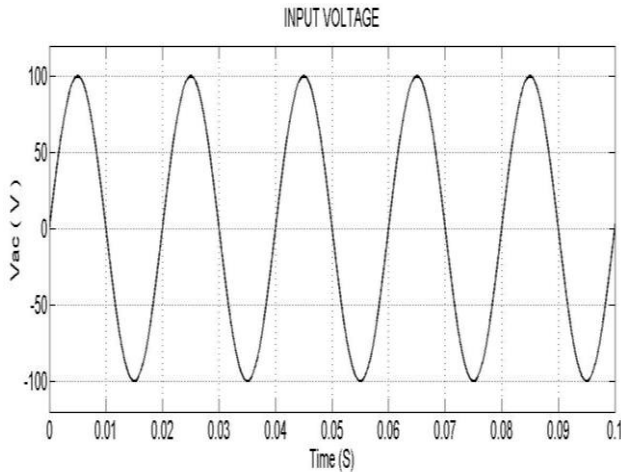


Figure 2: Input voltage

The output power is 150 W. The output voltage is -48V DC .

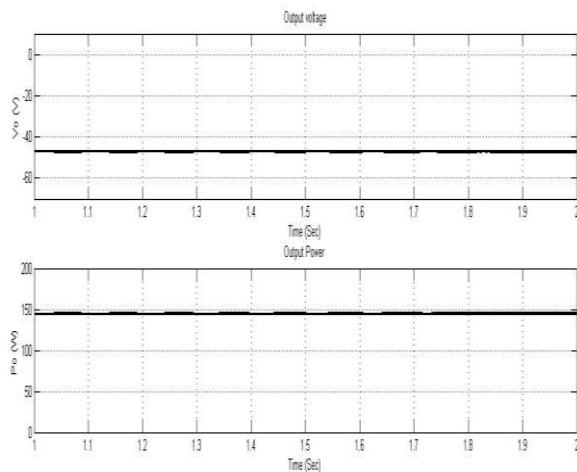


Figure 3. Output power and Output voltage

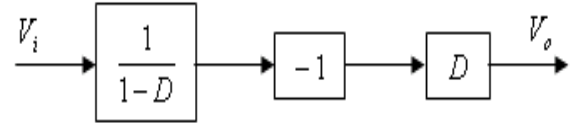


Figure 4: Block diagram representation of CUK DC-DC converter output voltage

3. PROPOSED BRIDGELESS CUK RECTIFIER

The proposed bridgeless Cuk PFC rectifiers is shown in Fig.5. The proposed topologies are formed by connecting two dc–dc Cuk converters, one for each half-line period ($T/2$) of the input voltage. Note that by referring to Figs. 5, there are one or two semiconductor in the current flowing path; hence, the current stresses in the active and passive switches are further reduced and the circuit efficiency is improved compared to the conventional CUK rectifier.

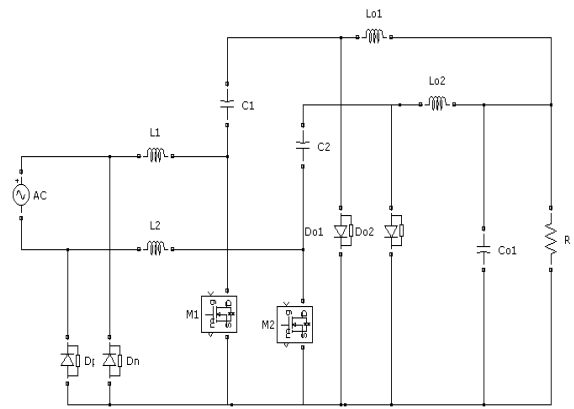


Figure 5: Proposed bridgeless CUK rectifier

The input to this bridgeless CUK rectifier is an AC source (AC) , with two slow-recovery diodes D_p and D_n , two power switches (M_1 and M_2). However, the two power switches can be driven by the same control signal, which significantly simplifies the control circuitry. The output filter capacitor C_o (C_{o1} and C_{o2}) has a large capacitance such that the voltage across it is constant over the entire line period, and a resistive load (R).

3.1 Converter Operation

The proposed bridgeless CUK rectifier has two CUK converter super imposed on each other. The working of the proposed circuit can be divide into two parts

1. Positive half cycle mode
2. Negative half cycle mode

During each modes the switches M_1 and M_2 are turned ON and OFF respectively, with a gate pulse of higher frequency

3.2 Positive Half Cycle:

This mode is active during positive half cycle of the input AC voltage source, during this mode the soft switching diode D_p , is forward biased. The first Cuk circuit, $L_1-M_1-C_1-L_{o1}-D_{o1}$, is active through diode D_p , which connects the input ac source to the output. There are two modes of operation during the positive half cycle,

- I. MODE 1: Switch (M_1) is ON
- II. MODE 2: Switch (M_1) is OFF

3.2.1 Mode – 1

During this mode the switch M_1 is at ON position, current flow is as shown in Fig.6. A pulse signal is given to the gate terminal of the switch (M_1). The switch is ON till the pulse signal is kept high. The diode D_p is forward biased and the inductor (L_1) is energized due to the input voltage source V_{ac} , the inductor current (i_{L1}) increases. Current flow path is as given $V_{ac} - L_1 - M_1 - D_p - V_{ac}$. Due to the capacitor voltage V_{C1} the diode D_{O1} is reverse biased, When $V_{C1} > V_{ac}$, C_1 discharges through M_1 , energy is transferred to the load. As the discharge of the capacitor through the switch (M_1) a part of the energy is stored in the inductor (L_{O1}). The current flow path is show as $C_1 - S_1 - R_L \& C_0 - L_{O1} - C_1$. Thus the load is always connected to the input source.

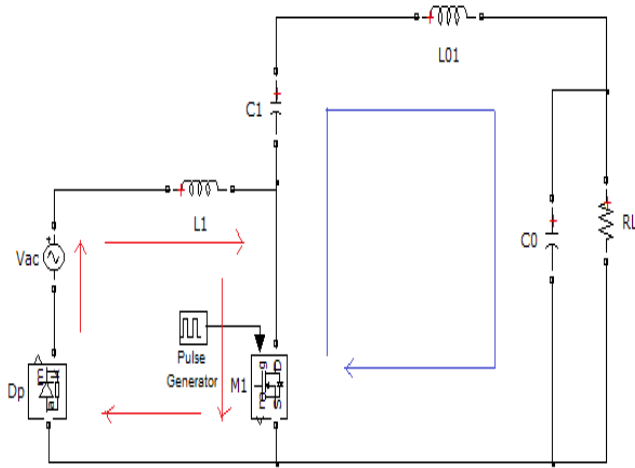


Figure 6 : Mode – 1

3.2.2 Mode - 2

The switch M_1 is turned OFF during this mode. The current flow is as shown in Fig.7, when the pulse signal is low, the capacitor C_1 charges. The current flow path is given by $V_{ac} - L_1 - C_1 - D_{O1} - D_p - V_{ac}$, as shown in the Fig 7. When capacitor voltage (V_{C1}) is greater than the input voltage source V_{ac} , i_{L1} starts decreasing, the energy stored in the inductor is given to the load through the diode D_{O1} . The current flow path is given by $L_{O1} - D_{O1} - R_L \& C_0 - L_{O1}$.

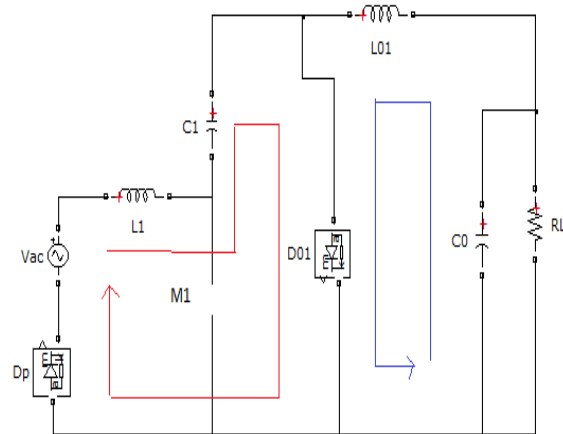


Figure 7: Mode - 2

3.3 Negative Half Cycle:

This mode is active during negative half cycle of the input AC voltage source, during this mode the soft switching diode D_n is forward biased. The second Cuk circuit, $L_2 - M_2 - C_2 - L_{O2} - D_{O2}$, is active through diode D_n , which connects the input ac source to the output load. There are two modes of operation during the positive half cycle,

- III. MODE 3: Switch (M_2) is ON
- IV. MODE 4: Switch (M_2) is OFF

3.3.1 Mode – 3

During this mode the switch M_2 is at ON position, a pulse signal is given to the gate terminal of the switch (M_2). The current flow is as shown in Fig.8. The switch is ON till the pulse signal is kept high. The diode D_n is forward biased and the inductor (L_2) is energized due to the input voltage source V_{ac} , the inductor current (i_{L2}) increases. The current flow path is as given $V_{ac} - L_2 - M_2 - D_n - V_{ac}$. Due to the capacitor voltage V_{C2} the diode D_{O2} is reverse biased, When capacitor voltage V_{C1} is greater than the input voltage source V_{ac} , capacitor (C_1) discharges through M_2 , energy is transferred to the load. As the capacitor discharges through the switch (M_2) a part of the energy is stored in the inductor (L_{O2}). The current flow path is show as $C_2 - M_2 - R_L \& C_0 - L_{O2} - C_2$. Thus the load is always connected to the input source.

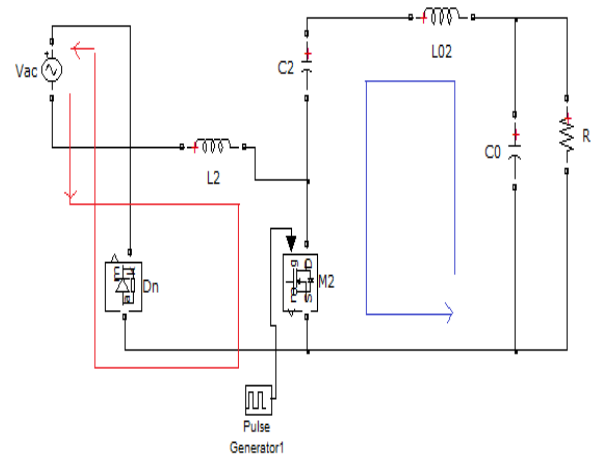


Figure 8: Mode - 3

3.3.2 Mode – 4

The switch M_2 is turned OFF during this mode. The current flow in this mode is as shown in Fig.9. When the pulse signal is low, the capacitor C_2 charges. The current flow path is given by $V_{ac} - L_2 - C_2 - D_{O2} - D_n - V_{ac}$. When capacitor voltage (V_{C2}) is greater than the input voltage source V_{ac} , i_{L2} starts decreasing, the energy stored in the inductor is given to the load through the diode D_{O2} . The current flow path is given by $L_{O2} - D_{O2} - R_L \& C_0 - L_{O2}$.

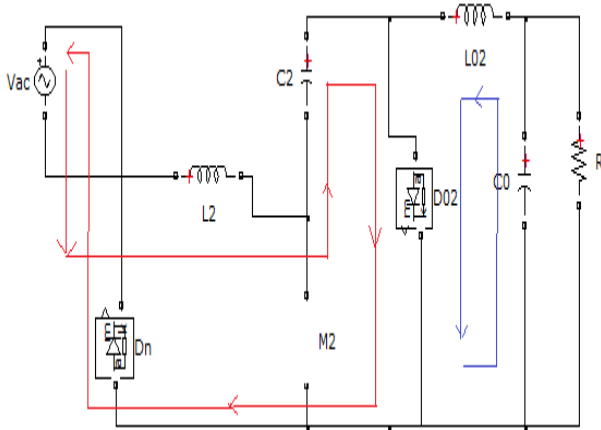


Figure 9 : MODE 4

3.4 Design Values Of Components

The design values of components used in the simulation are as shown below

Input Inductors (L_1 and L_{01})	- 1mH
Output inductors (L_2 and L_{02})	- 22 μ H
Energy storage Capacitor (C_1)	- 1 μ F
Filter capacitor (C_0)	- 12000 μ F
Load Resistor (R_L)	- 15 Ω

4. SIMULATION RESULTS

The simulation circuit of the proposed converter is shown in Fig.10. The input AC voltage given to the converter is 100V, 50Hz. The pulse signals to the switches M1 and M2 are given using a pulse generator, with the switching frequency of 25KHz and pulse width of 25% ($D=0.25$). The input AC voltage given to the converter is 100V, 50Hz as shown in the Fig 11. The gate pulses of 1 V, 25KHz, $D=0.25$ applied to the MOSFETs of the proposed converter circuit are as shown in the Fig12. The input current and voltage of the proposed bridgeless CUK rectifier is shown in Fig13. The input voltage is 100V, 50Hz and the current is 3.5A. The output power, output current and voltage is shown in the Fig.14 and Fig.15. The circuit is designed to have output power of 150W and output voltage of -48V.

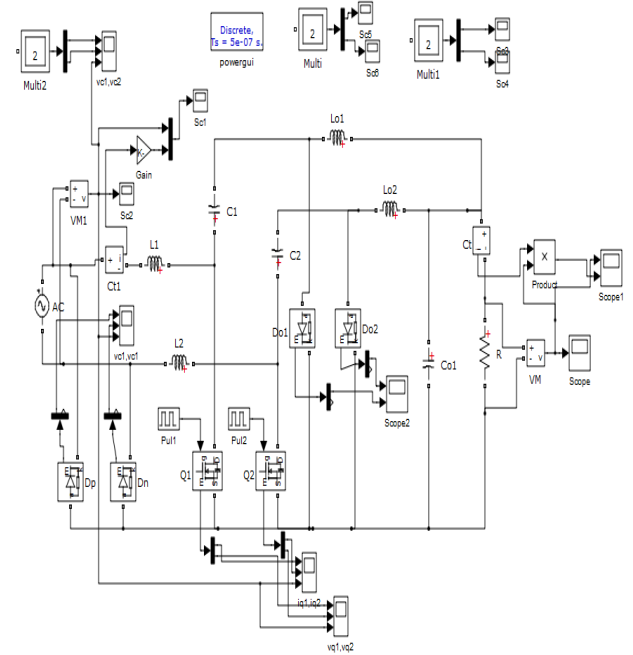


Figure 10: Simulation Proposed converter circuit

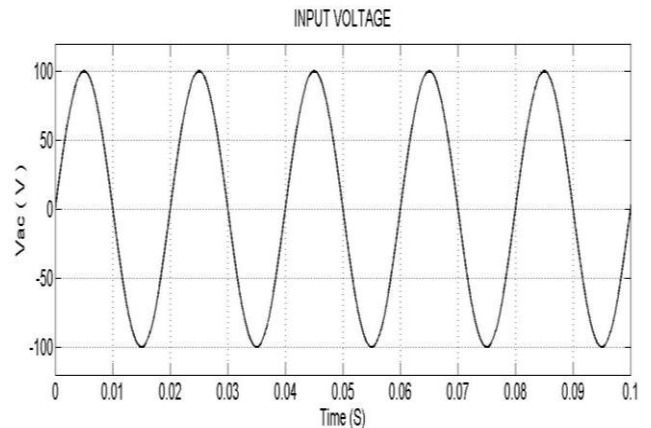


Figure 11 : Input voltage

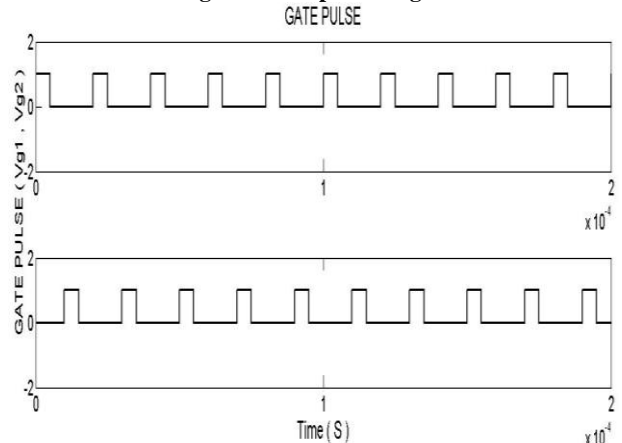


Figure 12 : Gate pulses to the proposed converter

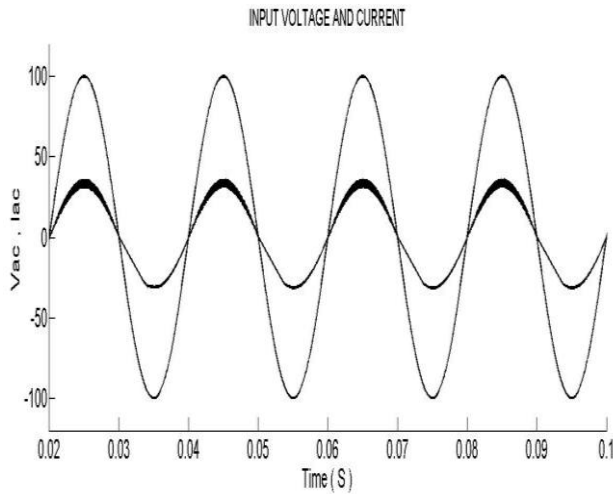


Figure 13: Input Voltage and Current

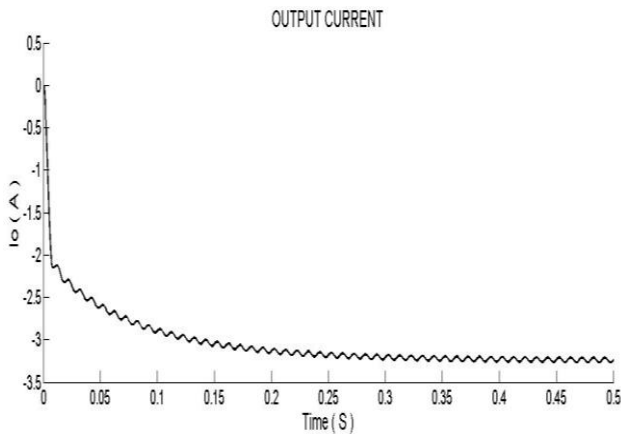


Figure 14 : Output current

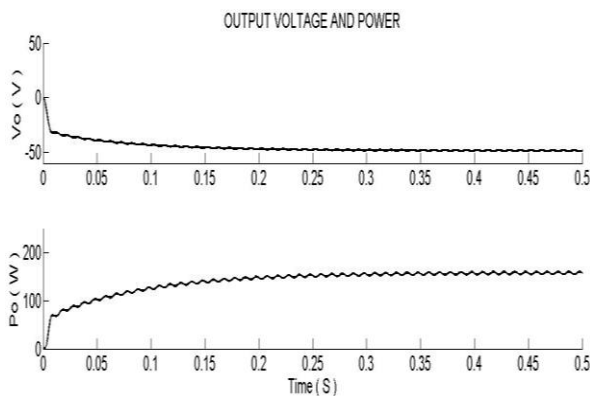


Figure 15 :Output power and output voltage

5. CONCLUSION

Thus a new bridgeless AC-DC CUK rectifier is discussed in this paper. The modes of operation and the required simulated waveforms are shown. The proposed circuit can be further simulated and designed with only one switch. The conventional circuit and the proposed circuit are compared with the output power of 150W and output voltage of -48V. The proposed circuit has low THD and the power factor is almost equal to unity .

6. REFERENCES

- [1] W. Choi, J.Kwon, E. Kim, J. Lee, and B.Kwon, "Bridgeless boost rectifier with low conduction losses and reduced diode reverse-recovery problems," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 769–780, Apr. 2007.
- [2] G. Moscho poulos and P. Kain, "A novel single-phase soft-switched rectifier with unity power factor and minimal component count," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 566–575, Jun. 2004.
- [3] R.-L. Lin and H.-M. Shih, "Piezoelectric transformer based current-source charge-pump power-factor-correction electronic ballast," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1391–1400, May 2008.
- [4] S. Dwari and L. Parsa, "An efficient AC–DC step-up converter for low voltage energy harvesting," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2188–2199, Aug. 2010.
- [5] Y. Jang and M. Jovanovic, "A bridgeless PFC boost rectifier with optimized magnetic utilization," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 85–93, Jan. 2009.
- [6] L. Huber, Y. Jang, and M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May 2008.
- [7] B. Su and Z. Lu, "An interleaved totem-pole boost bridgeless rectifier with reduced reverse-recovery problems for power factor correction," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1406–1415, Jun. 2010.