Simulation and Implementation of Single-Phase Single-Stage High Step-Up AC–DC Matrix Converter based on Cockcroft–Walton Voltage Multiplier

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ABSTRACT
This paper proposes a high-performance transformer less single-stage high step-up ac–dc matrix converter using a Cockcroft–Walton (CW) voltage multiplier. Employing an eight unidirectional-switch to form four bi-directional switch matrix converters between the ac source and CW circuit, the proposed converter provides high quality of line conditions, adjustable output voltage, and low output ripple. The matrix converter is operated with two independent frequencies. One of which is associated with power factor correction (PFC) control, and the other is used to set the output frequency of the matrix converter. Moreover, the relationship among the latter frequency, line frequency, and output ripple will be discussed. A commercial control IC associating with a pre-programmed complex programmable logic device is built as the system controller. The operation principle, control strategy, and design considerations of the proposed and modified converter are all detailed in this paper. The simulation results demonstrate the high performance of the proposed and modified converter and the validity for high step-up ac–dc applications.

Keywords
Cockcroft–Walton(CW) voltage multiplier; high step-up ac–dc matrix converter.

1. INTRODUCTION
The Matrix converter (MC) offers possible "all silicon" solution for AC-AC conversion, removing the need for reactive energy storage components used in conventional converter system. The use of direct AC-AC converter based on matrix converter topology is restricted due to inherent limitations [1]. One of those limitations is the absence of the natural free- wheeling path afforded in conventional converter topology through the use of diodes. The Matrix Converter is a forced commutated converter which uses an array of controlled bidirectional switches as the main power elements to create a variable output voltage system with unrestricted frequency [2]. The SPMC requires 4 bidirectional switches each capable of conducting current in both directions, blocking forward and reverse voltages. It requires the use of bidirectional switches capable of blocking voltage and conducting current in both directions.

The AC-AC matrix converters have received tremendous attention in the past few decades due to their distinct features such as: direct AC-AC power conversion; elimination of the DC bus reactive element (capacitor); ability to feed energy back to the AC utility line; sinusoidal input and output currents and controllable input current displacement power factor, which is achieved independently of the load type by proper modulation [3]. The intermediate DC-link can be a critical component, especially in high-power or high-voltage Applications, since it is large and expensive, and has a limited lifetime [4]. The line inductors are also a burden to the system since their size is usually 20-40% of the system size if a switching frequency of several kilohertz is assumed [4]. High cost, large size, heavy weight, and energy loss are the drawbacks of the conventional AC-DC-AC conversion process.

2. COCKCROFT-WALTON VOLTAGE MULTIPLIER
The Cockcroft-Walton (CW) is a voltage multiplier that converts AC or pulsing DC electrical power from a low voltage level to a higher DC voltage level. It is made up of a voltage multiplier ladder network of capacitors and diodes to generate high voltages. Unlike transformers, this method eliminates the requirement for the heavy core and the bulk of insulation/potting required. Using only capacitors and diodes, these voltage multipliers can step up relatively low voltages to extremely high values, while at the same time being far lighter and cheaper than transformers. The biggest advantage of such circuits is that the voltage across each stage of the cascade is equal to only twice the peak input voltage in a half wave rectifier. In a full wave rectifier it is three times the input voltage. It has the advantage of requiring relatively low cost components and being easy to insulate. One can also tap the output from any stage, like a multi tapped transformer. Operation of the CW multiplier, or any voltage doubler, is quite simple. Considering the simple two-stage version diagrammed within, which is attached to an AC power source on the left side of the diagram. At the time when the AC input reaches its negative pole the leftmost diode is allowing current to flow from the ground into the first capacitor, filling it up.

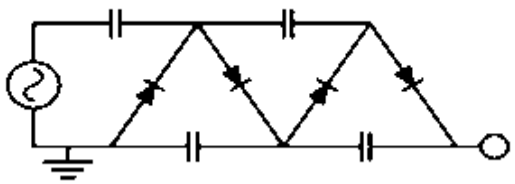


Fig 1: Cockcroft Walton Voltage multiplier

When the same AC signal reverses polarity, current flows through the second diode filling up the second capacitor with both the positive end from AC source and the first capacitor charging the second capacitor to twice the charge held in the first. With each change in polarity of the input, the capacitors add to the upstream charge and boost the voltage level of the capacitors downstream, towards the output on the right. The increase in voltage, assuming perfect conditions, is twice the input voltage times the number of stages in the multiplier.

2.1 Operational Characteristics

CW multipliers are typically used to develop higher voltages for relatively low current applications such as bias voltages ranging from tens or hundreds of volts to millions of volts for high-energy physics experiments or lightning safety testing. CW multipliers are also found, with a higher number of stages, in laser systems, high-voltage power supplies, X-ray systems, LCD backlighting, traveling wave tube amplifiers, ion pumps, electrostatic systems, air ionisers, particle accelerators, copy machines, scientific instrumentation, oscilloscopes, TV sets and CRTs, bug zappers and many other applications that use high-voltage DC.

3. CONVENTIONAL N-STAGE CW VOLTAGE MULTIPLIER

As shown in Fig. 2, the well-known CW voltage multiplier is constructed by cascading a number of diode–capacitor stages with each stage containing two capacitors and two diodes. Theoretically, an *n*-stage CW voltage multiplier provides dc voltage with the value of 2*n* times of the magnitude of the ac voltage source under no-load condition. However, the dc output voltage is practically less than the theoretic value due to no-ideal characteristics of the

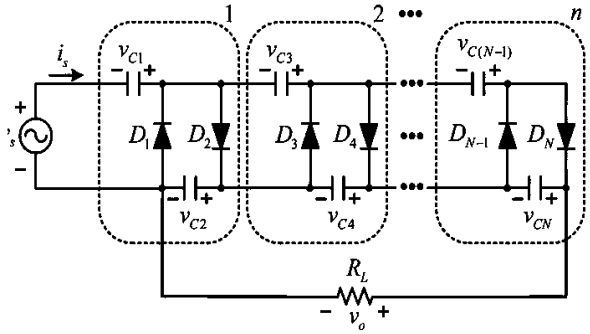


Fig 2: Conventional *n*-stage CW voltage multiplier.

circuit components [5], [6], [7].Under heavy-load condition, the CW multiplier intrinsically presents not only poor output voltage regulation but also high output ripple with line frequency. In some applications, line frequency transformers with high step-up ratio were generally used to cooperate with the CW voltage multiplier for higher voltage gain. However, sourced by the utility ac source, the transformers lead to inefficiency of bulk and cost, and the ripple problem still unsolved [8].Taking the advantages of the high-frequency switching technologies, many modified CW circuits have been developed for saving the volume of the transformers, smoothing the output ripple, and regulating the output voltage. In [9]–[11], some voltage-fed modified CW topologies, which provide not only high voltage gain but also simplicity of implementation, were proposed. Nevertheless, among these topologies, the high frequency transformer with high turn's ratios causes large winding capacitance and leakage inductance, which leads to high voltage and current stresses and higher switching losses on the switches. Moreover, operating in discontinuous conduction mode (DCM), these topologies incur more stress, losses, and electromagnetic interference (EMI) problems. In [12], series, parallel, and hybrid resonant converters incorporated with high-frequency and high step-up transformer were proposed to energize a CW circuit, in which the non ideal components of the transformer were under consideration. However, these converters were supplied only by dc sources. In [13]–[15], soft switching techniques were applied to resonant-type CW circuits to reduce switching losses on power switches for enhancing the system efficiency. In addition to these modified CW circuits, up to now, some cascaded single-switch step-up dc–dc converters without step-up transformer were also proposed in [16]–[18], which provided high voltage gain with advantages of simplicity and cost efficiency.

However, capacitors of these topologies with higher voltage rating are needed when higher numbers of stages are deployed. In [18], a modified topology, with integrated multiphase boost converter and voltage multiplier, was proposed for high step-up conversion and high-power applications as well. In this topology, all capacitors in the voltage multiplier had identical voltage rating. Moreover, some non isolated high step-up dc–dc converters with low-voltage dc input were proposed for renewable energy applications [19]–[22]. However, except sourced by dc power, such as photovoltaic generators, fuel cells, or batteries, these converters required a front stage for linking to the ac line. Some power factor correction (PFC) techniques have to apply to the front stage; otherwise, the converter will incur poor line quality.

Some standards have been already available to improve this situation, such as IEC519, IEC555, and IEC1000- 3-2 [23]–[25]. A lot of ac–dc converters with PFC techniques have been developed and applied into various types of electrical equipment [26]–[32]. In [26], the ac–dc topologies with high line quality were reviewed and classified, and most of them used hard-switching techniques. In [27] and [28], some modified boost PFC circuits with soft-switching techniques were proposed for enhancing the utilization of energy. However, only few of them were applied to high-voltage applications. In [29], a two-stage structure cooperated with conventional CW circuit was proposed for high-voltage dc applications. Although providing good line condition and fast response, this topology demonstrated complexity and cost inefficiency. In [30], a single-stage transformerless topology integrated with a single phase ac–ac converter and Dickson charge pump circuit was proposed for achieving high voltage gain and improving line conditions. Nevertheless, the voltage gain of this converter depended on duty cycles of switch current, capacitor current, the switching frequency, and switching load resistance. This led to complicated design considerations. Another topology with soft switching technique, which consisted of a conventional single phase boost ac–dc circuit, a four-switch full-bridge converter, a high step-up transformer, and a high-voltage rectifier, was proposed for high-voltage dc applications [31]. Applying PFC, this topology achieved high line quality, but efficiency and cost had to be considered for practical applications. In [32], a single-stage single-phase ac to high-voltage dc converter based on the CW voltage multiplier without step-up transformer was presented. Adding one boost inductor and one bidirectional switch to a conventional CW circuit, this converter provided simplicity, high efficiency, good line condition, and regulated dc output. Moreover, the control strategy for conventional single-switch boost ac–dc converter with PFC can be easily adopted for this converter.

However, low ripple output still could not achieve by this structure. A previous work on the proposed converter was conducted and presented in [33], in which a high step-up dc–dc converter based on CW voltage multiplier was discussed, i.e., the converter was energized by a dc source. In [33], four unidirectional switches formed the main converter and two independent switching frequencies were used to operate these switches. Successively, the unidirectional switches are replaced by bidirectional switches and the dc source is

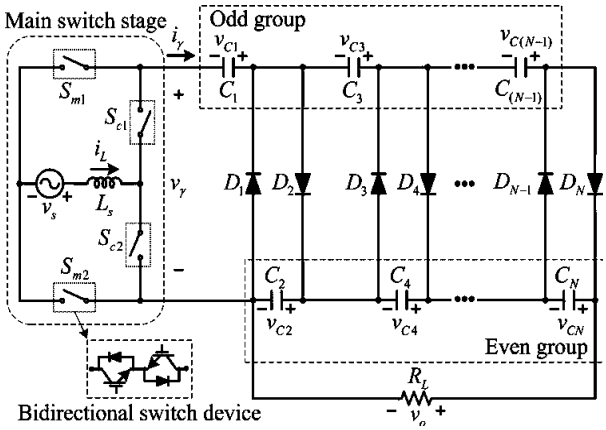


Fig 3: Circuit configuration of the proposed converter

replaced by an ac source. By these replacements, the high step-up ac–dc converter proposed in this paper is shown in Fig. 3. The arrangement of the four bidirectional switches can be seen as a single-phase matrix converter deployed between the ac source and the CW circuit. With the help of the boost structure, in the proposed converter, not only the voltage gain can be higher than that of the conventional one but also the PFC technique can apply to the matrix converter to achieve high quality of line conditions and dc output regulation. In this paper, only continuous conduction mode (CCM) is discussed for its promising less stress, loss, and EMI problems. Moreover, the proposed converter deploys a single-phase matrix converter, which employs two independent frequencies. One of the frequencies applies to two of the four switches to perform PFC function, and the other applies to the rest of the two switches to determine the output frequency of the matrix converter. The latter frequency determines the output frequency of the matrix converter and, then, can be used to smooth the ripple voltage in the dc output. Even deploying bidirectional switches, the proposed converter can adopt PFC control methods of conventional ac–dc boost converters just with some modifications. Therefore, some commercial control ICs with PFC function can be easily applied to the proposed converter with an extra auxiliary circuit which modifies the original switching signal to trig the four bidirectional switches properly.

4. STEADY STATE ANALYSIS

The proposed configuration is mainly composed of a single phase matrix converter cascaded with a traditional *n*-stage CW voltage multiplier, as shown in Fig. 3. The single-phase matrix converter forms with four bidirectional switches that are divided into two sets denoted as (S_{c1}, S_{c2}) and (S_{m1}, S_{m2}). The proposed converter is energized by a line-frequency ac source with a series inductor for boost operation. Till now, commercial products of bidirectional switches are not available [34]; thus, two anti series insulated gate bipolar transistors with freewheel diode are used as a bidirectional switch in this paper.

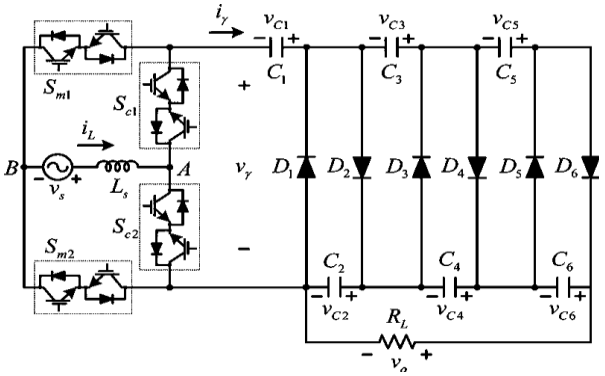


Fig 4: Proposed converter with a three-stage CW voltage multiplier.

4.1 Circuit Operation Principle

In order to simplify the analysis of circuit operation, a three stage CW voltage multiplier is used in the proposed converter, as shown in Fig. 4. Before analyzing, some assumptions are made as follows:

1) All of circuit elements are ideal and there is no power loss in the system.

2) All of the capacitors in the CW voltage multiplier are sufficiently large, and the voltage drop and ripple of each Capacitor can be ignored under a reasonable load condition. Thus, the voltages across all capacitors are equal, except the first capacitor which voltage is one half of the others.

3) The proposed converter operates in CCM and under steady-state condition.

4) During demagnetizing period of the boost inductor, only one of the diodes in CW circuit will conduct. This phenomenon was discussed in [32].

5) To avoid the open-circuit of the inductor, a safe commutation technique is practically used in the control strategy, which provides some overlap of the trig signals between S_{c1} and S_{c2}. According to the second assumption, each capacitor voltage in the CW voltage multiplier can be defined as

$$v_{Ck} = \begin{cases} V_C, & \text{for } k = 1 \\ 2V_C, & \text{for } k = 2, 3, \ldots, N \end{cases} \qquad (1)$$

where v_{Ck} is the voltage of the *k*th capacitor, V_C is the maximum peak value of terminal voltage of the CW voltage multiplier under steady-state condition, and $N = 2n$.

For an *n*-stage CW voltage multiplier, the output voltage is equal to the total voltage of all even capacitors, which can be expressed as

$$V_o = \text{NVC} \qquad (2)$$

where V_o is the steady-state dc output voltage.

Substituting (2) into (1), each capacitor voltage can be rewritten as

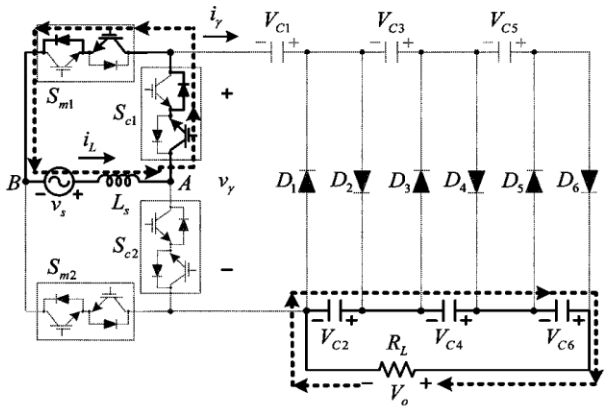
According to the polarity of the ac source and the switching state of S_{c1} , there are four operation modes of the proposed

$$v_{Ck} = \begin{cases} V_o/N, & \text{for } k = 1 \\ 2V_o/N, & \text{for } k = 2, 3, \ldots, N. \end{cases} \quad (3)$$

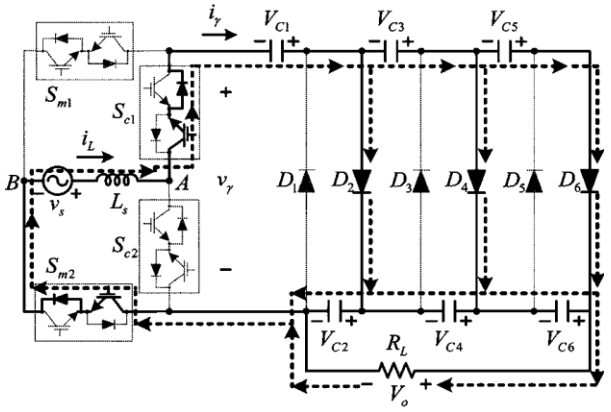
converter, denoted as modes I–IV. Moreover, combining with boost operation, each mode has two circuit states. Fig. 5 shows the two circuit states of mode I, which provides positive i_γ during positive-half cycle of the ac source, and Fig. 6 shows the two circuit states of mode II, which provides negative i_γ during negative-half cycle of the ac source. For simplicity, the circuit states of modes III and IV are not presented, and they can be obtained by changing the directions of i_γ and i_L from Figs. 5 and 6, respectively.

Obviously, S_{m1} and S_{m2} work as boost switches while S_{c1} and S_{c2} control the direction of i_γ , i.e., the output frequency of the matrix converter. Basically, S_{c1} (S_{m1}) and S_{c2} (S_{m2}) should be operated in complimentary mode and the operating frequencies of S_{c1} and S_{m1} are defined as f_c and f_m, respectively, where f_c is called alternating frequency and f_m is called modulation frequency.

For convenience, a simple case is used to explain the operation principle of the proposed converter. In this simple case, f_c is twice as large as line frequency and f_m = 60 kHz.



(a)



(b)

Fig. 5: Circuit states and conducting paths of the proposed converter at mode-I. (a) State 1. (b) State 2.

Fig. 7(a) shows some selected waveforms including the trig signals for the four bidirectional switches. According to the trig signals of S_{c1} and S_{c2} , which are complementary with 50% duty, the four modes spread over a line cycle equally. A PFC control method is applied to the matrix converter, which will be detailed later; thus, the line current is nearly sinusoidal and in phase with the line source. In accordance with the timing of v_s and S_{c1}, the pulse-shape current i_γ has discontinuous sinusoidal envelops. The behaviour between i_γ and CW circuit will be explained later in this section. Fig. 7(b) and (c) shows the zoom-in waveforms of i_L for modes I and II, respectively. The two states in modes I and II are related to the pulse width modulated (PWM) signals of S_{m1} and S_{m2}, and in state 2, $i_\gamma = \pm i_L$, where "+" is for mode I and "–" is for mode II. The circuit behaviour in modes I and II will be given in the following:

1) *State 1 in mode I [see Fig. 5(a)]:* During *DTm* interval, S_{m1} and S_{c1} are turned ON, the boost inductor is charged by the input source, i_γ is zero due to no current path, the even-group capacitors *C*6, *C*4, and *C*2 supply to the load *RL* , and the odd-group capacitors *C*5, *C*3, and *C*1 are floating.

2) *State 2 in mode I [see Fig. 5(b)]:* During (1–D)*Tm* interval, S_{m2} and S_{c1} are turned ON, the boost inductor and input source transfer energy to the CW circuit by positive i_γ flowing through one of the even diodes [32]. The ON/OFF states of the diodes and charging behaviour of the capacitors can be found in [32] as well.

3) *State 1 in mode II [see Fig. 6(a)]:* During *DTm* interval, S_{m2} and S_{c2} are turned ON, the boost inductor is charged by the input source, i_γ is zero due to no current path, the even-group capacitors *C*6, *C*4, and *C*2 supply to the load *RL* , and the odd-group capacitors *C*5, *C*3 and *C*1 are floating.

4) *State 2 in mode II [see Fig. 6(b)]:* During (1–D)*Tm* interval, S_{m1} and S_{c2} are turned ON, the boost inductor and input source transfer energy to the CW circuit by negative i_γ flowing through one of the odd diodes [32]. The ON/OFF states of the diodes and charging behaviour of the capacitors can be found in [32] as well.

The circuit behaviours of modes III and IV can be obtained by similar processes but with opposite directions of both i_γ and i_L.

4.2 Derivation of the Ideal Static Voltage Gain

In this paper, the proposed converter is sourced by a sinusoidal voltage source, which can be expressed as

$$v_s = \sqrt{2} Vs \sin \omega_s t \quad (4)$$

where v_s is the line source, and *Vs* and ω_s are the rms value and angular frequency of v_s , respectively. During state 1 in mode, from Figs. 5(a) and 6(a), it can be seen that the voltage across nodes A and B is zero; thus, the current variation of i_L can be represented as where *Ls* is the boost inductor, *D* is the duty cycle of S_{m1} in modes I and III or the duty cycle of S_{m2} in modes II and IV, and *Tm* = 1/ f_m is the modulation period each. From Figs. 5(b) and 6(b) and (4), it can be seen that during

$$\Delta i_{L(\text{on})} = \frac{v_s}{L_s} DT_m \quad (5)$$

state 2, the voltage across nodes A and B is equal to V_o /*N* both in modes I and II. Similarly, the terminal voltage V_{AB} is equal to $-V_o$ /*N* both in modes III and IV. Thus, the polarities

of the terminal voltage V_{AB} in positive- and negative-half cycles have opposite sign. Consequently, the current variation of i_L can be represented as

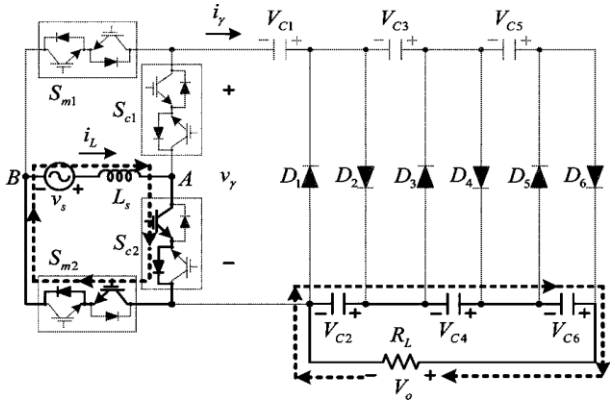
$$\Delta i_{L(\text{off})} = \frac{v_s - \text{sign}(v_s) \cdot V_o/N}{L_s}(1-D)T_m \qquad (6)$$

where sign (v_s) denotes the sign of *vs*. From (6) and (7), the average inductor voltage over one modulation period T_m can be expressed as

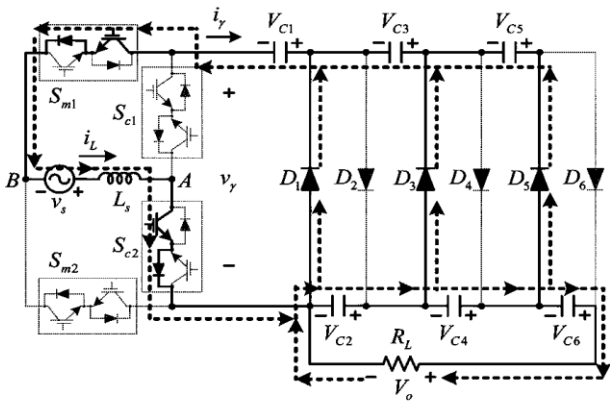
$$L_s \frac{\Delta i_L}{T_m} = L_s \frac{\Delta i_{L(\text{on})} + \Delta i_{L(\text{off})}}{T_m} \qquad (7)$$

where Δi_L is the variation of line current over one modulation period T_m.

If L_s is small enough, its influence on the low-frequency components of the converter waveforms is negligible, and the ideal static voltage gain of the proposed converter can be derived from (4)–(7).



(a)



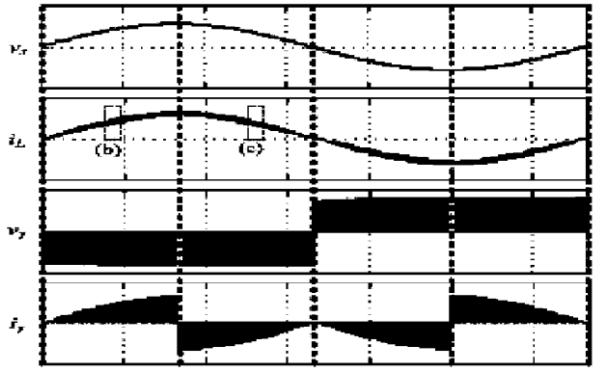
(b)

Fig 6: Circuit states and conducting paths of the proposed converter at mode II. (a) State 1. (b) State 2.

$$M_V = \frac{V_o}{|v_s|} = \frac{N}{1-D} \qquad (8)$$

Where M_V is the ideal static voltage gain and |*vs* | is the absolute value of line source v_s .

Under suitable PFC control, the output voltage can be regulated as a constant dc value by adjusting *D*. According to (4) and (8), Fig. 8 shows the duty cycle varying within positive- or negative-half cycles of the line source *vs* with different number of stages of CW circuit. For comparison, the corresponding duty cycle of a classic ac–dc boost converter with $V_o/\sqrt{2}V_s$ = 8 is presented as well. It can be seen that with such high-gain requirement, the classic ac–dc boost converter with $V_o/\sqrt{2}V_s$ = 8 is presented as well. It can be seen that with such high-gain requirement, the classic ac–dc boost converter



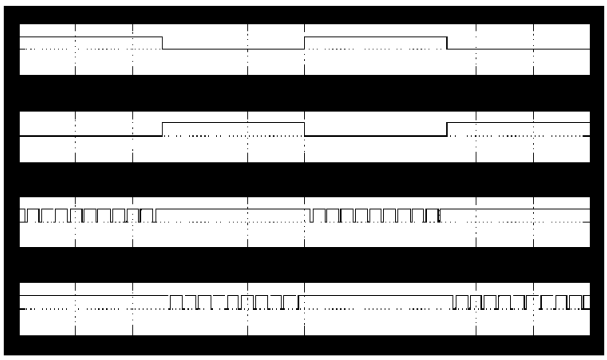


Fig 7: Some selected waveforms of the proposed converter for illustrating operation modes. (a) Waveforms of v_s , i_L , v_γ , i_γ , and trig signals for *Sm* 1 , *Sm* 2 ,*Sc* 1, and *Sc* 2.

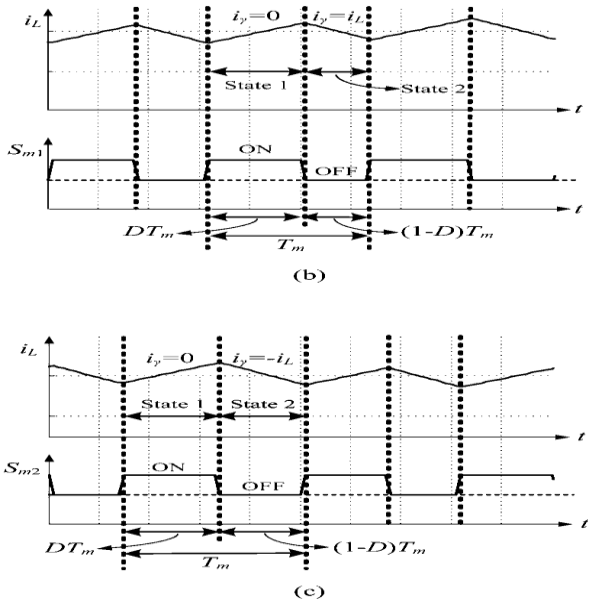


Fig 7: (b) Zoom-in waveforms of i_L and *Sm* 1 at mode I. (c) Zoom-in waveforms of i_L and *Sm* 2 at mode II.

almost operates with duty cycle higher than 0.875, which is not reasonable for practical application [23], while for the proposed converter, the duty cycles are in more reasonable regions.

5. SIMULATION RESULTS

5.1 Proposed Method

Third stage simulation circuit is shown in fig 8. Substation for proposed method is shown in fig 9. Input current waveform is shown in fig 10. Output waveform for proposed method is shown in fig 11.

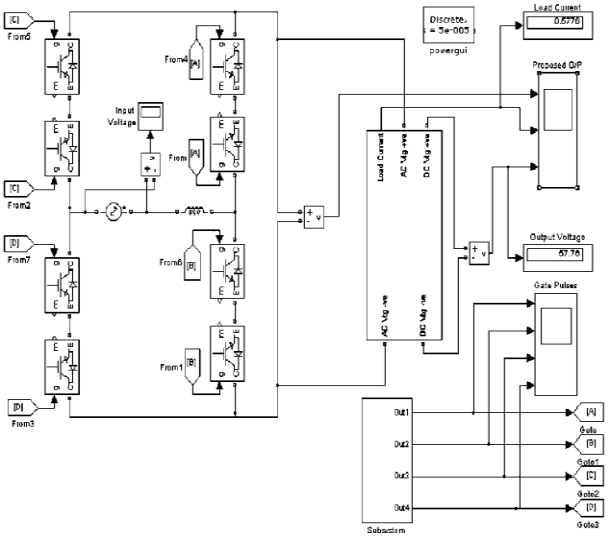


Fig 8: Proposed System

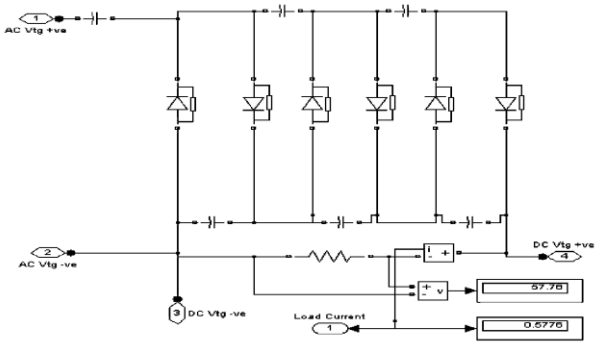


Fig 9: Sub-system for Proposed

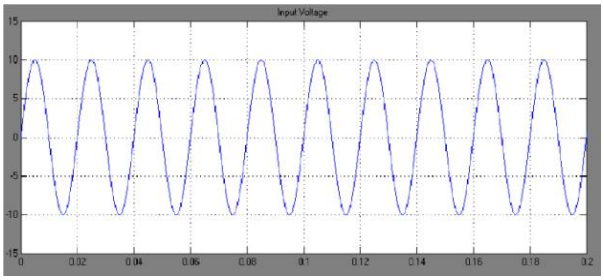


Fig 10: Proposed Input Voltage

In this simulation designed for proposed and modified system. In modified system Cockcroft-Walton circuit increased one more stage. For this modified further reference has been done and improve output voltage. To form four bi-directional switches using eight unidirectional switches. Because normal bi-directional switches was formed by connecting collector and emitter. But in this formation need to connect two switches emitter and forms bi-directional switches and form matrix converter.

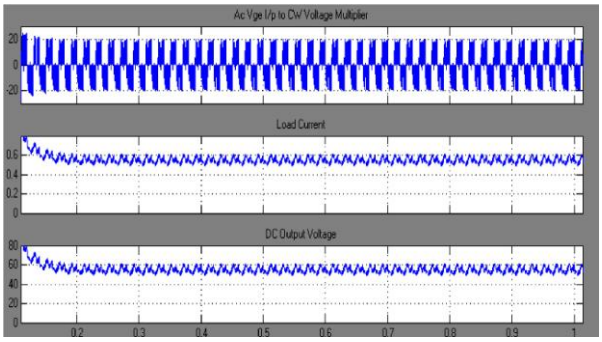


Fig 11: Proposed Output waveform

In matrix converter using one boost inductor to boost input voltage. Sub-system created for CW voltage multiplier it shown in the Fig 9 & 13. By using scope output of matrix converter, voltage multiplier's voltage and current also measured successfully.

5.2 Modified Method

Fourth stage simulation circuit is shown in fig 12. Substation for modified method is shown in fig 13. Input current waveform is shown in fig 14. Output waveform for modified method is shown in fig 15.

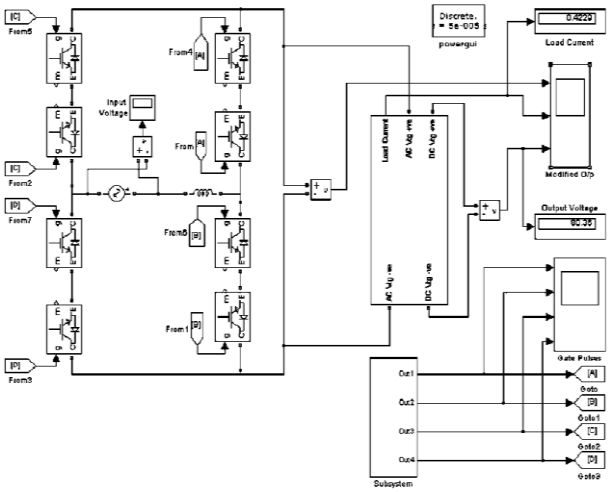


Fig 12: Modified System

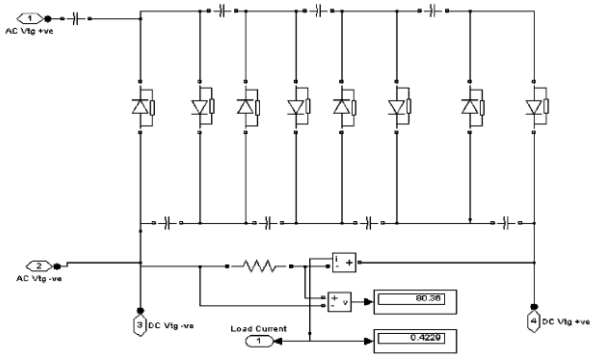


Fig 13: Sub-system for Modified

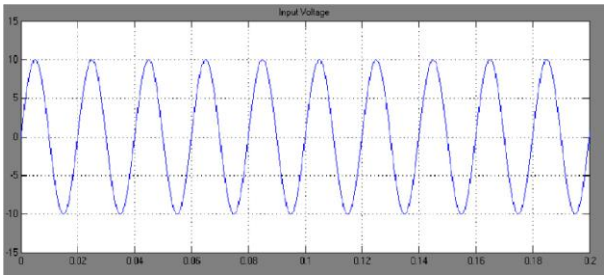


Fig 14: Modified Input Voltage

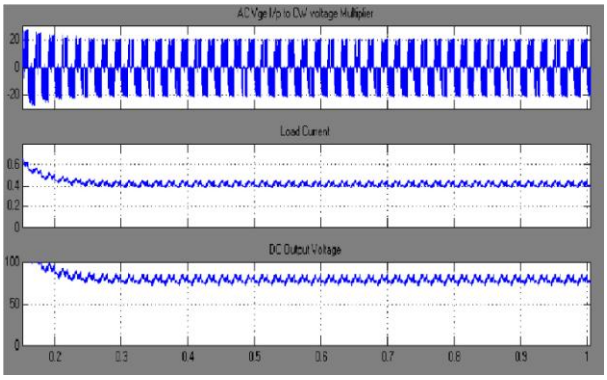


Fig 15: Modified Output waveform

Table 1. Summary of proposed and modified method

Sl. no	Datas	3rd Stage		4th Stage	
		Input	Output	nput	Output
1	Voltage	10V	57.76V	10V	80.55 V
2	Frequency	50Hz	----	50Hz	----
3	Boost Inductor	1e-3	----	1e-3	-----
4	Resistor (Load)	100Ω	----	190Ω	----

6. CONCLUSION

This paper explains the single-stage high step up transformerless ac–dc matrix converter using cockcroft-walton voltage multiplier. Structural parts of the circuits are described in detail. Switching strategy and operational principles of the proposed converters are explained and operational topologies are respectively given. This circuit is used to step-up the voltage without using transformer. This circuit is specially designed for high power rating. From these results the switching strategies are studied. Both proposed and modified output results are compared.

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