

Design of Gate-All-Around Tunnel FET for RF Performance

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ABSTRACT

This paper presents the design, radio frequency (RF) performance and high frequency stability of Gate-All-Around Tunnel Field Effect Transistor (GAA TFET). The small signal parameters that can be extracted using a non-quasi static small signal model are calculated using extracted parameters from a technology computer-aided design (TCAD) simulation. RF parameters like cut-off frequency (f_t), maximum oscillation frequency (f_{max}) and stability factor (K) are extracted to evaluate the high frequency performance of GAA TFET. The result shows that the GAA TFET has cut-off frequency of 22GHz and unconditionally stable from 1GHz onwards.

General Terms

VLSI, RF

Keywords

Radio Frequency, Tunnel FET, Small-signal model, Stability Factor, TCAD Simulation.

1. INTRODUCTION

The conventional MOSFETs when scaled down to nanometer length run into performance limitations such as increased leakage current and short channel effects. Over the last few years, extensive research to develop novel device structures like multi gate FETs (MuGFETs), fully depleted silicon-on-insulator MOSFETs and silicon nanowire MOSFETs have been proposed to resolve the problems arising from MOSFET scaling limitation. These devices have shown improvements in channel controllability, current drivability and RF performances. However recently, reducing power dissipation in semiconductor devices has been considered to be as important as improving their performance. In order to improve the energy efficiency of electronic circuits, Tunnel FETs are interesting candidates to replace or complement the MOSFETs used today. Tunnel FETs, which are gated p-i-n diodes whose on-current arise from band-to-band tunnelling, are attractive new devices for low-power applications as they have lower I_{off} , small subthreshold swing and low standby power consumption compared to conventional MOSFETs [1]. When the device is turned on, the carriers tunnel through the barrier for current to flow from source to drain. When the device is off, the barrier keeps the off-current extremely low, several orders of magnitude lower than the off-current of MOSFETs [2]. A gate-all-around structure is chosen to improve the on-current, while the off-current is furthermore lowered. This paper describes the design and RF behaviour of GAA TFET. The values of f_{max} , f_t and K have been obtained from extracted parameters using 2D technology computer aided design (TCAD) simulation.

2. DEVICE STRUCTURE AND SIMULATION

Figure.1 shows the designed GAA TFET of gate length (L_G) 30nm and gate dielectric thickness (t_{ox}) 1nm. The device has a p^+ source region, an intrinsic channel region and an n^+ drain region with uniform doping concentration of $1 \times 10^{20} \text{ cm}^{-3}$, $1 \times 10^{17} \text{ cm}^{-3}$ and $1 \times 10^{20} \text{ cm}^{-3}$ respectively. Figure.2 shows the drain current characteristics obtained as a function of gate voltage through device simulation on linear scale.

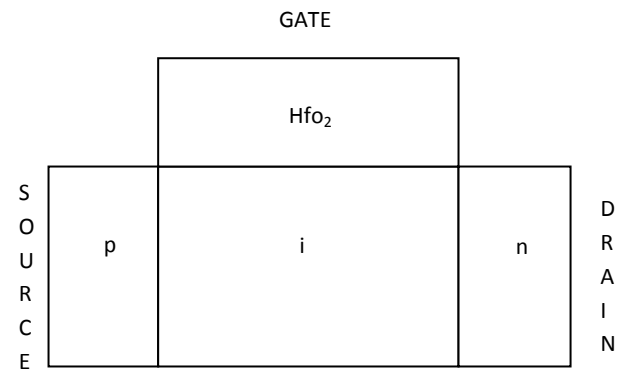


Figure 1: 2D structure of GAA TFET

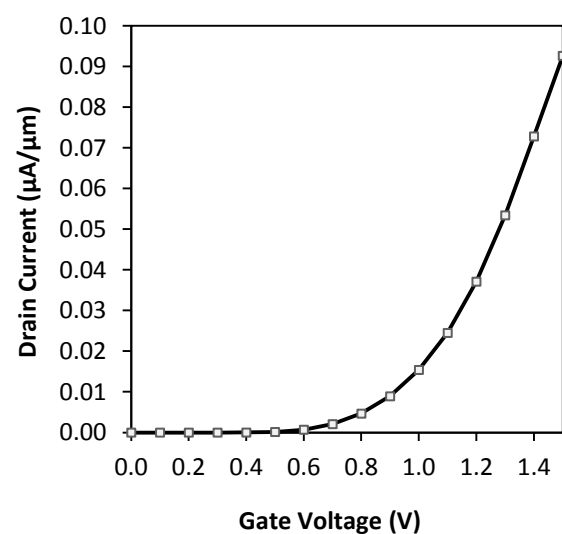


Figure 2: Drain current as a function of gate voltage

A non-local band to band tunnelling model with fermi-dirac statistics was used along with Shockley-Read-Hall recombination model for simulation [3].

Ac analysis was performed to extract the two port Y and Z parameters. The extracted Y-parameters were used to calculate f_t and f_{max} which help to understand the RF performance of GAA TFET. The extracted Z-parameters were used to calculate extrinsic parasitic resistances. The device simulation was performed using SILVACO ATLAS TCAD.

3. SMALL SIGNAL MODEL

The small signal equivalent circuit is shown in Fig.3. In the circuit, C_{gs} and C_{gd} are intrinsic gate to source and gate to drain capacitances. R_{gs} and R_{gd} are gate to source and gate to drain resistances that contribute to distributed channel resistance. C_{sdx} is source to drain capacitance which varies with larger drain bias on short channel devices [4].

The g_m and g_{ds} are transconductance and source-drain conductance respectively. $R_{gd}C_{gd}$, $R_{gs}C_{gs}$ and the time constant τ cause the time delay of the charges in the tunneling region. The effect of time constant can be formulated from the non-quasi static small signal model [5] shown in Figure.3.

The Y-parameters are extracted from the intrinsic non-quasi static small signal equivalent circuit after neglecting the extrinsic parameters and are expressed as follows:

$$Y_{11} = \frac{j\omega C_{gs} + \omega^2 R_{gs} C_{gs}^2}{1 + \omega^2 R_{gs}^2 C_{gs}^2} + \frac{j\omega C_{gd} + \omega^2 R_{gd} C_{gd}^2}{1 + \omega^2 R_{gd}^2 C_{gd}^2} \quad (1)$$

$$Y_{12} = \frac{-j\omega C_{gd} - \omega^2 R_{gd} C_{gd}^2}{1 + \omega^2 R_{gd}^2 C_{gd}^2} \quad (2)$$

$$Y_{21} = \frac{g_m - j\omega g_m \tau}{1 + \omega^2 \tau^2} - \frac{j\omega C_{gd} + \omega^2 R_{gd} C_{gd}^2}{1 + \omega^2 R_{gd}^2 C_{gd}^2} \quad (3)$$

$$Y_{22} = \frac{g_{ds} + j\omega g_{ds} R_{gd} C_{gd} + j\omega C_{gd}}{1 + j\omega R_{gd} C_{gd}} \quad (4)$$

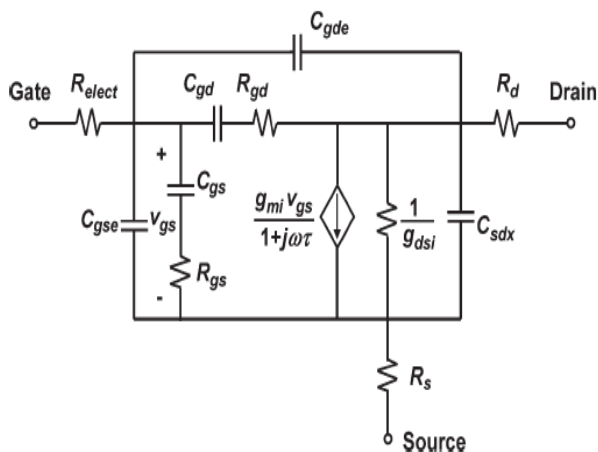


Figure 3: Non-quasi static small signal model (intrinsic and extrinsic part)

Using the real and imaginary parts of Y-parameters, the values of device parameters can be extracted as follows:

$$C_{gd} = -\frac{\text{Im}(Y_{12})}{\omega} \quad (5)$$

$$C_{gs} = \frac{\text{Im}(Y_{11}) + \text{Im}(Y_{12})}{\omega} \quad (6)$$

$$R_{gd} = -\frac{\text{Re}(Y_{12})}{\omega^2 C_{gd}^2} \quad (7)$$

$$R_{gs} = \frac{1}{C_{gs}^2} \left(\frac{\text{Re}(Y_{11})}{\omega^2} - R_{gd} C_{gd}^2 \right) \quad (8)$$

$$g_m = \text{Re}(Y_{21}) | \omega^2 = 0 \quad (9)$$

$$g_{ds} = \text{Re}(Y_{22}) | \omega^2 = 0 \quad (10)$$

$$\tau = -\frac{1}{g_m} \left(\frac{\text{Im}(Y_{21})}{\omega} + C_{gd} \right) \quad (11)$$

$$C_{sdx} = \frac{\text{Im}(Y_{22})}{\omega} - C_{gd} \quad (12)$$

Using equations (5)-(12), the intrinsic small signal parameters were calculated from Y-parameters. The above mentioned parameters were extracted at necessary bias conditions applied to the gate (V_{GS}) and drain (V_{DS}) terminals of the device.

In order to model the RF behavior over a wide range of frequency, it is necessary to calculate the intrinsic capacitances of the GAA TFET. The extracted values of C_{gs} and C_{gd} as a function of gate voltage (V_{GS}) at 1GHz are shown in Figure.4 and Figure.5 respectively. The C_{gd} is alone responsible for total gate capacitance (C_{gg}) as C_{gs} exponentially decreases as V_{GS} increases due to the presence of device potential barrier at the source side and C_{gd} increases with the increase in V_{GS} due to the reduction of potential barrier at the drain side.

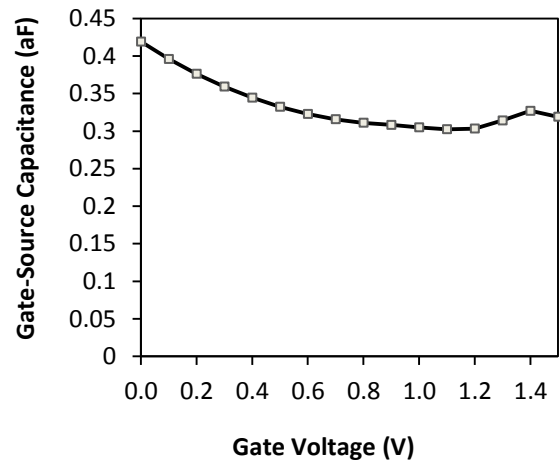


Figure 4: Gate-Source Capacitance as a function of V_{GS}

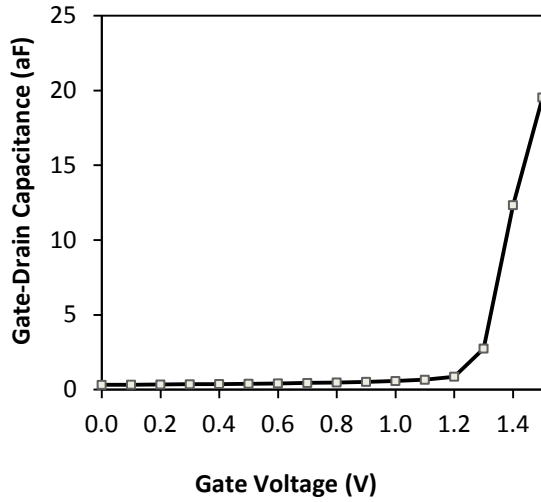


Figure 5: Gate-Drain Capacitance as a function of V_{GS}

The extrinsic parameters R_{ge} , R_{de} , R_{se} can be calculated using extracted Z-parameters from the device operated at $V_{GS}=V_{DS}=0V$. The expressions for the extrinsic parameters of the model [6] are as follows:

$$\text{Re}(Z_{11}) = r_g + r_s \quad (13)$$

$$\text{Re}(Z_{22}) = r_d + r_s \quad (14)$$

$$\text{Re}(Z_{12}) = \text{Re}(Z_{21}) = r_g \quad (15)$$

The parasitic resistances remain constant at higher frequencies. At low frequencies, the resistance values cannot be accurately determined. This is because the imaginary parts of the complex impedances are much larger than the real part.

4. RESULTS AND DISCUSSION

4.1 RF Performance of GAA TFET

The RF performance of GAA TFET is evaluated by extracting f_t , f_{max} , g_m and g_{ds} which are known as the Figures of Merit (FoM) [7]. It is necessary to observe the response of these FoM to understand the device behavior at high frequencies.

The f_t and f_{max} are the two parameters mainly responsible for estimating the high frequency performance of a RF device and can be defined as follows:

$$f_t = \frac{g_m}{2\pi C_{gg}} \quad (16)$$

$$f_{max} = \frac{f_t}{\sqrt{4R_g(g_{ds} + 2\pi f_t C_{gd})}} \quad (17)$$

Figure.6 (a-b) shows extracted f_t and f_{max} as a function of gate voltage. The f_t is extracted when current gain is unity and it is found to be 22GHz. From equation (16) it is observed that f_t increases as transconductance increases. The f_{max} is related to the capability of the device to provide power gain at large frequencies and is defined as the frequency at which the magnitude of the maximum available power gain, obtained

under power-matching conditions at both the input and output ports drops to unity [8].

In 2D device simulator, the ac solution is performed over wide frequency ranges to extract the Y-parameters. The extracted Y-parameters are shown in Figure.7 (a-d).

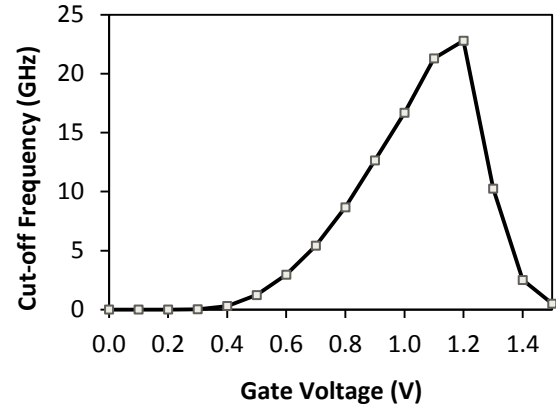


Figure 6(a): Cut-off frequency as a function of gate voltage

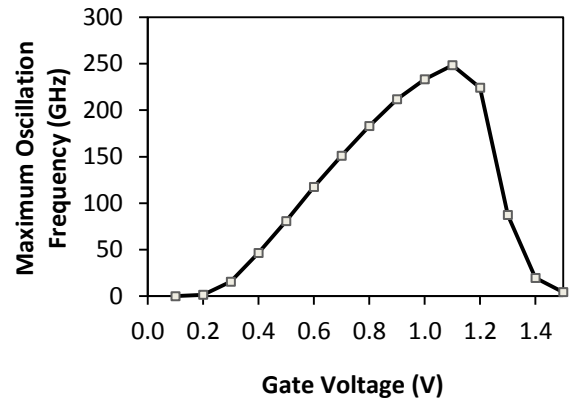


Figure 6(b): Maximum oscillation frequency as a function of gate voltage

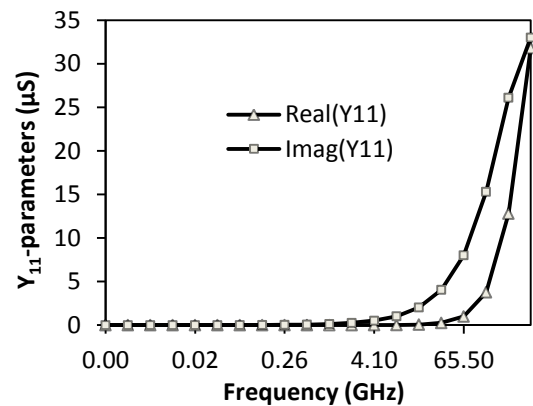
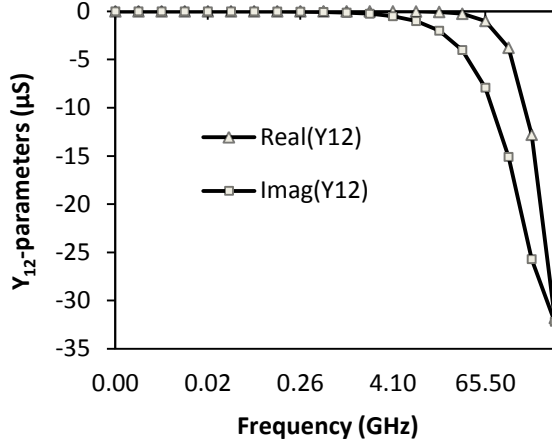
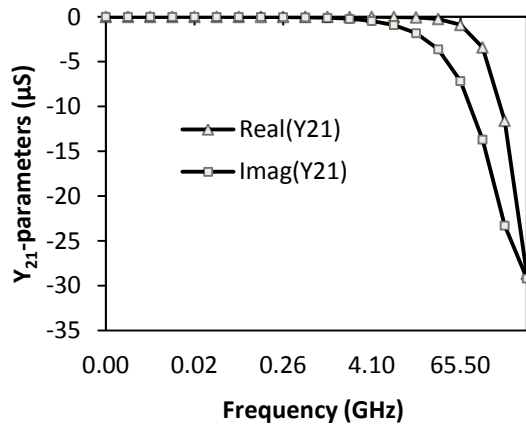
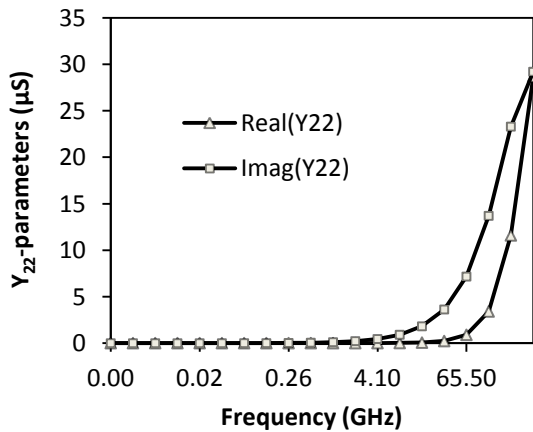
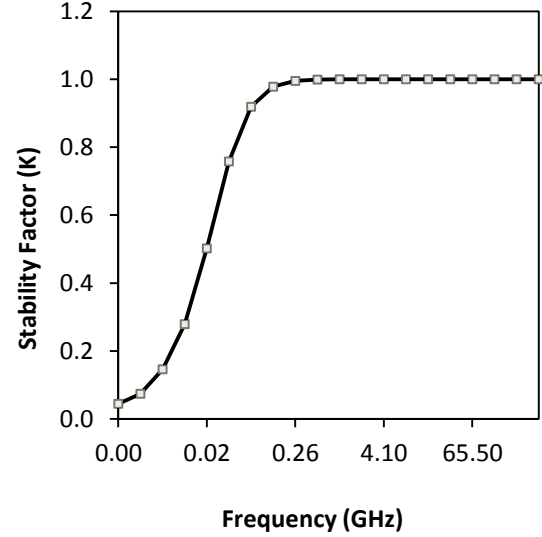


Figure 7(a): Y_{11} -parameters as a function of frequency

Figure 7(b): Y_{12} -parameters as a function of frequencyFigure 7(c): Y_{21} -parameters as a function of frequencyFigure 7(d): Y_{22} -parameters as a function of frequency

4.2 Stability Analysis of GAA TFET

Stability of a device is determined by its stability factor (K). This factor gives an indication whether the device is conditionally/unconditionally stable. It must satisfy the condition $K \geq 1$ for a device to be unconditionally stable [9]. Figure.8 shows the extracted stability factor curve as a function of frequency.

Figure 8: Stability factor (K) as a function of frequency

The stability factor in terms of Y-parameters [10] can be expressed as follows:

$$K = \frac{2\text{Re}(Y_{11})\text{Re}(Y_{22}) - \text{Re}(Y_{12} - Y_{21})}{|Y_{12} - Y_{21}|} \quad (18)$$

It is found that the device is unconditionally stable from 1GHz onwards. When the device is unconditionally stable over a wide frequency range, it indicates that additional stability circuits are not required for RF circuits which reduce the circuit complexity.

5. CONCLUSION

The design, stability and RF performance of GAA TFET is presented using TCAD simulation and the characteristics are studied. The intrinsic and extrinsic parameters are obtained through ac analysis. The cut-off frequency and the maximum oscillation frequency obtained estimate the high frequency performance of GAA TFET. It is evident from the results that GAA TFET shows good stability under RF range.

6. REFERENCES

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