Design of Efficient Low Power Stable 4-Bit Memory Cell

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ABSTRACT
Memory is the most common part in CMOS IC's applications. The power consumption and speed of SRAMs are important issue that has led to multiple designs with the purpose of minimizing the power consumption during both read and write operations. In this paper, a novel 9T static random access memory (SRAM) cell design which consumes less dynamic power and has high read stability is predicted. This paper also includes the SRAM array structure, it consist of sense amplifier and address decoders. The Tanner EDA tool is used for observe the schematic solution at different technologies. Based on the results obtained when compared with the existing methods, by utilizing the above proposed method it is clearly observed that there is a decrease in power consumption and stability improvement of the memory cells.

KEYWORDS
SRAM Cell, Read and Write, Stability, Stack effect, Array.

1. INTRODUCTION
A SRAM cell consist of a latch, therefore the cell data is kept as long as power is turned on and refresh operation is not required for the SRAM cell. SRAM is mainly used for the cache memory in microprocessors, mainframe computers, engineering workstations and memory in hand held devices due to high speed and low power consumption. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. High-performance on chip caches is a crucial component in the memory hierarchy of modern computing systems. In this technique each NMOS and PMOS transistor in the logic gates is split into two transistors are called Stack Technique [7]. Leakage current flowing through the NMOS transistor stack reduces due to the increase in the source to substrate voltage in the top NMOS transistor and also due to an enlarge in the drain to source voltage in the bottom NMOS transistor. The proposed SRAM memory cell consumes lower power during read and writes operations compared to 6T conventional circuit. The ability of the cell to write properly and to have sufficient read noise margin is very important for sub threshold region. Also, a new 9T SRAM combining the advantages of these circuits is proposed in the paper. A nine transistors (9T) SRAM cell configuration is proposed in this paper, which is amenable to small feature sizes encountered in the deep sub-micron/Nano CMOS ranges. Compared with the 8T and 10T cells of [1] and [2], the 9T scheme offers significant advantages in terms of power consumption. The conventional six transistor (6T) SRAM cell shows poor stability at very small feature size with low power supply. During the read operation, voltage division between the access and driver transistors causes the read stability to be very low. Hence in this paper, a 9T SRAM cell is proposed for high read stability and low power consumption. The proposed cell utilizes single bit-line (BL) for write operation, resulting in reduction of dynamic power consumption. During read operation, the data storage nodes are completely isolated from the bit lines, thus ornamental the read static noise margin.

Hence in this paper, a 9T SRAM cell is proposed for high read stability and low power consumption [5]. The proposed cell utilizes single bit-line (BL) for write operation, resulting in reduction of dynamic power consumption. During read operation, the data completely isolated from the bit line, thus enhancing the read static noise margin.

2. DIFFERENT SRAM CELLS

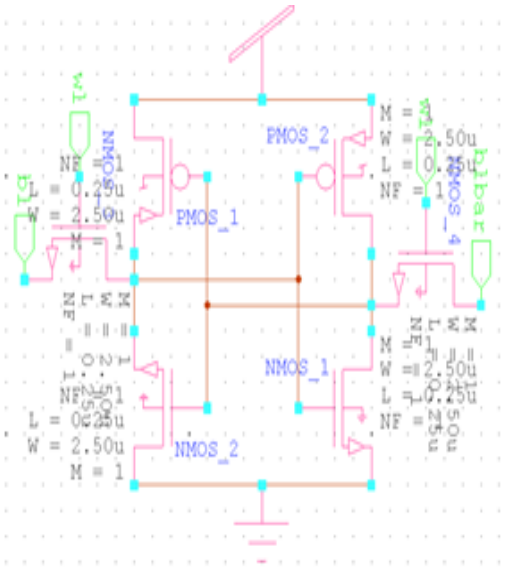

Fig1: conventional 6T SRAM cell

Figure.1 shows the conventional 6T SRAM cell with transistor sizing in 125 nm CMOS technology. Access to the cell is enabled by the word line (WL) which controls the two access transistors, in turn, control whether the cell should be connected to the bit lines: BL and BLB. They are used to transfer data for both read and write operations. While it's not strictly essential to have two bit lines, both the signal and its inverse are typically provided since it improves noise margins [11].

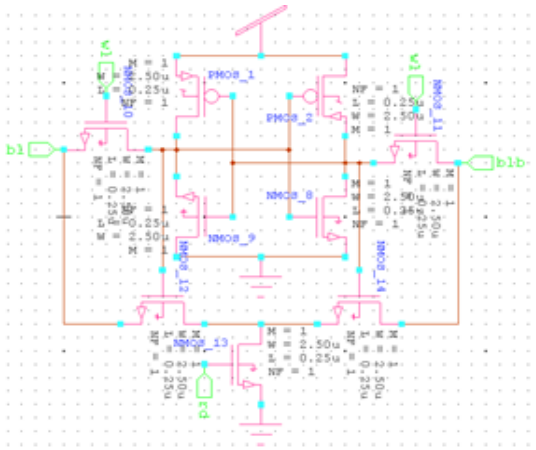

Fig 2: schematic 9T SRAM cell

Schematic of 9T SRAM cell is shown in the Fig. 2. This circuit shows reduced leakage power and enhanced data stability. The 9T SRAM cell completely isolates the data from the bit lines during a read operation. The idle 9T SRAM cells are placed into a super cutoff sleep mode, thereby reducing the leakage power consumption as compared to the standard 6T SRAM cells.

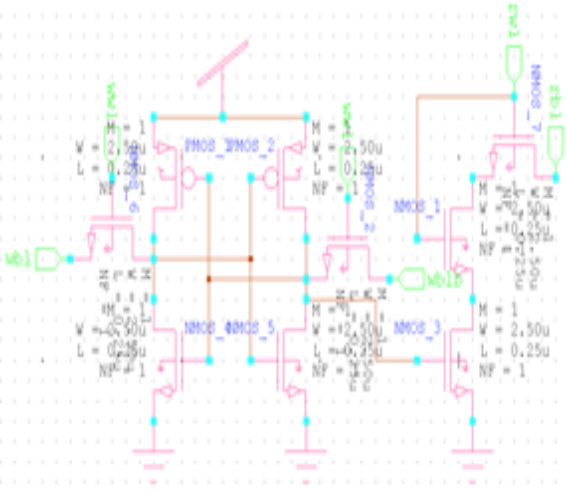

Fig 3: bit line scheme

The optimal transistor sizing for this 9T SRAM cell considering stability, energy consumption and delay. A write bit line balancing scheme is proposed to reduce the leakage current of the SRAM cell. A 9T structure is to improve the SNM by separating the read access structures of the original 6T cell, thus making the read SNM equal to the hold SNM. An innovative precharging and bit line balancing scheme for writing operation of the 9T SRAM cell is also proposed for extreme standby power savings in an SRAM array.

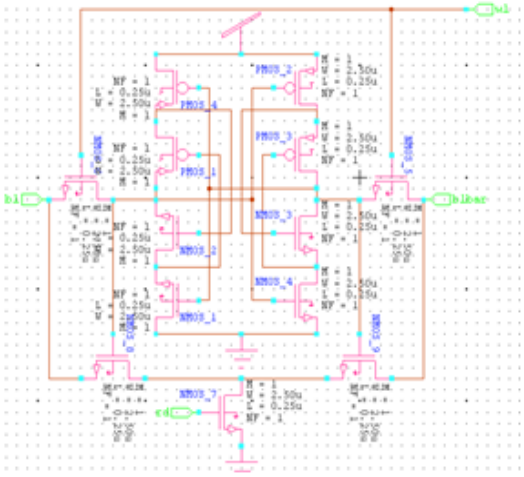

Fig 4: stack technique

Power consumption has become a critical design concern for many VLSI systems [12]. Leakage current flowing through the NMOS transistor stack reduces due to the increase in the source to substrate voltage in the top NMOS transistor and also due to an increase in the drain to source voltage in the bottom NMOS transistor. This reduces the power dissipation in logic circuits. In this technique each NMOS and PMOS transistors in the logic gates are split into two transistors. A state with more than one transistor is off condition from a path from supply voltage to ground path consist of less leakage equated to the only one transistor off condition from a path from supply voltage to ground path.

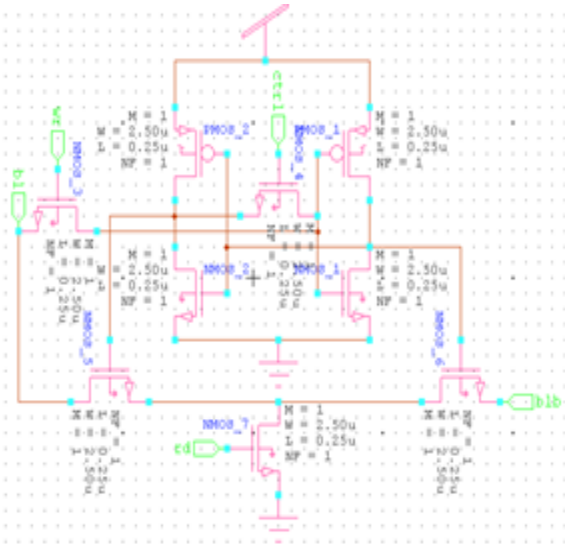

Fig 5: improve read stability

The data in a conventional 6T SRAM cell as shown in figure.1, is most vulnerable to external noise due to the direct access of the data storage nodes by the access transistors (N3 and N4) connected to bit line (BL) and bit line bar (BLB) respectively[9]. During read operation, the voltage division between the access transistors and cross coupled inverters °fluctuate the storage node voltage, resulting in destructive read operation. The 9T SRAM cell in figure has an improved static noise margin (SNM) as compared to conventional 6T SRAM cell. The upper sub-circuit of the memory cell is essentially a 6T SRAM cell (composed of N1, N2, N3, N4, P1, and P2). The two write access transistors (N3 and N4) are controlled by a write signal (WR). The data is stored within this upper memory sub-circuit. The lower sub-circuit of the new cell is composed of the bit-line access transistors (N5 and N6) and the read access transistor (N7).

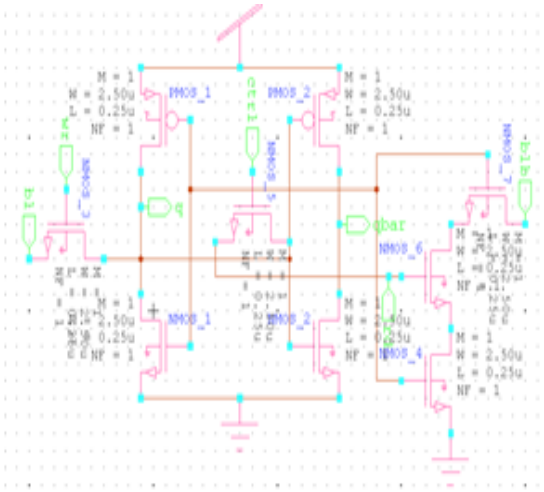

Fig 6: proposed design

Here only one single bit line capacitance (BL) will be charged and discharged during write operation which results in important reduction in dynamic power consumption and at the equal time the data stability of the 9T SRAM cell as in is also maintained. The planned cell maintains greatly improved write margins and functionality, even when the PMOS are much stronger than the NMOS ones. This cell completes full functionality deep into the sub-threshold section without the need for special peripheral circuits and techniques that necessitate additional power, die area and timing schemes [6]. In addition, this circuit presents a low-leakage state, at which its static power is lower than any of the other enactments when operated at a similar supply voltage [3]. This is accomplished lacking any performance degradation, while keeping a reasonable SNM.

3. PROPOSED SRAM ARRAY

3.1 Sense Amplifier

The sense amplifiers have to amplify the data which is present on the bit lines during the read operation. The memory cells are weak due to their small size, and hence cannot the discharge the bit lines fast enough. Also, the bit lines continue to slew till a large differential voltage is formed between them. This causes significant power dissipation since the bit lines have large capacitances. It consists of two cross coupled gain stages which are enabled by the sense clock signal. The cross coupled stage ensures a full amplification of the input signal. This type of amplifier consumes least amount of power. If the sense amplifiers enabled before sufficient differential voltage is formed, it could lead to a wrong output. Thus, the timing of the sense clock signal needs to be such that the sense amplifier can operate over various process corners and temperature ranges.

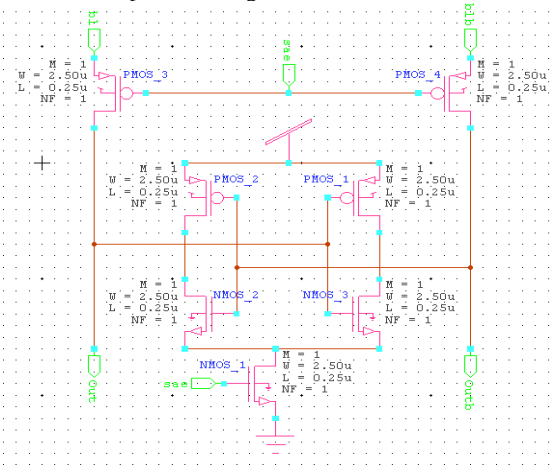

Fig 7: sense amplifier

3.2 DECODER DESIGN

Usually the memory address decoder is divided into two parts, row decoder and column decoder. If the address bits of the memory are m bits, there are m1 bits for the row decoder and m2 bits for the column decoder (m1+m2=m).

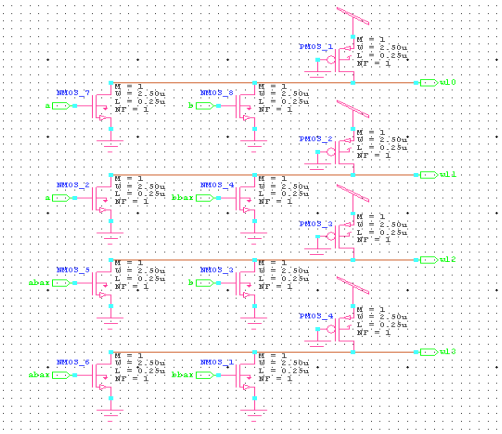

Fig 8: decoder design

3.3 SRAM ARRAY STRUCTURE

The row decoder and column decoder are used to select the particular cell onto which the data is to be written or from which the data is to be read. In our simulation, we designed 4X4 array. The schematic of the SRAM array is as shown below.

Fig 9: 4*4 SRAM array

4. SIMULATION AND ANALYSIS

4.1 Simulation Result

All the circuits have been simulated using BSIM 3V3 125nm, 45nm and 180nm technology on Tanner EDA tool with supply voltage ranging. The maximum operating frequency of the SRAM cell is 165 MHZ.

Table 1. Power comparison at 45nm tech

Different SRAM cells	POWER CONSUMPTION IN WATTS				
	VDD=1V	VDD=2V	VDD=3V	VDD=4V	VDD=5V
6T SRAM	6.2E-6	4.6E-5	1.2E-4	3.4E-4	3.3E-3
Bit Line Scheme	8.3E-6	7.6E-5	3.8E-4	4.8E-4	3.6E-3
Improve Read Stability	9.2E-6	2.1E-5	7.6E-4	6.1E-4	4.5E-3
Proposed Design	1.1E-7	6.8E-6	9.7E-6	7.3E-5	5.9E-4

Table 2. Power comparison at 250nm tech

Different SRAM Cells	Power Consumption in watts				
	VDD (1V)	VDD (2V)	VDD (3V)	VDD (4V)	VDD (5V)
6T SRAM	7.2E-4	1.1E-3	8.8E-4	2.2E-5	1.0E-5
Bit Line Scheme	6.6E-4	1.5E-3	8.2E-5	2.7E-5	1.2E-5
Improve Read Stability	6.4E-10	2.9E-10	8.9E-9	2.2E-9	1.4E-8
Proposed 9t Design	2.3E-11	8.7E-11	2.2E-10	5.1E-10	1.1E-9

Table 3. Power comparison at 180nm tech

Different SRAM cells	POWER CONSUMPTION IN WATTS				
	VDD=1V	VDD=2V	VDD=3V	VDD=4V	VDD=5V
6T SRAM	1.2E-11	4.6E-10	6.2E-10	2.4E-9	2.6E-9
Bit Line Scheme	2.3E-11	7.6E-11	9.7E-11	1.8E-10	1.6E-9
Improve Read Stability	1.2E-12	2.1E-11	4.6E-12	6.1E-12	4.5E-11
Proposed Design	1.1E-14	6.8E-14	9.7E-13	7.3E-13	5.9E-12

Table 4. Power comparison at different V_{th}

Different SRAM cells	POWER CONSUMPTION IN WATTS									
	VDD=1V		VDD=2V		VDD=3V		VDD=4V		VDD=5V	
	Vth(0.2)	Vth(0.4)	Vth(0.2)	Vth(0.4)	Vth(0.2)	Vth(0.4)	Vth(0.2)	Vth(0.4)	Vth(0.2)	Vth(0.4)
6T SRAM	6.7E-05	6.1E-06	1.0E-05	9.2E-04	6.9E-04	5.2E-04	1.4E-07	6.8E-08	5.2E-09	5.1E-09
Bit Line Scheme	7.7E-07	6.1E-10	3.3E-08	9.0E-09	1.6E-07	5.6E-08	4.1E-06	6.8E-09	7.7E-05	5.2E-08
Improve Read Stability	1.4E-11	1.1E-11	1.1E-11	1.2E-11	3.3E-90	3.4E-09	6.4E-09	1.0E-09	2.4E-09	4.3E-09
Proposed Design	1.5E-12	5.3E-11	5.3E-11	5.6E-11	1.3E-10	1.2E-10	2.6E-10	2.9E-10	5.6E-10	5.4E-10

Table 5. Power comparison at different nm tech

Different nm Tech	POWER CONSUMPTION IN WATTS				
	VDD=2V	VDD=3V	VDD=4V	VDD=4.5V	VDD=5V
Proposed SRAM at 250nm tech	8.6E-03	3.6E-02	8.6E-02	101E-01	5.1E-01
Proposed SRAM at 180nm tech	7.7E-03	2.2E-02	4.9E-02	6.4E-02	1.4E-01
Proposed SRAM at 45nm tech	5.2E-05	2.1E-04	4.6E-04	6.1E-04	4.5E-03

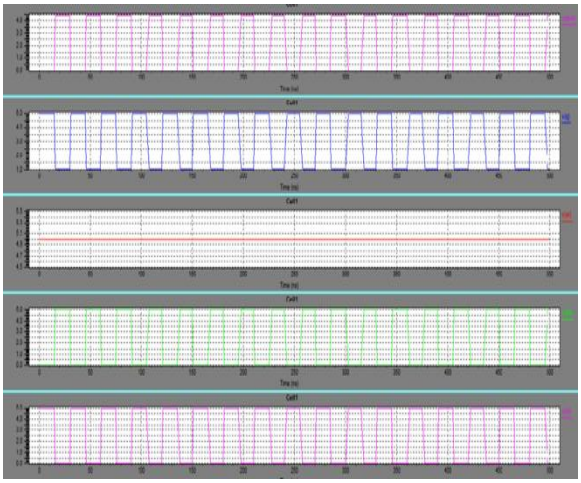

Fig 10: waveform for write operation of 9T SRAM

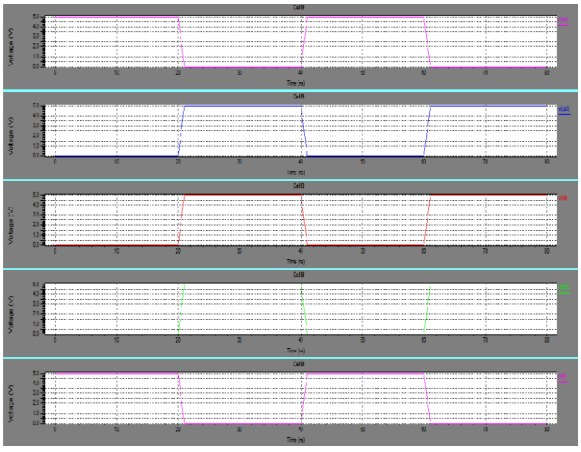

Fig 11: waveform for read operation of 9T SRAM

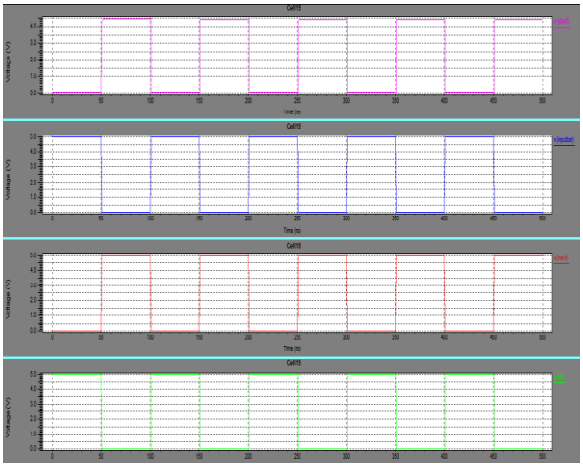

Fig 12: waveform for write operation of SRAM array

5. CONCLUSION

A Novel 9T SRAM cell is accessible in this paper for high read stability and low energetic power consumption. For low leakage and high speed circuits concern should be on both the factors speed and power. During the write operation, the SRAM cell utilizes the charging/discharging of only one bit line (BL), resulting in reduction of dynamic power consumption as compared to conventional 6T SRAM cell. Different techniques have been analyzed to reduce the standby leakage current and dynamic power dissipation of the SRAM cell. In the proposed method 45nm and 250nm and 180nm technologies are analyzed using the Tanner EDA software and is used to analyze parameters such as power consumption, delay time and operating frequency. This paper presents the design of SRAM array in 45 nm having very low power consumption. Based on the results obtained when compared with the existing methods, by utilizing the above proposed method it is clearly observed that there is a decrease in power consumption and stability improvement of the memory cells.

6. REFERENCES

[1] S. Borkar, T. Karnik, S. Narendra, J.T schanz, A. Keshavarzi, and V.de, \Parameter Variations and Impact on Circuits & Micro architecture," *Proceedings of Design Automation Conference.*, pp. 338-342, Jun.2003.

[2] A.J. Bhavnagarwala, X. Tang, and J. Meindl,\The simpact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability," *IEEE Journal of Solid State Circuits*, vol. 36, No. 4, pp. 658-665,April 2001.

[3] S. Mukhopadhyay, H. Mahmoodi, and K. Roy,\Modeling and estimation of failure probability due to parameter variations in nano-scale SRAMs for yield enhancement," *In VLSI circuit Symposium*, 2004.

[4] K. Agarwal, and S. Nassif, \Statistical analysis of SRAM stability," *Proceedings of 43rd Annual Conference on Design Automation*,pp. 57, 2006.

[5] E. Seevinck, F.J. List, and J. Lohstroh, \Static Noise Margin Analysis of MOS SRAM cells, "*IEEE Journal of Solid State Circuits*, vol.22, No.5, pp. 748-754, Oct. 1987.

[6] J. Lohstroh, E. Seevinck, and J.de Groot, \Worst-case static noise margin criteria for logic circuits and their mathematical equivalence, "*IEEE Journal of Solid State Circuits*, vol.SC-18,No.6, pp. 803-807, Dec. 1983.

[7] L. Chang, R.K. Montoye, Y, Nakamura, K.A. Batson, R.J. Eickemeyer, R.H. Dennard, W.Haensch, and D. Jamsek, \An 8T SRAM for Variability Tolerance and Low-Voltage Operation in High-Performance Caches," *IEEE Journal of Solid State Circuits*, vol. 43, No. 4,pp. 956-963, April 2008.

[8] S. Lin, Y.B. Kim, and F. Lombardi, \A Highly Stable Nanometer Memory for Low-Power Design," *Proceeding of IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems*, pp. 17-20, 2008.

[9] Z. Liu, and V. Kursun, \Characterization of a Novel Nine-Transistor SRAM Cell," *IEEETransactions on Very Large Scale Integration (VLSI) Systems*, vol. 16, No. 4, pp. 488-492,April 2008.

[10] K. Agarwal, and S. Nassif, \The Impact of Random Device Variations on SRAM Cell stability in Sub-90-nm CMOS Technologies," *IEEE Transactions on Very Large Scale Integration (VLSI)Systems*, vol.16, No. 1, pp. 86-97, Jan 2008.

[11] Neil H.E.Weste, Kamran Eshraghian, *Principles of CMOS VLSI Design*, Pearson Education, Inc.,Singapore, 2002.[12] Sung-Mo Kang, Yusuf Leblebici, *CMOS Digital Integrated Circuits*, McGraw-Hill Companies,Inc., New York, 2003.

[12] Dake Liu, and Christer Svenson, Power Consumption Estimation in CMOS VLSI Chips, "*IEEE Journal of Solid State Circuits*, vol. 29,No. 6, pp. 663-670, June 1994.