Power and Delay Analysis on Double-Tail Comparator using Nano Scale CMOS Technology

Aiswarya.J
P G Scholar, ECE
Sri Krishna College of Technology
Coimbatore, India.

R. Udaiya Kumar
H.O.D, ECE
Sri Krishna College of Technology
Coimbatore, India.

ABSTRACT
Dynamic comparators are used in high speed analog to digital converters. In this paper low voltage, low power dynamic comparators are designed in 130 nm technology and the analysis of the power consumption and delay will be presented. Based on the presented analysis, a new dynamic comparator is proposed. By using power gating technique and adding few transistors, the positive feedback during the regeneration is strengthened in the proposed comparator structure. Post layout simulation results in 0.130μm CMOS technology confirm the analysis results. In the proposed comparator the power consumption is significantly reduced.

General Terms
Low- power VLSI

Keywords
Double-tail comparator, dynamic clocked comparator, high-speed analog-to-digital converters (ADCs), Low-power analog design

1. INTRODUCTION
Comparator is one of the building blocks in most of analog-to-digital converters without which conversion of data cannot take place. In general comparators are "fast". The circuits of comparators are not immune to speed power trade off. High speed comparators such as flash ADC's use transistors with large aspect ratios and hence also consume more power. So depending on the application a comparator with either high speed or low power should be selected. Nano scale comparators are ideal for portable and ultra-low-power applications. Lower power and Good accuracy can be obtained by using a clocked comparator structure. This clocked comparator structure, when the clock is high, uses strong positive feedback for a "Regenerator phase" and enters into a "Reset phase" when the clock is low.

High speed comparators in ultra deep submicrometer CMOS technologies suffer from low supply voltages [2]. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. Many techniques, such as supply boosting methods [3], [4] techniques employing body-driven transistors [5], [6], current-mode design [7] and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. Additional nMOS switches are used to overcome the static power consumption [1].

In this paper, a comprehensive analysis on delay, power consumption and area of the dynamic comparator with different architecture will be presented. Based on the double-tail structure of 180 nm, proposed comparator is designed which does not require stacking of too many transistors. By using power gating technique and by adding few minimum-size transistors to the conventional double tail comparator, latch delay and power consumption is reduced when compared to the conventional dynamic and double-tail comparator.

2. CLOCKED REGENERATIVE COMPARATORS
Clocked regenerative comparators can make fast decisions since they use strong positive feedback in the regenerative latch and so that they can be used in high speed ADCs. Many papers have been presented based on the performance of these comparators from different aspects, such as kick-back noise [12], random decision errors [11], and noise [7], offset [8], [9] and [10]. In this section four comparator architectures are to be analysed.

2.1 Conventional Dynamic Comparator
The schematic circuit diagram of the conventional dynamic comparator with high input impedance, rail-to-rail output swing, and no static power consumption is shown in the Fig.1.

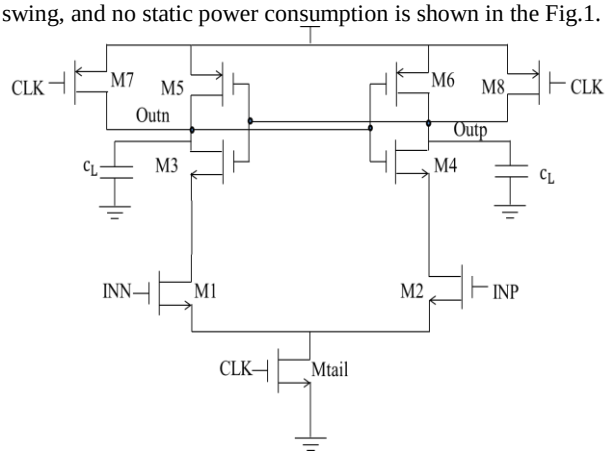


Fig 1.Schematic diagram of the conventional dynamic comparator

The comparator operation is given below. During the reset phase when CLK =0, M_{tail} goes to off state, reset transistors ($M_7 - M_8$) pull both output nodes Outn and Outp to V_{DD} to define a start condition and to have a valid logic level during reset. In the comparison phase when CLK=V_{DD}, transistors M_7 and M_8 are off, and M_{tail} is in on condition. Output voltages (Outp and Outn), which had been pre-charged to V_{DD}, start to discharge with different discharging rates depending on the corresponding input voltage

(INN/INP).Assume $V_{INP} > V_{INN}$, Outp discharges faster than Outn, hence when Outp falls down to V_{DD} - $|V_{thp}|$ before Outn, the corresponding pMOS transistor (M_5) will turn on initiating the latch regeneration caused by back to back inverters. Thus Outn pulls to V_{DD} and Outp discharges to ground. If $V_{INP} < V_{INN}$, the circuit works vice versa. The delay of this comparator consists of two delays, t_0 and t_{latch}. The delay t_0 is the capacitive discharge of the load capacitance until the first p-channel transistor (M_5/M_6) turns on. In case, the voltage at node INP is bigger than INN (i.e., $V_{INP} > V_{INN}$), the drain current of the transistor M_2 causes faster discharge of Outp node compared to the Outn node, which is driven by M_1 with smaller current. In [13], it has been shown that an input common-mode voltage of 70% of the supply voltage is optimal regarding speed and yield.

This structure has the advantage of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch [2]. Due to the fact that parasitic capacitance of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage is the fact that due to several stacked transistors, a sufficiently high supply voltage is need for a proper delay time. Another drawback of this structure is that there is only one current path, via tail transistorM_{tail}, which defines the current for both the differential amplifier and the latch. While one would like a small tail current to keep the differential pair in week inversion and obtain a long integration interval and a better G_m/I ratio, a large tail current would be desirable to enable fast regeneration in the latch. Besides, as far as M_{tail} operates mostly in triode region, the tail current depends on the input common-mode voltage, which is not favorable for regeneration. This structure has the power consumption of 6.76 µW and overall circuit delay of 51 ns.

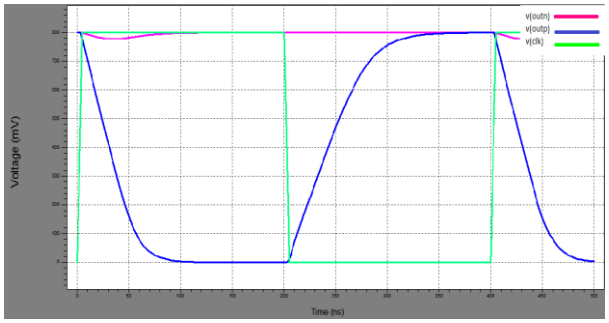


Fig.2. Transient simulations of the conventional dynamic comparator for input voltage difference of 5 mV

2.2. Conventional Double- Tail Dynamic Comparator

The schematic of conventional double tail comparator is shown in the fig (3). This structure has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator.

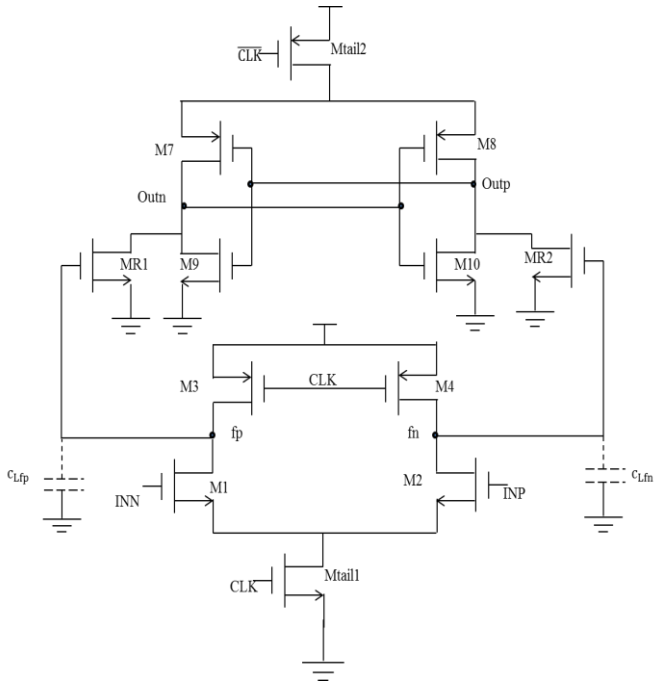


Fig.3. Schematic diagram of the conventional double-tail dynamic comparator

The operation of this comparator is given below. During reset phase (CLK=0, M_{tail1} *and* M_{tail2} turn off), transistors $M_3 - M_4$ pre-charge nodes fn and fp to V_{DD}, which in turn causes transistors M_{R1} and M_{R2} to discharge the output nodes to ground.

During the decision making phase (CLK=V_{DD}, M_{tail1} *and* M_{tail2} are turn on), $M_3 - M_4$ are turn off and the voltages at the node fn and fp start to drop with the rate defined by $I_{Mtail}/C_{fn(p)}$ and on top of this an input dependent differential voltage $\Delta V_{fn(p)}$ will build up. The intermediate stage formed by M_{R1} and M_{R2} passes $\Delta V_{fn(p)}$ to the cross coupled inverters and also provides a good shielding input and output.

2.2.1. Power and Delay Analysis

In this comparator, both intermediate stage transistors are finally cut-off, hence they do not play any role in improving the effective transconductance of the latch. Besides during reset phase, these nodes have to be charged from ground to V_{DD}, which means power consumption. This comparator consumes 13 µW. The overall circuit delay is 7.79 ns. Therefore delay is reduced when compared to the previous structure since speed of operation is increased in this structure with the intermediate transistors (MR1 and MR2). The following section demonstrates how the existing comparator improves the performance of the double-tail comparator.

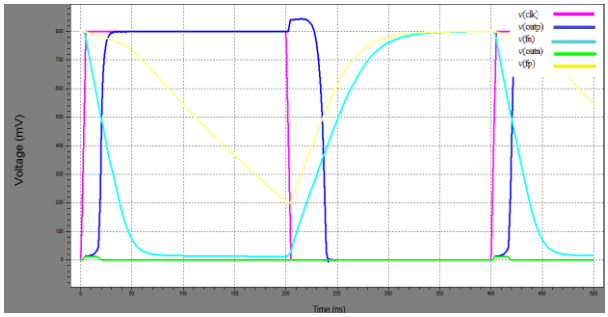
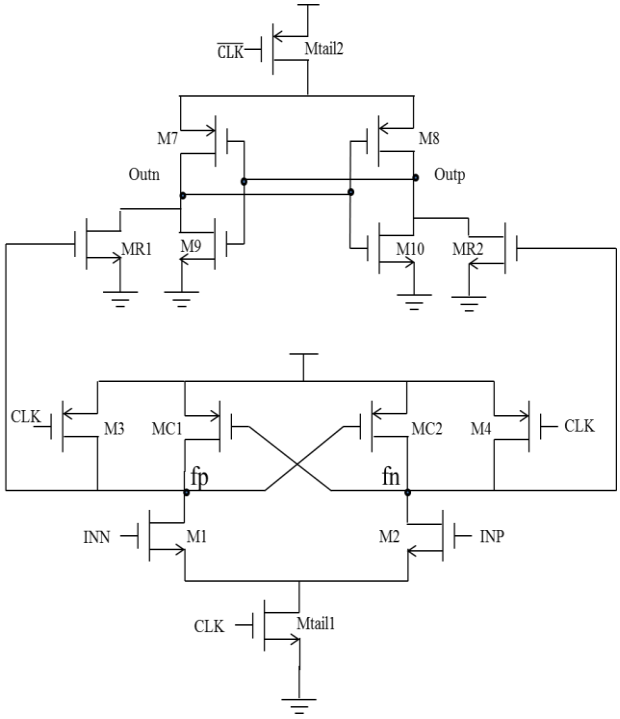


Fig.4. Transient simulations of the conventional double tail dynamic comparator for input voltage difference of 5 mv

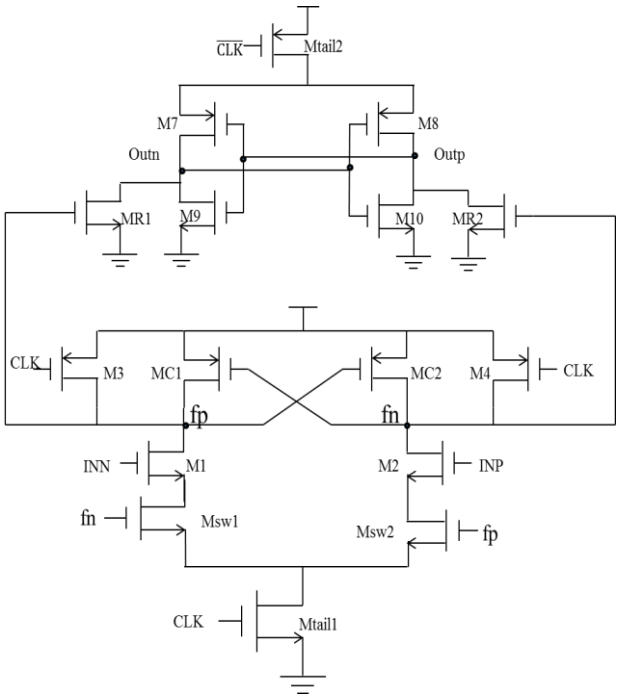
2.3. Existing Double- Tail Dynamic Comparator

Fig.5. (a) is the schematic diagram of the proposed double tail comparator. The proposed comparator is designed based on the double tail architecture due to its better performance in the low voltage applications.



(a)

The idea of this comparator is to increase $\Delta V_{fn/fp}$ in order to increase the latch regeneration speed. For this purpose, M_{c1} and M_{c2} are the two control transistors that have been added to the first stage in parallel to M_3/M_4 transistors but in a cross-coupled manner.



(b)

Fig.5. Schematic diagram of the existing dynamic comparator (a) With static power consumption. (b) Without static power consumption

The operation of proposed comparator is as follow. During reset phase (CLK= 0, $M_{tai\,1l}$ and $M_{tail\,2}$ are off), M_3 and M_4 pulls both fn and fp nodes to V_{DD}, hence transistor M_{c1} and M_{c2} are cut off. Intermediate stage transistorsM_{R1} and M_{R2}, reset both latch outputs to ground.

During the decisions making phase (CLK= V_{DD}, $M_{tai\,1l}$ and $M_{tail\,2}$ turn on), transistors M_3 and M_4 are in off state. At the beginning of this phase both the control transistors are still off (since fn and fp are about V_{DD}). Nodes fn and fp starts to drop at different rates according to the input voltages. Suppose $V_{INP} > V_{INN}$, thus fn drops faster than fp, (since M_2 provides more current than M_1). As long as fn continues falling, the corresponding pMOS control transistor M_{c1} starts to turn on, pulling node fp back to theV_{DD}; so another control transistor (M_{c2}) remains off, therefore allowing fn to be discharged completely.

In this structure as soon as the comparator detects for instance node fn discharges faster, a pMOS transistor turns on, pulling the node fp back toV_{DD}.Therefore by the time passing, the difference in fn and fp increases in exponential manner leading to the reduction of latch regeneration time.

When one of the control transistors (e.g., M_{c1}) gets turned on, a current from V_{DD} is drawn to the ground through input and tail transistor (e.g., M_{c1} ,M_1 , and $M_{tai\,1l}$), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistor [$M_{sw\,1}$ and $M_{sw\,2}$] as shown in fig.5.(b).

2.3.1 Power and Delay Analysis

In this structure the power consumption is reduced. The reason is that in conventional double–tail topology, both fn and fp nodes discharge to the ground during the decision making phase and each time during the reset phase they should be pulled up back to theV_{DD}. But, in our proposed comparator, only one of the mentioned nodes (fn/fp) has to be charged during the reset phase. This is due to the fact that during the previous decision making phase, depending on the status of control transistors, one of the nodes had not been discharged and thus less power is required. This can be seen when being compared with conventional topologies. This comparator consumes 9.73 µW. The overall delay of this comparator structure is 7.67 ns. The delay of this structure is reduced due to the effect of two control transistors.

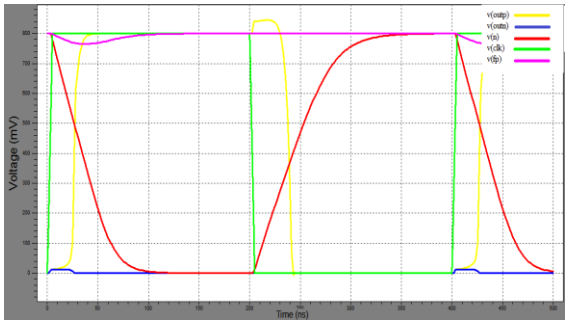


Fig. 6. Schematic diagram of the existing double-tail dynamic comparator

2.4 Proposed Dynamic Double Tail Comparator

The schematic diagram of the proposed dynamic double tail comparator is shown in the Fig. 7.with two nMOS switches (Mn1 and Mn2) added to the switching transistors (Msw1 and Msw2) in order to reduce the static power consumption. This circuit works similar to the previous comparator structure.

This circuit uses the power gating technique to reduce the static power consumption. The additional transistors switches when it has high input voltage otherwise it remains in the off state and reduces power consumption by grounding the static power consumed. In addition to reducing the stand-by power, power gating has the merit of enabling iddq testing.

2.4.1. Power and Delay Analysis

This circuit has reduced power consumption when compared to the existing comparator structure. Its power consumption is 7.40 µW. The overall delay of this circuit increases because the switching transistors Mn1 and Mn2 is added to Msw1 and Msw2 respectively.

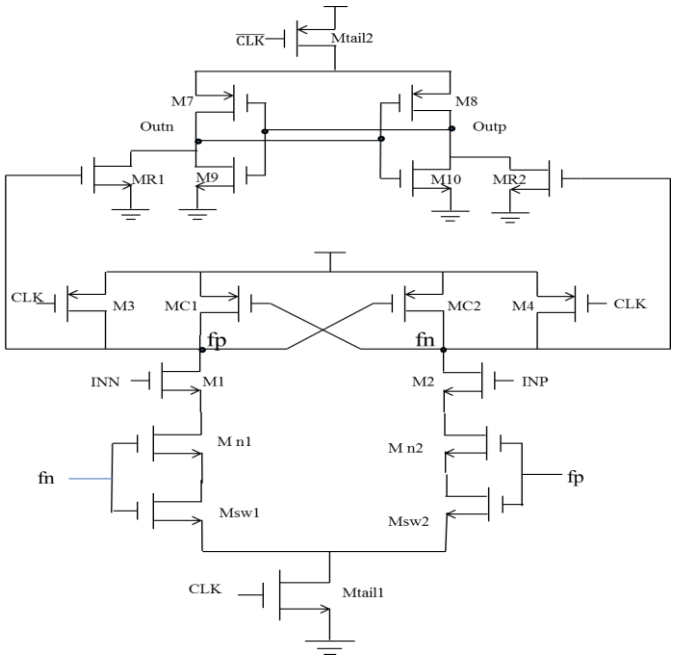


Fig.7. Schematic diagram of the proposed double tail dynamic comparator

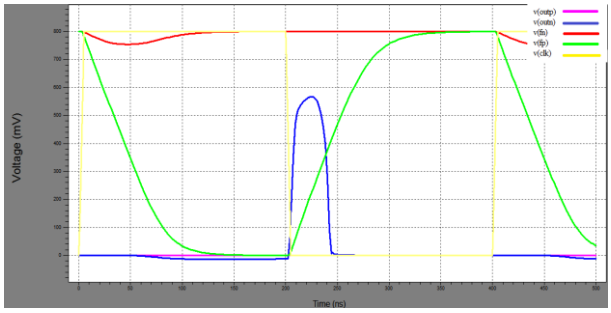


Fig.8. Transient simulations of the conventional double tail dynamic comparator for input voltage difference of 5 mV.

3. SIMULATION RESULTS

In order to compare the modified comparator with the existing , conventional and double-tail dynamic comparators, all circuits have been simulated in a 130 nm CMOS technology with V_{DD} = 0.8 V using t-spice. The output waveform of dynamic, conventional double tail, existing and proposed comparator is shown in the fig. (2), (4), (8) and (6) respectively. From the analysis it is known that the proposed comparator consumed less power. The power consumption has been reduced significantly in the modified comparator. The delay of this comparator is increased in 130 nm technology.

Fig .9 shows the layout of the proposed dynamic structure using micro wind tool. It is of 55 × 16 µm in dimensions.

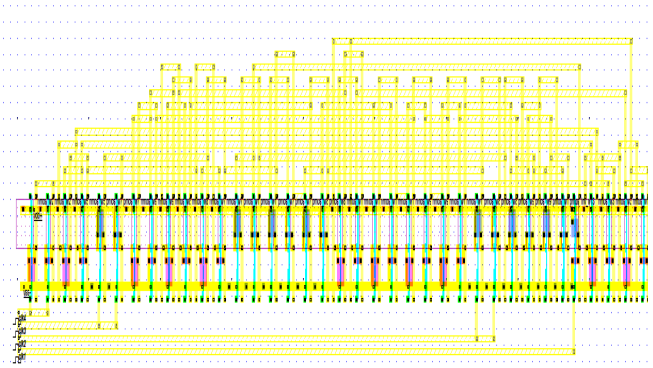


Fig.9 layout schematic diagram of the proposed dynamic double tail comparator

Table 1.Power Comparison

S. No	Comparator type	Power consumed in µW
1	Conventional double tail comparator	13
2	Existing double tail dynamic comparator	9.7
3	Proposed double tail dynamic comparator	7.4

4. CONCLUSION

In this paper, two common structures of conventional dynamic comparator and conventional double tail comparators were designed and analyzed in 130 nm. Based on the analysis, a new dynamic double comparator with low-voltage low-power capability is proposed in order to reduce the static power consumption by adding two switching transistors. Post layout simulation results in 0.13-µm CMOS technology confirmed that the power consumption of the proposed comparator is reduced to a great extent. This circuit can be used in analog to digital converter structures. With the help of this circuit applications such as sense amplifier, operational transconductance amplifier and pre-defined amplifier can be built.

5. REFERENCES

[1] Samanesh Babayan and Reza Lotfi, "Analysis and design oflow-voltage low-power double-tail comparator,"IEEE transcations on very large scale integration systems, 2013

[2] B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 11, pp. 810–814, Nov. 2009.

[3] S. U. Ay, "A sub-1 volt 10-bit supply boosted SAR ADC design in standard CMOS," Int. J. Analog Integr. Circuits Signal Process., vol. 66,no. 2, pp. 213–221, Feb. 2011.

[4] A. Mesgarani, M. N. Alam, F. Z. Nelson, and S. U. Ay, "Supply boosting technique for designing very low-voltage mixed-signal circuits in standard CMOS," in Proc. IEEE Int. Midwest Symp. Circuits Syst. *Dig Tech. Papers*, Aug. 2010, pp. 893–896.

[5] B. J. Blalock, "Body-driving as a Low-Voltage Analog Design Technique for CMOS technology," in Proc. IEEE Southwest Symp. Mixed-Signal *Design*, Feb. 2000, pp. 113–118.

[6] M. Maymandi-Nejad and M. Sachdev, "1-bit quantiser with rail to rail input range for sub-1V __ modulators," *IEEE Electron. Lett.*, vol. 39, no. 12, pp. 894–895, Jan. 2003.

[7] P. Nuzzo, F. D. Bernardinis, P. Terreni, and G. Van der Plas, "Noise analysis of regenerative comparators for reconfigurable ADC architectures," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 6, pp. 1441–1454, Jul. 2008.

[8] A. Nikoozadeh and B. Murmann, "An analysis of latched comapratoroffset due to load capacitor mismatch," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 12, pp. 1398–1402, Dec. 2006.

[9] S. Babayan-Mashhadi and R. Lotfi, "An offset cancellation technique for comparators using body-voltage trimming," *Int. J. Analog Integr. Circuits Signal Process.*, vol. 73, no. 3, pp. 673–682, Dec. 2012.] 2009

[10] J. He, S. Zhan, D. Chen, and R. J. Geiger, "Analyses of static and dynamic random offset voltages in dynamic comparators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 5, pp. 911–919, May 2009.

[11] J. Kim, B. S. Leibowits, J. Ren, and C. J. Madden, "Simulation and analysis of random decision errors in clocked comparators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 8, pp. 1844–1857, Aug. 2009

[12] P. M. Figueiredo and J. C. Vital, "Kickback noise reduction technique for CMOS latched comapartors," IEEE Trans. Circuits Syst. II, Exp. *Briefs*, vol. 53, no. 7, pp. 541– 545, Jul.2006.s

[13] B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1148–1158, Jul. 2004.