T-CAD Assessment of Non-Conventional Dual Material Double Gate SOI MOSFET

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ABSTRACT
The upcoming trend in VLSI technology has led to the miniaturization of semiconductor devices which in turn is strongly dependent on the advancement in the CMOS technology. The present technology is below sub-100 nm in channel length which is the minimum dimension of single device. As CMOS technology dimensions are being intrusively scaled down to the fundamental limits such as reduction in carrier mobility due to impurity, increasing gate tunneling effect as the gate oxide thickness decreases, increasing p-n junction leakage current as the junction become more and more shallow, etc.. Established by the material characteristics, secondary effects begin to influence the performance of the device significantly and more accurate device models such as MOS device structures are needed to be developed. All these requirements have led to development of alternative technology which is the (SOI) Silicon-On-Insulator technology. This SOI is one such alternative technology which can offer the performance that is expected by the next generation Si technology. In my work, a Dual-Material Double Gate Fully-Depleted SOI MOSFET has been analyzed. The analytical model for the MOSFET's electrical parameters (such as electric field distribution, electron velocity distribution, sub-threshold swing, threshold voltage, device capacitance, drain-current, trans-conductance, drain-resistance, cut-off frequency and transit time) has been developed and the results are compared by numerical analysis using ATLAS. It has been seen that this structure provides for significant improvement in high frequency behavior of the device. And an effort has been taken to control the short-channel effects.

Index Terms
Dual material double gate, Atlas Device simulator, SOI

1. INTRODUCTION
Since the invention of the first calculation machine, the density of circuits continues to increase with the shrinkage of individual device dimension. Decreasing circuit dimension reduces the overall circuit area, thus allows more transistors on a single die without negatively impacting the cost of manufacturing. From the beginning constant miniaturization has become the standard option to increase circuit speed and to reduce the cost and power. Electronic devices have brought, and will bring in the future, a far increasing number of new functions to the basic computing systems such as fast data computing, telecommunication and several kinds of actuations which are collectively fabricated on the same physical object named *solid state circuit*, *integrated circuit* or *chip*. In present electronic era, electronic devices are so small, that billions of basic functions are accessible in a hand held system. Moreover, their unit cost has been divided by more than a factor of 100 million over the past 30 years! In the history of mankind, the fabrication of miniaturized, high speed, low power electronic devices have given a tremendous technological success and this has been achieved with innovative fabrication process. Continuous scaling of device dimension to a quasi-nanometer level allows the technologists and researchers to build complex integrated systems on a single chip which reduce drastically their volume and power consumption per function, whilst tremendously increasing their speed.

2. SOI MOS STRUCTURE
Perhaps the most attractive alternative to conventional MOS devices is a variant on SOI MOSFETs. As the device count in an ultra-dense integrated circuit is running into billons per chip, the issue of power dissipation in the chip is becoming one of the two most important issues (other being the speed). Through scaling, decreasing device dimensions have reached a state where the performance of the bulk silicon MOSFET is limited by the fundamental physical limits such as reduction in carrier mobility due to impurities, increasing gate tunneling effect as the gate oxide thickness decreases and increasing p-n junction leakage current as the junctions become more and more shallow [2.56]. Low operating voltage is a necessity as reduced power consumption is aimed at. These requirements have led to development of some alternative technologies. The SOI technology is one such alternative which can offer a performance as expected from next generation silicon technology. Figure 2.8 shows the structures of n-enhancement bulk Si MOSFET and the corresponding SOI MOSFET. The main difference between the two is that in the SOI structure the silicon channel layer is separated from the substrate by a layer buried layer or Buried Oxide (BOX, generally is SiO_2 layer).

3. SIMULATION MODEL
The third generation of BSIM model has been widely used by most semiconductor and IC design companies world-wide for device modelling and memory and processor design [5]. For present analysis, latest fourth generation BSIM4 (verilog-a version) model has been used for conventional MOS SRAM cell design [5]. For Dual material SOI, very recently developed BSIMSOIv4.4.va model has been used. Firstly, schematic has been designed with GATEWAY simulator of SILVACO and then generated spice code has been executed in SMART SPICE using SILVACO.

4. CIRCUIT OPERATION
A schematic view of n-channel SOI MOSFET (fully-depleted) implemented in 2-D device simulator has been shown in Fig 1. M1 and M2 are the gate metals with length of L1 and L2. The doping concentration in p-type and n source/drain regions is $6x10^{16}cm^{-3}$ and $3x10^{19}cm^{-3}$ respectively.

Gate oxide thickness, buried oxide thickness and thin film thickness are 5,400, and 50 nm. Work function is chosen such as 4.5 and 4.1 ev respectively. The device parameters of SMG are equivalent to that of DMG.

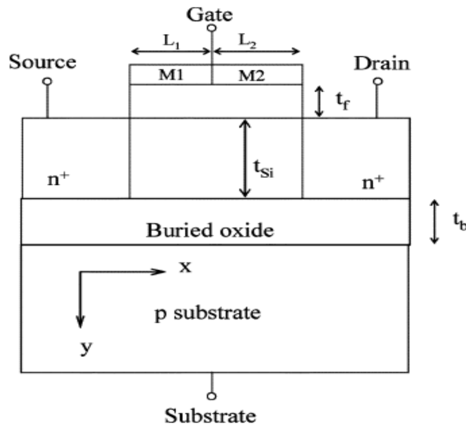

Fig:1 Cross sectional view of fully depleted DMG SOI n-channel

5. SOFTWARE USED

Device simulations have been performed at 30nmtechnology node using Silvaco. ATLAS device simulator.Silvaco software package (DEVEDIT-2d) is used to design the device structures. DMDG MOSFET structure and several DMDG MOSFET structures are simulated to show the performanceevaluation of various dual insulator structures and standardMOSFET.The models that are activated in the simulations arecomprise of the inversion layer Lombardi constant voltage andtemperature (CVT) mobility model that considers the effect of parallel and perpendicular fields, along with doping and temperature dependent parts of the mobility. The Shockley Read Hall and Auger recombination models for minority carrier recombination are used. Furthermore, Gummel's method (or the decoupled method), along with Newton's method (or the fully coupled method), are included in the CVT model to solve the equations. The inversion layer quantum effects are not considered in the present analysis, as these effects are significant for oxide thicknesses smaller than 5 nm and for channel length below 10 nm.

6. RESULTS & DISCUSSION

The properties of fully depleted DMG SOI MOSFET have been studied in the context of its potential integration in the current CMOS technology. The unique features of the DMG that is not available in the conventional SOI devices which include: Threshold Voltageroll-up reduced DIBL and simultaneous trans-conductance enhancement and SCE suppression. They can be controlled by an alternative way of gate material engineering.

One of the difficulties in Integrating DMG structures in the present CMOS technology maybe its asymmetric structure.

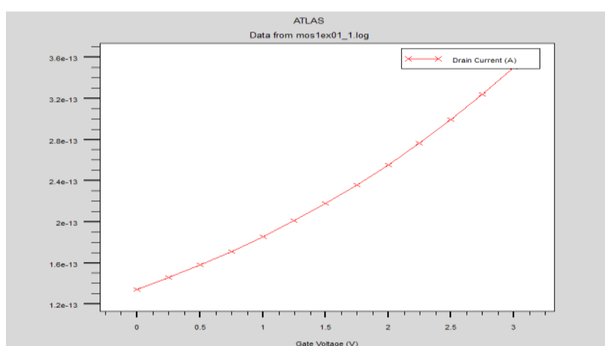

Fig 2

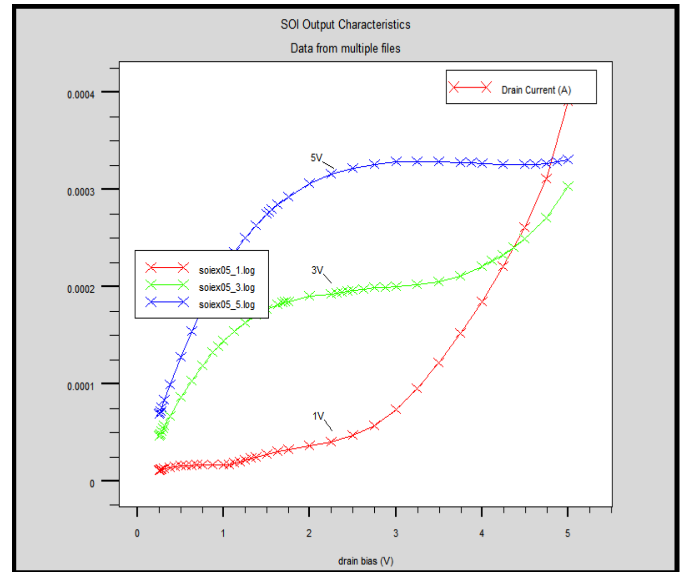

Fig 3: Drain Current Variation

7. CONCLUSIONS

In a short channel MOS structure operation is asymmetrical even at very small drain bias due to a higher drain side electric field resulting in short-channel effects like DIBL. Some unconventional asymmetrical structures have been employed to reduce the drain side electric field and its consequent impact upon the channel.

Dual-Material Gate structure employs "gate-material engineering" instead of "doping engineering" with two different work-function metal side by side as single gate to introduce a potential step in the channel. This concept leads to a suppression of SCEs and an enhanced source side electric field resulting in increased carrier transport efficiency in the channel region. FDDMGSOI may also be employed in symmetric structures (like an LDD spacer). With the CMOS processing technology already into the 100-nm regime fabricating sub-100-nm feature gate lengths should not preclude the possibility of realizing the substantial performance gains over conventional SOI devices and excellent immunity against SCEs that the DMG SOI MOSFET promises.

The future scope of the paper can be still developed by changing the material of the gate and again the performance can be compared with that of the silicon material used.

8. REFERENCES

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