Certain Investigations on Power Performance in Nanoscale CMOS Digital Circuits with Low Leakage Design Techniques

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ABSTRACT
In this paper, it is attempted to analyze the power performances of few CMOS digital circuits such as full adder, multiplexer and SRAM cell with the inclusion and redesign of ultra low leakage (ULL) techniques. The basic principle behind this ULL is based on a pair of source-connected N-MOS and P- MOS transistors, automatically biasing the stand-by gate-to source voltage of N-MOSFET at negative and P-MOSFET at a positive voltage levels, thereby pushing the leakage current towards its physical limits. Virtual ground concept is also introduced to reduce the power dissipation further. The circuits are designed with DSCH schematic design tool using CMOS 90nm technology and simulations are performed by using Level3 model files. The final layout of all circuits is generated using microwind. From the obtained results, a significant amount of power reduction is noticed without other functional performances such as area and speed are getting affected.

General Terms
Analysis, Power Performance, Design

Keywords
Power optimization, Ultra Low Leakage, Virtual ground, CMOS digital circuits, Full Adder, Multiplexer, SRAM cell

1. INTRODUCTION
Low power has emerged as a major theme in today's electronic industry. The urge for low power has caused an important paradigm shift where power dissipation played a considerable role. The factors contributed to this include wide use of wireless communication systems, integration of more number of transistors in a single chip. In most of the high performance design the leakage component of power consumption is comparable to the switching component. Power consumption results from both static leakage and dynamic switching [10]. Dynamic switching can be reduced by lowering the total capacitance or supply voltage while the static leakage reduction needs a drastic reduction of the off current (Ioff). In conventional CMOS design, Ioff is determined by the MOSFET drain current (ID) at zero gate-to source voltage (VGS) and can hence be decreased by increasing the MOS threshold voltage (Vth), but at the expense of functional performance (i.e. speed or frequency).

To overcome this drawback disruptive ultra low leakage technique is experimented. In this technique the n-MOS (resp. p-MOS) FET can be automatically biased at negative (resp. positive) VGS in stand-by mode, thereby pushing Ioff towards its physical limits[1-9] to reduce the off current without affecting other functional performances. The three ULL basic blocks are a 2- terminal diode [3], a 3-terminal transistor [6] and a voltage follower [2].

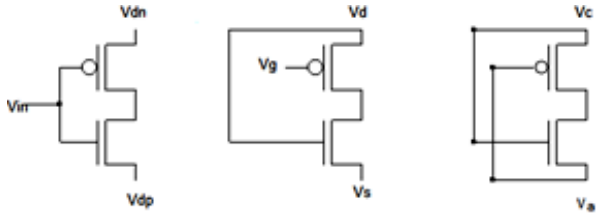


Figure 1:ULL basic blocks: (a) Voltage follower, (b) Transistor, (c) Diode

As microprocessors and other electronics applications get faster and faster, the need for large quantities of data at very high speeds increases, while providing the data at such high speeds gets more difficult to accomplish. There are many reasons to use an SRAM design which include density, speed, volatility, and cost. The primary advantage of an SRAM over a DRAM is its speed. SRAMs are consuming most of the power of the core Processor Element. The leakage in the SRAM circuit is high when compared to the all other processor components as its consuming much power [5]. Heat dissipation also occurs, so less efficiency than all other elements. The cell stability could be less in this SRAM cell and the noise performance also high during the read operation. This is reduced to a certain extend by using the ultra low leakage technique [1].

The leakage is further reduced by using virtual ground concept. In this technique the ground terminal of the inverter is connected to the virtual ground.

2. ULL TRANSISTOR
The main concept of operation of ULL design techniques is depicted in Figure. 2.

Each n- and p-MOSFETs Vth are selected so that their respective ID-VGS saturation curves intercept at a low current in weak inversion, at each temperature [1].

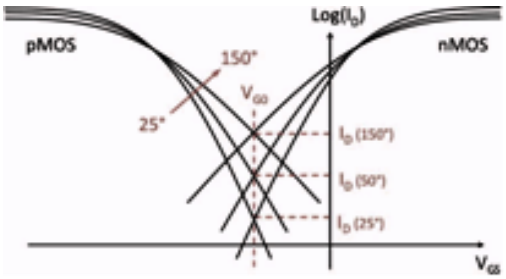


Figure 2: Typical saturation ID-VGS curves of common-source n-MOS and p-MOSFETs with sizes and Vth selections targeting an intercept current voltage bias point in subthreshold regime at each temperature [1].

In the ULL n-type transistor [6] of figure 3(a) the n-MOS gate and drain are the input and output nodes and the p-MOS gate is connected to the n-MOS drain. The leakage reduction is based on the self-biased negative/positive V_{GS} of the n/p-MOSFETs, i.e. equal to -/+ Vdd/2 in off conditions if the n/p I-V curves are symmetrical [1].

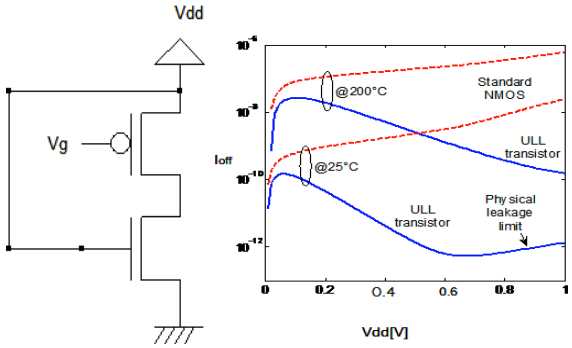


Figure 3: (a) ULL transistor (b) Measured Ioff of standard NMOS and ULL (of Figure. 2(b) transistors in SOI technology (W=1µm, L = 0.1µm, Vth = ±0.3 V) [1]

Figure 3(b) shows measured Ioff for standard and ULL n-MOS transistors in 0.13 µm SOI CMOS at room and at high temperatures. When Vdd increase, the off current first increases because VDS of both devices increase too. Then, Ioff strongly decreases as n/p- MOS VGS becomes more and more negative/positive.

3. ULL DESIGN IMPLEMENTATION IN CMOS DIGITAL CIRCUITS

3.1 ULL Multiplexer

In ULL 2:1 MUX, as shown in figure 4, ordinary transistors are replaced by the ULL transistors. The leakage power is reduced due to self-biased V_{GS} of the MOSFETS.

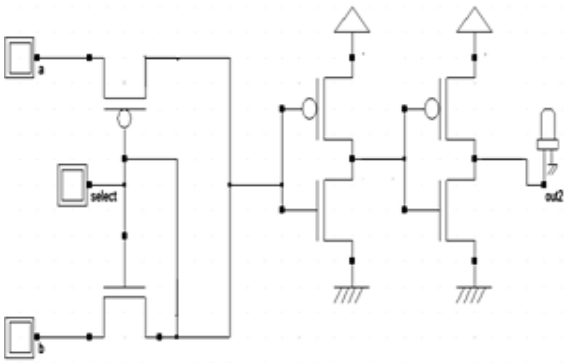
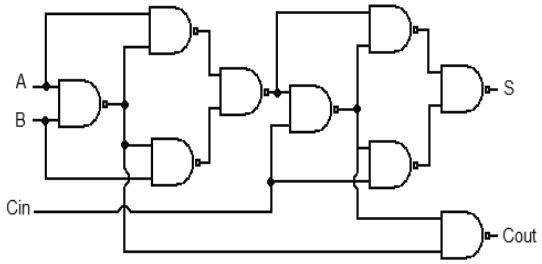


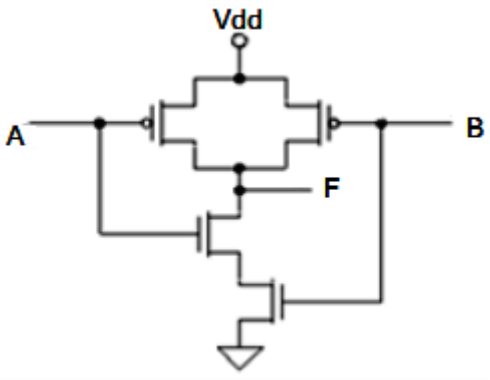
Figure 4: ULL 2:1 Multiplexer

3.2 Full adder

The idea of using ultra low design technique in combinational circuit is extended by applying the technique in 10T and 36T full adder. The NAND gate implementation of a full adder is shown in the figure 5.



(a)



(b)

Figure 5:(a) Full adder using NAND gates(b)NAND gate using CMOS Logic

Figure 5(b) depicts the internal circuitry of a NAND gate using the transistors. The transistors of a single NAND gate are replaced by the ultra low power transistor. Each block in the below figure 6 represents a NAND gate. The dotted block represents the modified ULL NAND in the full adder as shown in figure 6.

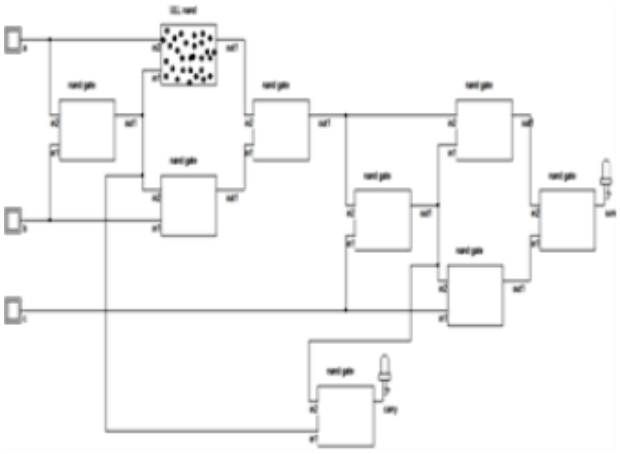


Figure 6: ULL 36T Full Adder

Due to the use of ultra low power transistors in the design, the leakage power is reduced to a great extend.

The ULL technique is also experimented in 10T full adder. It is depicted in figure 7.

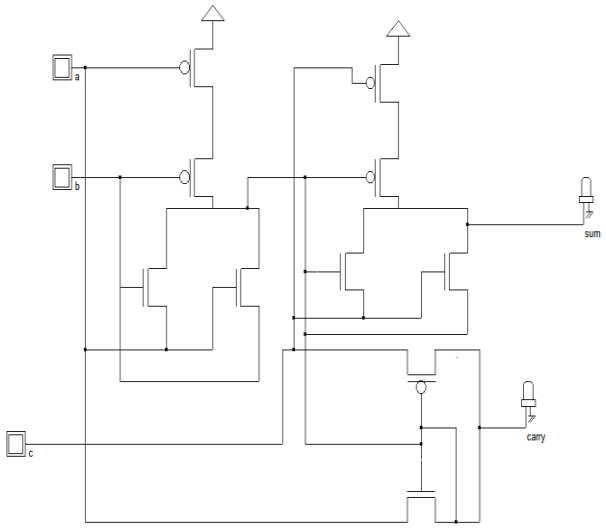


Figure 7: ULL 10T Full Adder

3.3 ULL 7T SRAM with Virtual Grounding

3.3.1 Architecture

A 7T memory cell based on the ULL latch with virtual grounding is depicted in Figure 8 with the read and writes control lines**.**

It has separated accesses for write and read operations, with two bit lines and two word lines. The cell supply voltage can be equal or inferior to the supply voltage of peripheral circuits. In retention mode, both write and read access transistors (N3 and N5 respectively) are cut off by keeping write word line low and read word line to ground.

3.3.1.1 Write Operation

Write operation is performed by writing the input data on the write bit line and then turning on N3by a high write word line voltage.

3.3.1.2 Read Operation

A 2T read buffer is used for the read operation. When the cell is accessed for read operation, read word line is set to high level and a reference source current is activated. The bit line which is precharged initially is charged or discharged depending on the stored voltage in the accessed cell. If the accessed cell stores a high voltage, the read transistor sources a current, and read bit line is discharged. If the cell stores a low voltage, N4 is cut off and is read bit line charged.

3.3.2 Virtual Ground

Whenever data is 0 and bit-Line is not enabled P2 causes unnecessary leakage. This can be avoided by connecting using P2 to the virtual ground instead of ground.

Virtual ground acts as ground when Word Line is enabled and in other case it provides logical 1. This reduces a considerable amount of leakage power.

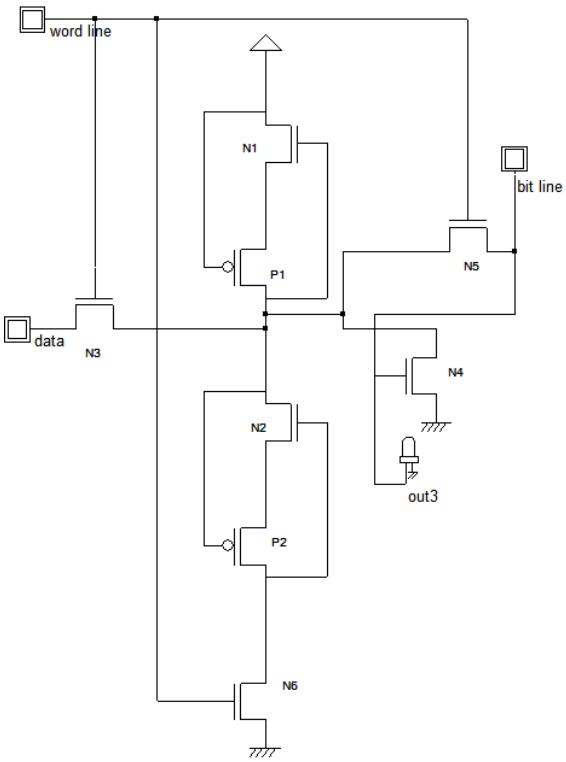


Figure 8: ULL 7T SRAM with virtual ground

4. SIMULATION AND DISCUSSIONS

The designs depicted in the figure are simulated on microwind and schematic level3 models for 90nm technology at 27^0c.

4.1 Layout

The layouts for the ULL 7T SRAM with virtual grounding are given in figure 9.

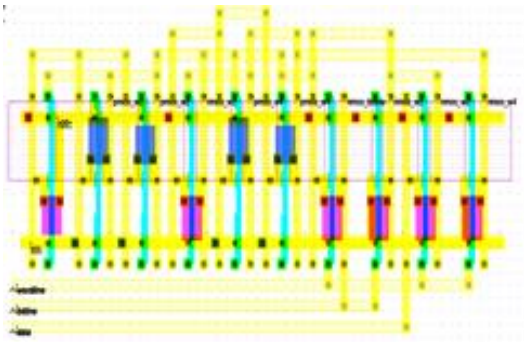
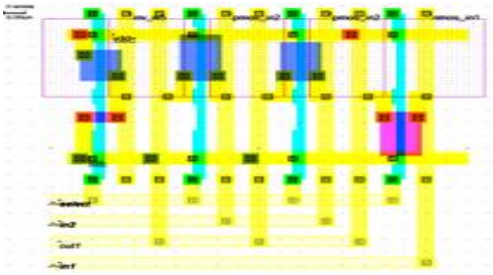


Figure 9: Layout of ULL 7T SRAM with virtual grounding

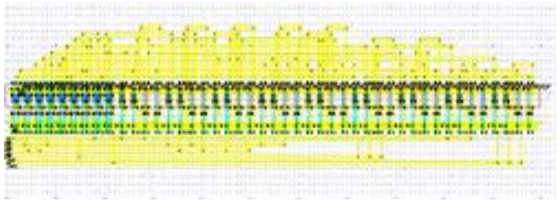
4.2 Results

The circuit designs are experimented at 27^0c in 90nm technology. The simulated ULL design in MUX gives a power consumption of 0.782µW.The leakage power of the 2:1 MUX is reduced 340 times compared to the conventional design.

Replacement of transistors in a single NAND gate of 36Tfull adder reduces the power in to 23µW.



(a)



(b)

Figure 10: Layout of CMOS digital circuits (a) ULL 2:1 MUX (b) 36T ULL Full adder

Use of virtual grounding technique in SRAM cell increases the read stability by reducing the leakage power from microwatts to nano watt range (9nw). The proposed system achieves 14x leakage reduction when comparing to the conventional ULL 7T SRAM cell.

4.3 Discussions

Table 1 summarizes the performance of the proposed system compared with the conventional design.

Table 1. Performance comparison

Circuit	Conventional design		Proposed design		% reduction	
	Power (in watts)	*Area (in μm^2)*	*Power (in watts)*	*Area (in μm^2)*	*Power*	*Area*
2:1 MUX	0.169e-3	71.00	0.78e-6	25.00	99.54	64.79
Full adder (10T)	6.03e-6	119.00	0.07e-6	119.35	98.88	-2.90
Full adder (36T)	65.15e-6	491.00	23.35e-6	471.00	64.16	4.07
ULL SRAM	0.13e-6	66.98	9.00e-9	65.65	92.86	1.87

Only in ULL 10T full adder, there is a slight increase in areas compared to the conventional one. It is because of the fact that there is no change in the number of transistors as compared to the conventional circuits. It is clear that no compromise is made in the case of area while a significant reduction is done in power. The percentage of reduction of power and area is given in the table. More than 60% power is reduced in 36T full adder and all other experimented circuit have more than 90% reduction in power without compromising the area, in addition area too get reduced

5. CONCLUSION AND FUTURE WORK

The unique ULL design is exploited in CMOS Digital circuits-2:1MUX, Full adder and SRAM circuits targeting ultra low leakage in stand-by without reducing the functional performance.

Virtual grounding is experimented in ULL SRAM circuit and the power reduction is verified.

As we illustrated, ULL technique can also be further extended to other circuits like sequential logic circuits, analog circuits and dual mode logic circuits.

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