Filtering Noise from Electrocardiogram using FIR filter with CSD Coefficients

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ABSTRACT
Filtering of ECG signal is very important because noisy ECG signal can mask some important features of the Electrocardiogram (ECG). Hence the filters are necessary to remove this noise for proper analysis of the ECG signal. This paper presents the study of FIR filter using common subexpression elimination techniques for ECG signal Processing. The common subexpression elimination techniques minimize the logic operators (LO) in realizing finite impulse response (FIR) filters. The Canonical Signed Digit (CSD) representation of filter coefficients will increase the common subexpressions which reduces the design complexity. The design examples show that the average reduction of LO achieved using the optimized method is better than the other subexpression techniques. All the techniques are designed and simulated using MATLAB and Modelsim.

Keywords
Electrocardiogram, FIR Filter, Canonical Signed Digit, Subexpression Elimination, Logical Operator.

1. INTRODUCTION
Filters are a basic component of all signal processing and telecommunication systems. Filters are widely employed in signal processing and communication systems in applications such as channel equalization, noise reduction, radar, audio processing, video processing, biomedical signal processing, and analysis of economic and financial data. A digital filter takes a digital input, gives a digital output, and consists of digital components [1].

The various blocks used in architecture of Digital FIR filter are multipliers, adders, flip flops. Generally, the recorded ECG signal is often contaminated by noise that can be within the frequency band of interest. In order to extract useful information from the noisy ECG signals you need to process the raw ECG signals using digital filters. We have used MATLAB for generating ECG wave and noise is added to the original signal as it is the most advanced tool for DSP applications. Also it helps to verify the design and results that comes from the hardware. FIR filters is designed using Parks-McClellan Algorithm.

The paper is organized as follows. In section 2, we provide filter architecture with a brief review of the CSD approach. In section 3, we illustrate the HCSE technique, VCSE technique and the CSE optimization method and its comparisons are presented. In section 4, the simulation result for the above techniques and their comparison are given. In section 5, the ECG generation and Filtering is shown. Section 6 provides our conclusions and Future enhancement is given in Section 7.

2. DIGITAL FILTER ARCHITECTURE REPRESENTATION
2.1 Canonical Signed Digit Algorithm (CSD)
The Canonical Signed Digit representation is radix-2 signed digit system with the digit set {1, 0,-1}. Given a constant coefficient, the CSD representation is that two nonzero digits are not adjacent [3]-[6]. Encoding a binary number such that it contains the fewest number of non-zero bits is called Canonical Sign Digit. A CSD representation is a kind of sum of signed power of two representations. In binary representation the value is expressed using only 0 and 1, but in CSD representation we use 0, 1 and -1 [4].

An Example for CSD representation is

$71*X = 1000111_2*X = X \ll 6 + X \ll 2 + X \ll 1 + X$ (shift/add operation) ---- (2.1)

$1000111_2*X = 100100\text{-}1*X = X \ll 6 + X \ll 3 - X$ ----- (2.2)

It is signed digit number system that minimizes the number of non-zero digits. It can reduce the number of partial product additions in a hardware multiplier. They are successful in implementing multipliers with less complexity. Now the multipliers in the digital filters are realized with shifters, adders and subtractions. Figure 1 shows the multiplier block designed using shift and add operation. The use of CSD expression can reduce the number of adders and subtractors for example, the normal binary representation would need 3 adders, as 15 is represented as 1111_2.

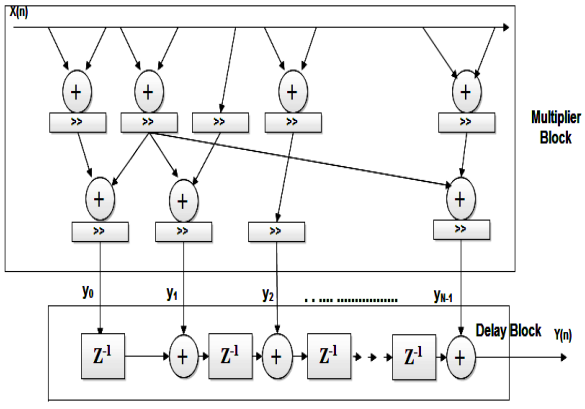

Figure 1. Multiplier Block Using Add & Shift.

The total number of adders and sub tractors is less than the number of non-zero digits by 1. This results in the area reduction of multiplier of the digital filters. The Complexity of a digital filter design depends on the number of non-zero value in the filter Coefficients. So that by using CSD representation for fixed coefficients in FIR filter design will reduces the number of partial products as well as the area and the power consumption[5]-[6].

3. COMMON SUBEXPRESSION ELIMINATION (CSE) METHODS

Two types of Common Subexpressions (CSs) [7]-[9] are generally used in CSE Techniques, the horizontal Common Subexpressions (HCSs) that exist within each coefficient and his techniques is called the Horizontal Common Subexpression Elimination (HCSE) and the Vertical Common Subexpressions (VCSs) that exist across the adjacent coefficients and this technique is called as the Vertical Common Subexpression Elimination (VCSE). A 6-tap LPFIR filter designed using Parks-McClellan algorithm is used.

Table 1 shows the 6-tap FIR filter coefficients in CSD form where -1 is denoted as n for ease of understanding. The pass-band edge of the filter is taken as 0.2π and stop-band edges is taken as 0.25π. The numbers in the first row (-1,-2…) represent the number of bitwise right shifts. In this paper, we analyze the impact of HCSE and VCSE in exploiting the symmetry of FIR filter coefficients. Further, we present an optimization algorithm to reduce the number of LOs and LD in FIR filters.

3.1. HCSE Technique

The HCSE utilizes the common horizontal subexpressions that occur within each coefficient to eliminate redundant computations. In general, these methods use Hartley's [5] two most common HCS, i.e., [1 0 1] and [1 0 –1] and their negated versions [-1 0 -1] and [-1 0 1]. If x_1 is the input signal and 2^{-j} represents shift right by j, the HCS is [1 0 1] and [1 0 -1] as shown in rectangles in figure 4 are given by

$$x_2 = x_1 + 2^{-2} x_1$$
$$x_2 = x_1 - 2^{-2} x_1 \quad \text{---------- (3.1)}$$

Using HCSE technique, the output of the filter can be represented as

$$\begin{aligned} &2^{-2}x_1 + 2^{-6}x_3 + 2^{-10}x_2 + 2^{-14}x_3 + 2^{-2}x_3[-1] + 2^{-8}x_2[-1] + \\ &2^{-12}x_3[-1] - 2^{-16}x_1[-1] + 2^{-2}x_1[-2] - 2^{-5}x_1[-2] + 2^{-9}x_1[-2] \\ &-2^{-15}x_1[-2] + 2^{-2}x_1[-3] - 2^{-5}x_1[-3] + 2^{-9}x_1[-3] - 2^{-15}x_1[-3] \\ &+2^{-2}x_3[-4] \end{aligned} \quad \text{-(3.2)}$$

where [-*k*] represents a delay of *k.*

There are two types of adders in the filter structure, structural adders (SAs) that compute the sum of convolved signals and MB adders (MBAs) which compute the sum of partial products formed in coefficient multiplication. For a given filter length N, the number of SAs is fixed. The Common Subexpression Elimination technique is mainly used to reduce the number of MBAs since they dominate the hardware cost. If N_b represents the number of nonzero bits in the symmetric half coefficient set of an FIR filter of length N, the total number of MBAs, T_{mba}, needed to realize the filter using direct method. Thus15 MBAs are required to realize the filter using direct method but only 11 MBAs (A1–A11) are needed for the HCSE implementation, which is a reduction of 26% over the direct method which is shown in [13]. The LDs of the filter circuit are identical (3adder- steps) in both direct method and CSE technique.

3.2. VCSE Technique

The VCSE Algorithm [11-13] utilize the VCSs that occur across the adjacent coefficients. The VCSs [1 1] and [1 -1], that exist across the coefficients as in [13] by x4 and x5, respectively:

$$x_4 = x_1 + x_1[-1] \text{ and } x_5 = x_1 - x_1[-1] \text{ ---(3.3)}$$

Where $x_1[-k]$ represents x_1 delayed by k units. With these VCSs, the filter output using VCSE is

$$\begin{aligned} &2^{-2}x_4 + 2^{-6}x_1 - 2^{-8}x_5 + 2^{-10}x_4 + 2^{-1}x_4 + 2^{-1}x_4 + 2^{-4}x_1[-1] \\ &+2^{-2}x_4[-2] - 2^{-5}x_4[-2] + 2^{-9}x_4[-2] - 2^{-15}x_4[-2] \\ &+2^{-2}x_4[-4] - 2^{-4}x_1[-4] + 2^{-8}x_5[-4] + 2^{-10}x_4[-4] + \\ &2^{-12}x_4[-4] + 2^{-14}x_5[-4] - 2^{-16}x_4[-4] + 2^{-6}x_1[-5] \end{aligned} \quad (3.4)$$

Since the bits that form VCSs occur across the coefficients, the symmetry of VCSs cannot be utilized when the bits are of opposite signs as denoted in [10]&[11]. Hence in VCSE, additional MBAs are required to obtain the symmetric part of the coefficients exist. Consider the VCSs across the coefficients h(0) and h(1) in Fig. 3 in [13].

$$\begin{aligned} &2^{-2}x_4 + 2^{-6}x_1 - 2^{-8}x_5 + 2^{-10}x_4 + 2^{-12}x_4 + \\ &2^{-14}x_5 - 2^{-16}x_4 + 2^{-4}x_1[-1] \end{aligned} \quad (3.5)$$

Table 1. CSD representation of 6-tap FIR Filter coefficient

Bit shift / h(n)	-1	-2	-3	-4	-5	-6	-7	-8	-9	-10	-11	-12	-13	-14	-15	-16
h(0)	0	1	0	0	0	1	0	n	0	1	0	1	0	1	0	n
h(1)	0	1	0	n	0	0	0	1	0	1	0	1	0	n	0	n
h(2)	0	1	0	0	n	0	0	0	1	0	0	0	0	0	n	0
h(3)	0	1	0	0	n	0	0	0	1	0	0	0	0	0	n	0
h(4)	0	1	0	n	0	0	0	1	0	1	0	1	0	n	0	n
h(5)	0	1	0	0	0	1	0	n	0	1	0	1	0	1	0	n

Its symmetric VCS part across the coefficients h(4) and h(5) is

$$2^{-2}x_4[-4]-2^{-4}x_1[-4]+2^{-8}x_5[-4]+2^{-10}x_4[-4]+ \\ 2^{-12}x_4[-4]+2^{-14}x_5[-4]-2^{-16}x_4[-4]+2^{-6}x_1[-5] \quad \text{--(3.6)}$$

Note that (3.6) cannot be directly obtained from (3.5) by simple delay operation. The signs and delays of certain terms of (3.6) are different from that of (3.5). Therefore, (3.6) needs to be obtained from (3.5) using (3.7) and (3.8) as given below

$$2^{-2}x_4+2^{-10}x_4+2^{-12}x_4-2^{-16}x_4 \xrightarrow{[4]} 2^{-2}x_4[-4] \\ +2^{-10}x_4[-4]+2^{-12}x_4[-4]-2^{-16}x_4[-4] \quad \text{- (3.7)}$$

$$-2^{-8}x_5+2^{-14}x_5 \xrightarrow{[4]} \xrightarrow{-} 2^{-8}x_5[-4]-2^{-14}x_5[-4] \quad \text{- (3.8)}$$

3.3 CSE Optimization Method

The main aim of the algorithm is to extract the maximum number of most frequently occurring common subexpressions. The HCSs, [1 0 1], [1 0 -1], [1 0 0 1], [1 0 0 -1] and their negated versions are used in our method since they are the most commonly occurring subexpressions. Among all the possible VCSs, we only use [11], [101] and their negated versions, since the signs of nonzero bits in these VCSs are identical (we designate these two VCSs as 'compatible VCSs'). Therefore, the use of these compatible VCSs facilitates better utilization of coefficient symmetry. Note that other HCSs [10 0 01] and [10 0 0 01] and other VCSs [10 01] and [10 01] are also exist in the CSD representation of coefficients which can also be used in CSE process. However, their frequency of occurrence is relatively smaller when compared to the HCSs and VCSs we have chosen. Fig.2 shows the filter design using our CSE optimization technique for 6tap and 16tap design.

For any coefficient, the CSs (HCSs or VCSs) with highest frequency are selected with priority given to HCSs first. If two or more HCSs occur common to different coefficients and they are having identical shifts between them which are known as identical-shift HCSs (IS-HCSs). Each coefficient is compared with all the other coefficients for IS-HCSs. If more than one common IS-HCSs occur between a coefficient pair, the IS-HCSs can be grouped together to further eliminate redundant computations. Our optimization procedure is given in detail in [13]

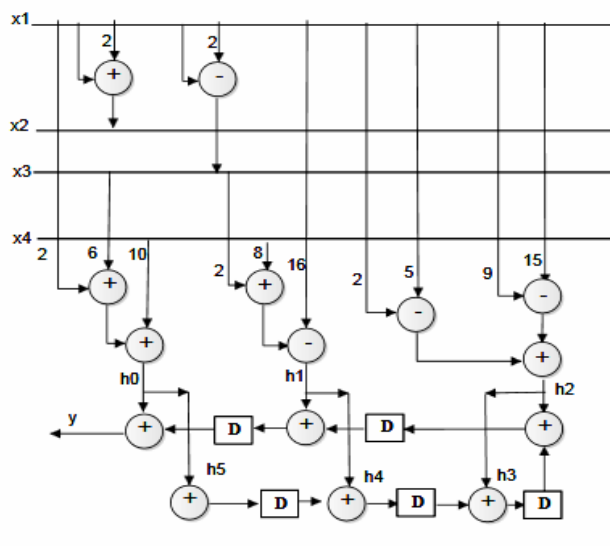

Figure 2(a). 6 tap FIR filter implementation using our CSE optimization.

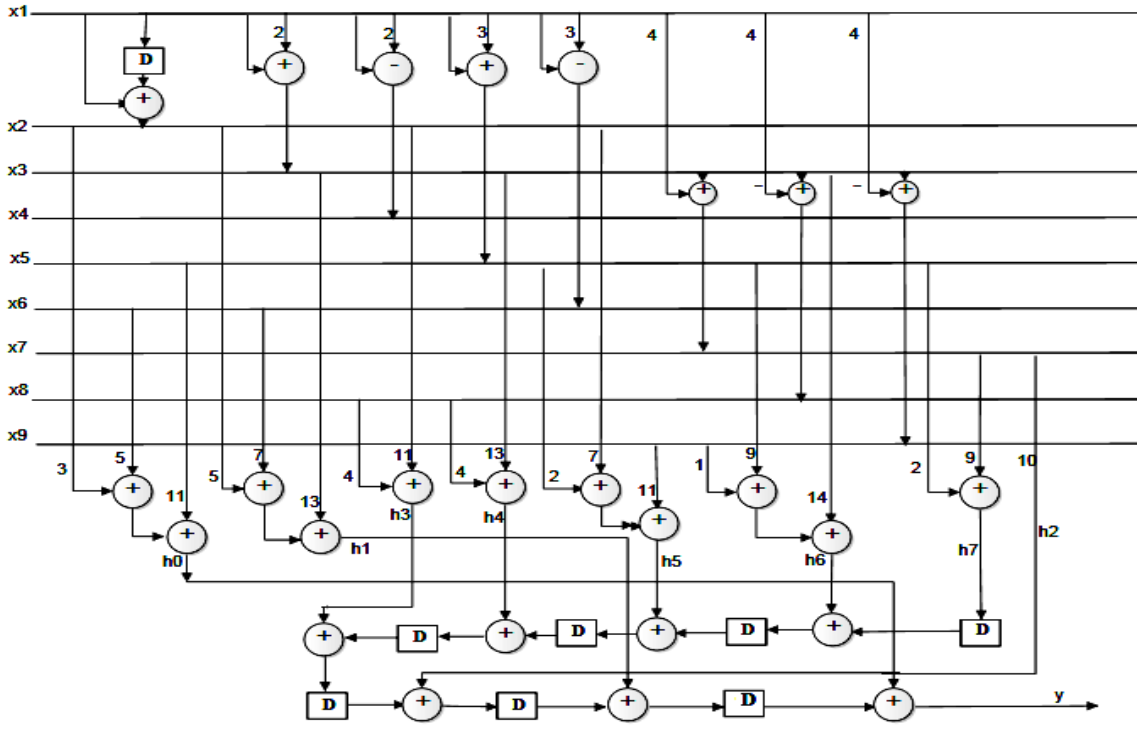

Figure 2(b). 16 tap FIR filter implementation using our CSE optimization.

Table 2 Comparison of simulation results

Technique	Filter type	N(No of filter tap)	W(No of bits)	LO	LD	IOs	No of Registers	CLOCK PERIOD (ns)	OFFSET IN TIME (ns)	OFFSET OUT TIME (ns)	REALTIME COMPLETION TIME (sec)
HCSE	FIR	6	16	11	3	66	314	10.626	12.240	16.191	13
VCSE	FIR	6	16	13	5	34	331	9.253	10.815	17.419	15
OPTIMIZED CSE	FIR	**6**	**16**	**8**	**4**	**34**	**281**	**9.220**	**10.42**	**24.07**	**15**
HCSE	FIR	16	16	20	4	34	556	11.138	13.183	21.721	48
VCSE	FIR	16	16	32	5	34	936	11.387	13.524	23.084	62
OPTIMIZED CSE	FIR	**16**	**16**	**19**	**4**	**34**	**270**	**9.247**	**10.491**	**22.347**	**16**

4. SIMULATION RESULT

Among the CSE techniques discussed the VCSE implementation requires more MBAs (13 MBAs in this case) than the HCSE despite the fact that the number of VCSs (16 VCSs) is more than the number of HCSs (12 HCSs). Furthermore, the LD in VCSE implementation (5 adder-steps) is larger than the HCSE (3 adder- steps). Hence the VCSE method results in increased LOs and LDs when compared with HCSE. The optimization algorithm produces the best reduction of LOs when compared to the other CSE algorithms in literature without increasing the LD of the coefficient multiplier. Further, the above discussed techniques are simulated using Modelsim and its results are compared with each other. The coefficients are derived from the Matlab code using Parks-Mcclellan algorithm for the specification of FIR Filter mentioned above in section 3. The Table 2 shows the comparison table where the logical operators, logical depth, number of registers, delay and number of IOs utilized by optimized CSE method is less than other methods and techniques dented in [12], where the real time completion of HCSE is less than the optimized CSE and the reduction of 3 LO when compared to HCSE in 6 tap filter and when filter tap increases it shows that this optimized algorithm is the best for subexpression elimination in the filter design.

5. ECG WAVEFLORM GENERATION AND FILTERING

ECG Waveform distortion occurs due to,

1. Power line interference
2. Electrode contact noise.
3. Motion artifacts.
4. Muscle contraction.
5. Base line drift.
6. Noise generated by electronic devices.

The ECG signal corrupted due to these noises leads to wrong diagnosis [14]. Therefore, to reduce and remove the noises, digital filters are widely used in biomedical signal processing[15]. The ECG signal is generated with constant PQRSTU amplitude and time intervals in MATLAB as shown in fig.3 and a noise The biomedical signal filtering is done using FIR filter or simply IIR filter. The frequency of ECG signal is between 0.5 Hz-100Hz.This ECG gets corrupted due to various kinds of the artifacts signal such as sine wave is also generated and added to the original ECG signal so that the resulting noisy signal is generated using MATLAB code as shown in fig.4.

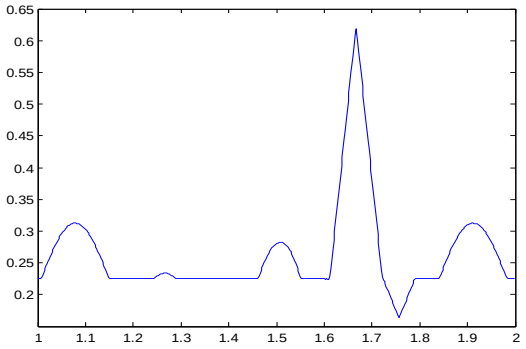

Figure 3 Original ECG waveform

The samples are taken from the noisy signal in MATLAB and they are passed in to ADC to obtain the 16 bit binary value to pass the signal values to filter. The ADC, DAC and FIR Filter are coded in VHDL using Modelsim and the filtered result is converted to analog using DAC to plot the filtered wave and verify the output of the filter with the original ECG wave. The output of the filter from modelsim is used to generate a waveform using MATLAB as shown in fig.5.

6. CONCLUSIONS

As the noise present in ECG signal lead to improper diagnosis so the digital filters can be used to remove these noises.

The FIR filters have the following advantage,

1. FIR filter are always stable as they have non-recursive structure.
2. They gave the exact linear phase.
3. Efficiently realizable in hardware.
4. The filter response is of finite duration.

From section 4, it is clear that the optimized CSE method is having less number of IOs and registers when compared to other CSE techniques and when the number of taps increases it gives a better result. This technique however suits only for the linear phase symmetrical coefficients fir filter with constant coefficient. By observing the VHDL simulation results we conclude that the filter functions correctly which matches the MATLAB design of the filters. The delay between input and output signal is 998396.5 ns.

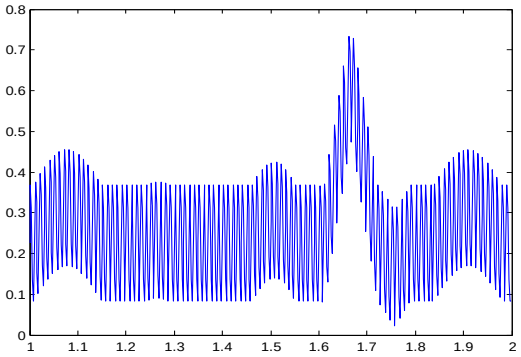

Figure 4 Noisy ECG waveform

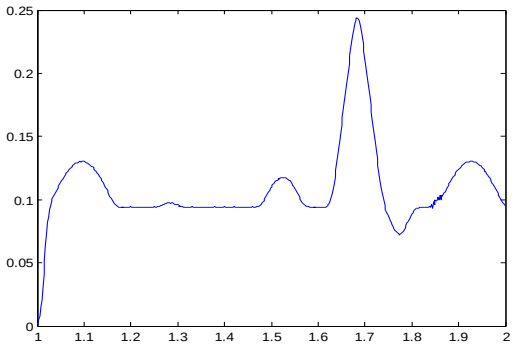

Figure 5 Filtered ECG waveform

7. FUTURE WORK

The ECG signal filtering is done using our filter architecture which has the overall advantage. The design is further studied for its performance. In Future the proposed design is implemented in other signal processing applications like audio and video signal processing and comparison of existing and proposed method are made to analyze the performance and the stability of the design.

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