Performance Analysis of High Speed Double Tail Dynamic Comparator

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ABSTRACT:
In this paper, we present a performance comparison of existing clocked dynamic comparators. As delay is directly correlated with the submicron scaling, we investigate the performance of the above comparators in terms of delay and Power-Delay Product (PDP). PDP gives the average energy dissipated by the comparator for a single comparison. Simulation results using Mentor Graphics revealed better performance of High Speed Dynamic Comparator (HSDC) compared to conventional clocked comparators in 180nm, 250nm and 350nm technologies. Implementation results reveal that high speed dynamic comparator has energy dissipation of 25.14% less compared to the best of the designs used for comparison when operated at 50 MHz.

Keywords:
Clocked dynamic comparator, Analog-to-Digital Converters (ADCs), Common mode voltage

1. INTRODUCTION
An important circuit used for transition of the analog signal to digital signal is the comparator. In general, a comparator is a device, which compares two currents or voltages and produces a digital output based on the comparison. Many high speed ADCs, such as flash ADCs, require high-speed, low-power comparator.

Due to high speed, low power consumption, high input impedance and full-swing output dynamic latched comparators are very attractive. They use positive feedback mechanism with one pair of back-to-back cross coupled inverters (latch) in order to convert a small input-voltage difference to a full-scale digital level in a short time. Designing high-speed comparators suitable to be operable in low supply voltages is a more challenging work.

Many techniques, such as supply boosting methods [2] that can handle higher supply voltages have been developed to meet low-power design challenges. These are effective but introduces reliability issues in CMOS technologies. Two power-saving schemes namely the current-controlled latch sense amplifier and static power-saving input buffer (SPSIB) for high-performance VLSIs with a large-scale memory and many interface signals were described by Kobayashi et al [7]. A CMOS latch-type voltage sense amplifier was designed with a separated input and cross-coupled stage [4]. Based on Blalock [8] approach, a 1-bit quantizer for sub-1V $\sum\Delta$ modulators was proposed by Maymandi-Nejad and Sachdev [9]. A comparator with a modified latch [2] is different from the conventional circuit by replacing a new latch for low power supply voltage operation (i.e.) for supply voltages down to 0.65V for 65nm technology. This latch is helpful in low power supply voltage operation.

A low power, low voltage Successive Approximation Analog-to-Digital Converter (SAR ADC) design based on supply boosting technique is proposed in [3]. SBT is suitable for mixed-signal circuit designed for energy limited applications and systems in where supply voltage is in the order of threshold voltages of the process. Many researches contribute in analyzing the performance of the dynamic comparators. Random decision errors are analyzed in the dynamic comparators using LPTV (Linear Periodically Time Varying) model [5]. A method to estimate the input referred noise in fully dynamic regenerative comparators leveraging a reference architecture is proposed in [10]. The effect of load capacitor mismatch on the offset of a regenerative latch comparator is analyzed in [11]. Kickback noise reduction by neutralization technique is investigated by Figueiredo and Vital [12] and offset cancellation by body voltage adjustment using low-power simple analog control feedback circuit without any additional capacitive loading at the comparator output is investigated by Babayan-Mashhadi and Lotfi [13]. A novel balanced method is proposed to facilitate the evaluation of operating points of transistors in a dynamic comparator in [14], making it possible to obtain an explicit expression for offset voltage in dynamic comparators.

As high speed is the great demand of comparators used in portable applications today, we present a performance comparison of various existing dynamic comparators in terms of delay using different submicron technologies in this brief. The rest of the paper is organized as follows: Section II describes the architecture and working of existing single tail and double-tail dynamic comparators. Analytical expression for the computation of delay is also presented. Section III gives the experimental results of the existing dynamic comparators discussed in section II in different technologies and, Final section IV gives brief conclusion.

2. EXISTING CLOCKED COMPARATOR DESIGNS
Conventional dynamic [7] and double-tail comparators [4], [1] are clocked regenerative comparators which are useful in high speed ADCs like flash ADC because of their fast decision making capability due to strong feedback loop in the regenerative latch. The analyses presented in literature investigate the performance of the comparators in terms of noise [10], offset [11], [13] and [14], random decision errors [5] and kick back noise [12]. Since delay is directly correlated

with the submicron technology, we investigate the performance of the above comparators in terms of delay using different technology files.

2.1 Conventional Dynamic Comparator

Kobayashi et al. (1993) [7] proposed a latch type dynamic comparator and is shown in Fig.1 (two cross-coupled inverters).It has high input impedance, rail-to-rail output swing and there is no static power consumption. There exists an indirect influence of the parasitic capacitances of the input transistors (larger gate area for lower offset) to the output nodes and, thus, influences switching speed. The novelty of the Kobayashi's design is the use of a sleep transistor (M_{tail}) which establishes the path from VDD to GND only when the circuit is active and the design operates in two phases to produce an output.

a) Reset phase

In reset phase CLK=0, sleep transistor M_{tail} is OFF, and reset transistors (M_7–M_8) will be ON and pull both output nodes Out_n and Out_p to V_{DD} to define a start condition and to have a valid logical level during reset.

b) Comparison phase

In the second phase i.e., comparison phase CLK=V_{DD}, sleep transistor M_{tail} is ON and transistors M_7 and M_8 are OFF. The output voltages (Out_p, Out_n), which had been pre-charged to V_{DD}, start to discharge in this phase with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where $V_{INP}>V_{INN}$, Out_p discharges faster than Out_n, hence when Out_p (discharged by transistor M_2 drain current), falls down to $V_{DD}-|V_{thp}|$ before Out_n (discharged by transistor M_1 drain current), the corresponding pMOS transistor (M_5) will turn on initiating the latch regeneration caused by back-to-back inverters (M_3, M_5 and M_4, M_6). Thus, Out_n pulls to V_{DD} and Out_p discharges to ground. If $V_{INP}<V_{INN}$, the circuits works vice versa.

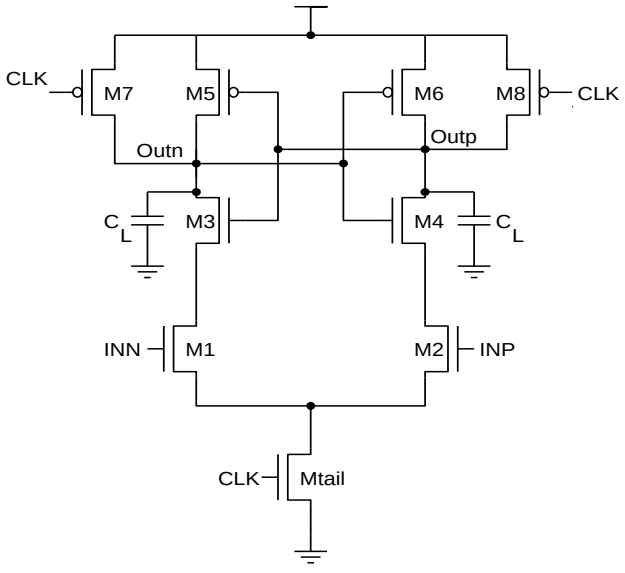

Fig. 1. Schematics of the Conventional Dynamic Comparator

The delay of this comparator is given by,

$$t_{delay} = t_0 + t_{latch} \quad (1)$$

$$t_{delay} = 2\frac{C_L|V_{Thp}|}{Itail} + \frac{C_L}{gm,eff}\ln\frac{V_{DD}}{4|V_{Thp}|\Delta Vin}\sqrt{\frac{I_{tail}}{\beta_{1,2}}} \quad (2)$$

The features of Kobayashi's design is that it has high input impedance, robustness against noise and mismatch. In addition, the use of sleep transistor eliminates static power dissipation. However the use of stacked transistors, necessitates sufficient high supply voltage to maintain proper delay.

2.2 Conventional Double-Tail Dynamic Comparator

Shinkel et al. (2007) [4] proposed a double-tail dynamic comparator which has a separate input-gain stage and output-latch stage and is shown in Fig. 2. The grouping of input and output stages as two different stages made this comparator to have a lower and more stable offset voltage over a wide common-mode voltage (V_{cm}) range and to operate at reduced supply voltage. It is because by controlling the sizes of the tail transistors (M_{tail1} and M_{tail2}) of the input and output-stage in such a way that a small tail current for the differential input pair can obtain a long integration time and a better g_m/I_D ratio for a bigger gain (hence, less offset voltage) and a large tail current for the output latch-stage for fast regeneration, so one can get high speed and low offset voltage with less dependence on $V_{cm.}$

Since this comparator requires both clk and $\overline{clk}$ signals for its operation, a high synchronization between clk and $\overline{clk}$ is required because the second stage has to detect the voltage difference between the differential outputs of the first gain stage at very limited time. If a simple inverter is used to generate $\overline{clk}$, it inserts an additional load on the clock generator. If $\overline{clk}$ is lagging clk , it results in increased delay and if $\overline{clk}$ is leading clk , it results in increased power dissipation due to existence of short circuit current path M_{tail2} to M_7/M_8 through M_{R1}/M_{R2} and it can even increase the latch offset voltage if the device mismatch between M_7 and M_8 is significant.

Similar to Kobayashi et al.'s (1993) design Shinkel et al's (2007) comparator has two phases of operation viz., reset phase and comparison phase, to compare the inputs.

(a) Reset phase

In this phase CLK=0, $Mtail_1$, and M_{tail2} are OFF, transistors M_3-M_4 pre-charge fn and fp nodes to V_{DD}, which turn causes transistors M_{R1} and M_{R2} to discharge the output nodes to ground.

(b) Comparison Phase

In this phase CLK = V_{DD}, M_{tail1} and M_{tail2} turn on, M_3-M_4 turn off and voltages at nodes fn and fp start to drop with the rate defined by $I_{Mtail1}/C_{fn(p)}$ and on top of this, an input-dependent differential voltage $\Delta V_{fn(p)}$ will build up. The intermediate stage formed by M_{R1} and M_{R2} passes $\Delta V_{fn(p)}$ to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise.

Delay of conventional double-tail dynamic comparator is given as,

$$t_{delay} = 2\frac{VThn\ CLout}{Itail2} + \frac{CLout}{gm,eff}\ln\left(\frac{\frac{VDD}{2}}{\Delta Vo}\right) \quad (3)$$

$$t_{delay} = 2\frac{VThn\ CLout}{Itail2} + \frac{CLout}{gm,eff}.\ \ln$$

$$(V_{DD}I^2_{tail2}C_{L,fn(p)}/8V^2_{Thn}C_{Lout}g_{mR1,2}g_{m1,2}\Delta V_{in}) \quad (4)$$

However in Shinkel et al's (2007) comparator both intermediate transistors will be cut-off, (since fn and fp nodes both discharge to the ground) and thus, during reset phase, these nodes have to be charged from ground to V_{DD}, which leads to high power consumption.

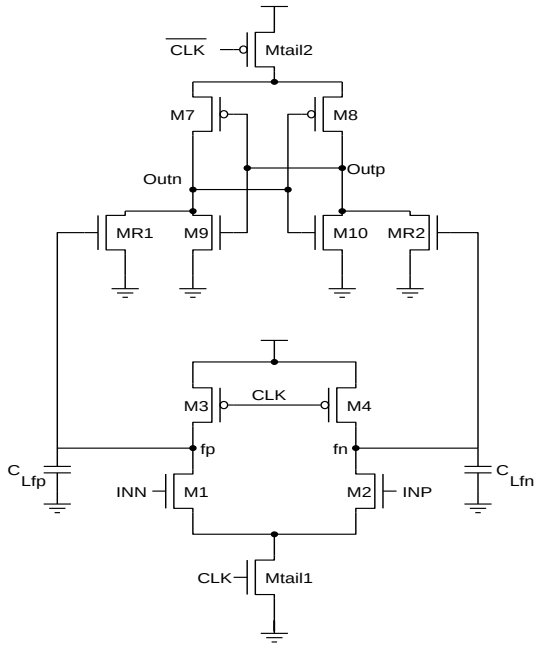

Fig. 2. Schematic Diagram of the Conventional Double-tail Dynamic Comparator

2.3. High Speed Double-Tail Dynamic Comparator

Samaneh Babayan-Mashhadi and Reza Lotfi (2013) [1] proposed a high speed energy efficient double-tail dynamic comparator. Due to the better performance of double-tail architecture in low-voltage applications, Samaneh Babayan-Mashhadi and Reza Lotfi design incorporates double-tail in its architecture. The main idea of this comparator is to increase $\Delta V_{fn/fp}$ in order to increase the latch regeneration speed. For this purpose, two control transistors (M_{c1} and M_{c2}) have been added to the first stage in parallel to M_3/M_4 transistors but in a cross-coupled manner as shown in Fig. 3.The design operates in two phases to compare the two inputs viz., Reset Phase and Comparison Phase.

(a) Reset phase

In reset phase (CLK=0, M_{tail1} and M_{tail2} are OFF, avoiding static power), M_3 and M_4 pulls both fn and fp nodes to V_{DD}, hence transistor M_{c1} and M_{c2} are cut off. Intermediate stage transistors, M_{R1} and M_{R2}, reset both latch outputs to ground.

(b) Comparison Phase

In this phase (CLK=V_{DD}, M_{tail1}, and M_{tail2} are ON), transistors M_3 and M_4 turn OFF. Furthermore, at the beginning of this phase, the control transistors are still OFF (since fn and fp are about V_{DD}). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose $V_{INP} > V_{INN}$, thus fn drops faster than fp, (since M_2 provides more current than M_1). As long as fn continues falling, the corresponding pMOS control transistor (M_{c1} in this case) starts to turn on, pulling fp node back to the V_{DD}; and another control transistor (M_{c2}) remains off, allowing fn to be discharged completely.

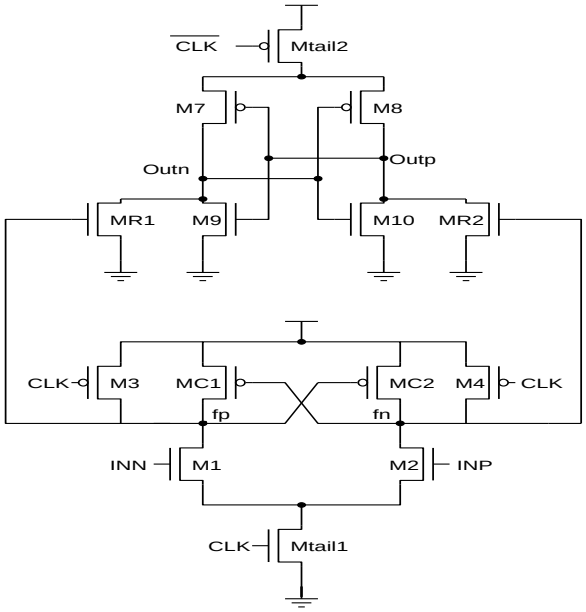

Fig. 3. Schematic of the High Speed Energy Efficient Dynamic Comparator

2.3.1 Static Power Eliminated version (HSDC -SPEV)

To overcome the issue of direct current path from V_{DD} to ground .Two nMOS switches below the input transistors [M_{sw1} and M_{sw2}] and is shown in Fig. 4. At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to V_{DD} (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates.

As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference

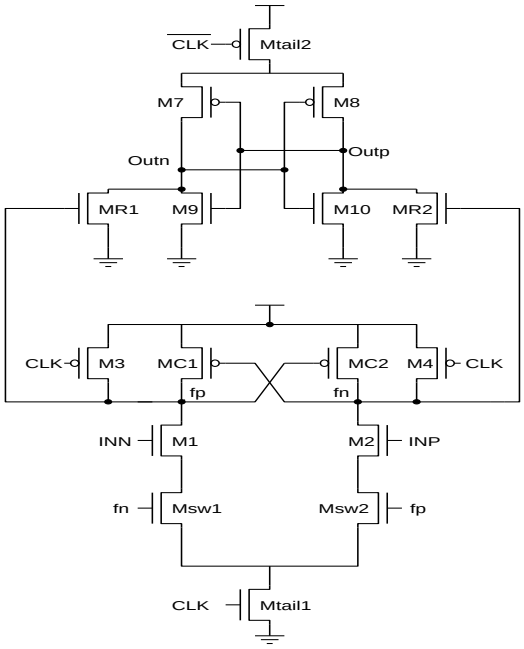

Fig. 4. Schematic of the High Speed Dynamic Comparator

Suppose that fp is pulling up to the V_{DD} and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn fromV_{DD}) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

Delay of this design is given by,

$$t_{delay}=2\ \frac{VThn\ CLout}{Itail2}+\frac{CLout}{gm,eff+gmR1,2}\ln\left(\frac{\frac{VDD}{2}}{\Delta Vo}\right) \quad (5)$$

$$t_{delay}=2\ \frac{VThn\ CLout}{Itail2}+\frac{CLout}{gm,eff+gmR1,2}\ X\ \ln\left(\frac{\mathbf{VDD}}{\mathbf{2}}/\left(\mathbf{4V_{Thn}}\left|\boldsymbol{V_{Thp}}\right|\frac{\boldsymbol{g_{mR1,2}}}{\boldsymbol{I_{Tail2}}}\frac{\boldsymbol{g_{mR1,2}\,\Delta V_{in}}}{\boldsymbol{I_{Tail1}}}\mathbf{exp}\left(\frac{\boldsymbol{G_{m,eff1}.t_0}}{\boldsymbol{C_{L,fn(p)}}}\right)\right)\right) \quad (6)$$

The novelty of the design is that it has high speed compared to the conventional double-tail dynamic comparator [4] due to high initial output voltage difference (ΔV_o) and Effective transconductance (g_{meff}).

3. RESULT ANALYSIS

Transient simulation of the conventional dynamic comparator [7], conventional double-tail comparator [4] and High speed Energy efficient double-tail comparator [1] were performed using MENTORGRAPHICS with 180nm sub-micron technology file.

The pMOS and nMOS transistors in the circuits are sized to satisfy its drive capability. In order to measure the delay at the output nodes, CLK signal is set as the reference. The delay at the output nodes (Outn and Outp) are measured with respect to the clock. The parameters used for the simulation are: ΔV_{in}=5mV, V_{cm}=0.7V, V_{DD}=0.8V,INN=0.6975V and INP=0.7025V with the rise and fall time of the clock maintained equal and is kept at 1ns. Here the results of the existing comparators in terms of delay, power and PDP are shown in Table 1 for the frequency of 50MHz.

It is seen from Table 1 that the delay of the HSDC is lower by 90.72%, 91.03% and 43.72%, 25.14% compared to Kobayashi's [7] and Shinkel et al's [4] designs respectively. This is because the HSEEC enhances the speed by Enhancing the latch output voltage difference at time t_0 i.e., (ΔV_0) and by Enhancing the latch effective transconductance ($g_{m,eff}$).

Table 1: Power, Delay, Area and PDP Estimates of Existing Comparators

S.No.	Parameters	Conventional dynamic comparator [7]	Conventional double-tail dynamic comparator [4]	HSDC [1]
1.	Power (pW)	17.7103	12.8708	17.1250
2.	Worst Case Delay (ns)	10.860	1.7741	0.9885
3.	Power-Delay Product (PDP) ($X10^{-21}$ Joules)	192.33	22.83	16.92
4.	Transistor Count	9	12	16

The enhanced speed of the HSDC design shows better delay reduction compared to conventional dynamic comparators. The number of transistors is more in the high speed energy efficient design compared to the conventional designs.

In addition, we have estimated the delay of existing clocked comparator designs in different scaling technologies and shown in Table 2.The parameters used for simulation are V_{DD}=0.8V, V_{cm}=0.7V and ΔV_{in}=5mV with the clock frequency maintained at 50 MHz.

Table 2: Delay Estimates of Existing Clocked Comparator Designs using Different Technology Files

S. No.	Technology (nm)	Conventional dynamic comparator (ns) [7]	Delay reduction (%)	Conventional double-tail dynamic comparator (ns) [4]	Delay reduction (%)	HSDC (ns) [1]	Delay reduction (%)
1.	350	12.969	_	6.586	_	4.3732	_
2.	250	10.789	16.8	2.3906	63.7	1.2613	71.16
3.	180	10.760	17.02	1.7741	73.06	0.9985	77.17

From Table 2, it is seen that the delay of HSDC design is less compared to the conventional dynamic comparators in all technologies. Also the percentage of delay reduction is better in HSDC compared to conventional clocked dynamic comparators as we go for higher scaling. This is due to enhancement in ΔV_0 and g_{meff}.

4. CONCLUSION

A performance comparison of existing clocked dynamic comparators in different scaling technologies is carried out in this brief. As high speed and minimum energy dissipation are the main criteria in day to day portable applications, we performed an extensive delay analysis of the comparators mentioned in literature. Experimental evaluation of the existing comparator designs shows that the HSDC design show better delay reduction compared to conventional dynamic comparator designs. The analysis reveals the suitability of HSDC designs for high speed ADCs like flash ADC used in portable devices.

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