

Design of Decoder using Modified Hybrid Weighted Symbol Flipping for Nonbinary LDPC Codes

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ABSTRACT

A hybrid decoding algorithm which proposed for nonbinary and binary low density parity (LDPC) codes, both the algorithm combines the weighted symbol flipping (WSF) algorithm with the fast Fourier transform q-ary sum product algorithm (FFT-QSPA). The flipped position and value are determined by the symbol flipping metric and the received bit values in the first stage WSF algorithm. If the low complexity WSF algorithm is failed, the second stage FFT-QSPA is activated as a switching strategy. They are particularly effective for decoding LDPC codes constructed based on finite geometries and finite fields. Analyzing both the techniques nonbinary LDPC codes gives the better error performance and greatly reduces the computation complexity compared to binary LDPC codes. The proposed hybrid algorithm is used for some applications in communication systems for high speed and low power consumption.

Keywords

Nonbinary and binary low density parity-check (LDPC) code, Weighted symbol-flipping (WSF), Hybrid weighted symbol-flipping (HWSF), iterative decoding.

1. INTRODUCTION

Low density parity check codes (LDPC) is an error correcting code used in noisy communication channel to reduce the probability of loss of information. With LDPC this probability can be reduced as small as desired, thus the data transmission rate can be as close to Shannon's limit for a symmetric memory-less channel. Nonbinary low density parity-check (LDPC) codes were first proposed and proven to exhibit a significant improvement over their binary counterparts [1]. Nonbinary LDPC codes can be classified in to four general categories: (1) soft-decision decoding, (2) hard-decision decoding, (3) reliability-based decoding, (4) hybrid decoding. The most well-known soft-decision iterative decoding for nonbinary LDPC codes is the q-ary sum-product algorithm (QSPA). The error rate performance of LDPC codes is decoded by soft-decision iterative decoding algorithms. Two main branches of QSPA are studied to reduce the computation complexity: (1) frequency domain, which forms fast Fourier transform QSPA (FFT-QSPA), (2) log-likelihood ratio (LLR) domain, which forms the extended min-sum (EMS) algorithm. One of the hard-decision iterative decoding algorithms for nonbinary LDPC codes is the symbol-flipping(SF) algorithm with very low complexity and prominent performance degradation. The other hard-decision decoding algorithm is the generalized bit-flipping (GBF) algorithm for majority-logic decodable nonbinary LDPC codes [2]. And the reliability-based decoding, such as weighted SF (WSF) algorithm, can be viewed as a simplified version of soft-

decision decoding or an enhanced version of hard-decision decoding. Binary LDPC codes can be classified in to two general categories [3]: (1) Euclidean geometry, (2) Finite field LDPC codes. Euclidean geometry LDPC codes are shown to be regular gallager codes with tanner graphs of girth eight. The minimum distance of these codes is shown to be lower bounded by 2^m . They perform very well with iterative decoding. Finite field is a field that contains finite number of elements. The finite field are classified by size, there is exactly one finite field up to isomorphism of size p^k for each prime p and positive integer both nonbinary and binary LDPC codes provide a wide spectrum tradeoffs between performance, complexity and decoding speed. Combining the WSF algorithm with the FFT-QSPA, a hybrid WSF (HWSF) decoding algorithm is derived aiming to achieve an excellent error performance yet to maintain a low computation complexity.

2. PROPOSED TECHNIQUE

2.1 Nonbinary LDPC Codes

A nonbinary (N, K) LDPC code is represented by its sparse nonbinary parity-check matrix H that has N columns and $M \geq N-K$ rows. The WSF algorithm is used as the first stage iterative decoding algorithm [4]. Two parameters are required to finish one symbol flipping: the position and the value of one flipped symbol. The position of symbol is selected according to the symbol flipping position at each iteration during the decoding process. The symbol flipping function combines the number of failed checks and the calculated symbol reliability dependent on the received bits. And the updated value of the selected symbols depends on absolute values of the channel output. The more closely the absolute value of the channel output approaches zero, the less reliable the corresponding bit is. A loop detection procedure is also designed to protect the symbol selection from falling into infinite loops traps and benefit the value selection of the flipped symbol.

The symbol flipping process may enter a loop, which means that symbols are changed and changed back again after some iteration if no loop detecting strategy is applied [5]. To detect and avoid such infinite loops and favour selecting the symbol, a loop detection mechanism is introduced and applied to the WSF. We can calculate vector $E(l)$ iteratively, $l \leq k$. If any of these vectors is zero, an infinite loop is detected, and variable flag bit will be added by one, the present determined value is removed and anew value is redetermined by the updated flag bit. If flag bit reaches the size of Galois field q , it resets and the selected symbol is in the exclusion symbol list. If the first stage WSF algorithm is terminated or failed, the second well-known FFT-QSPA is activated.

2.1.1 Weighted Symbol-Flipping Algorithm

With the concepts and notations, WSF algorithm as follows:

Step 1: Define the parameters M, N and iterations. For example set the no of rows and columns say R=3, C=3 and iteration=5.

Step 2: According to rows and columns create H matrix.

$$H = \begin{bmatrix} 4 & 3 & 3 \\ 3 & 4 & 3 \\ 3 & 3 & 3 \end{bmatrix}$$

Step 3: Creation of sub matrices based on parity check matrix.

Step 4: For the matrix above calculate the syndrome. If the criteria are obtained stop the process else go to the next step. According to the input H matrix syndrome is calculated. It is independent upon the value K, and sorting the obtained result either in descending or ascending order. Rank the symbols according to the obtained result.

Step 5: Proceed till maximum iteration is obtained.

Step 6: Calculate the flipping position and flipping value based on step 5.

Step 7: Error checking process is done based on weight calculation. Calculate the vote from the paired values. The paired values is calculated for obtained weight and compared with each other. If the obtained result is lesser than predetermined value the symbols will not be corrected (i.e., symbols having no error).

Step 8: Based on weight calculation bit error value is calculated.

2.1.2 Hybrid Weighted Symbol-Flipping Algorithm

The HWSF algorithm consists of one or two stages. Decoding is implemented using WSF algorithm firstly. If all the parity checks are met, the whole decoding terminates and outputs the decoded code words. Otherwise, it switches to the second stage and decoding continues by using FFT-QSPA [6]. The second stage decoding is employed as an independent decoder to the received code words from the channel. A frame error occurs when the parity check is unsatisfied or the decoded vector is a fake code word. A fake codeword is denoted as the one that satisfy the parity check constraints but actually is not the transmitted one. Therefore, the FER of decoding almost equals the failure probability of parity checks. It means that the effect of fake words is limited. In the high SNR region, the FER of WSF is low, and the computation complexity of HWSF has been reduced with the same performance of FFT-QSPA.

With the above idea, the complete HWSF algorithm is described as follows [7]:

Step 1: Choosing the values for E_b/N_0 . Set the parameter setting values for frame error rate (FER), signal to noise ratio (SNR), iterations and gamma value (γ).

Step 2: Start the no of iterations and perform the FFT analysis.

Step 3: FFT analysis is performed for parity check matrix H and random initialize matrix and then multiply the H matrix and random initialize matrix values.

Step 4: For obtained matrix value contains the real and imaginary part for that taking the inverse fast Fourier transform (IFFT).

Step 5: Start the processing from 1: frame rate and then apply the BPSK modulation, for each bit to have energy E_b , bits in BPSK are RF pulses of amplitude A and duration T_b . Their energy is $A^2 T_b / 2$.

$$E_b = A^2 T_b / 2 \rightarrow A = \sqrt{2E_b / T_b} \quad (1)$$

Step 6: In the QSPA technique is applied for matrix value and then three operations are performed they are addition, multiplication and division.

Step 7: For these operations theoretical formula is given by,

$$\text{Nonbinary Addition} \rightarrow A_{ni1}(1 - P_{ss})C_{1A} + A_{ni2}P_{ss}C_{2A}$$

$$\text{Nonbinary Multiplication} \rightarrow A_{ni2}P_{ss}C_{2M}$$

$$\text{Nonbinary Division} \rightarrow A_{ni2}P_{ss}C_{2D} \text{ .Where,}$$

$C_{1A}, C_{2A}, C_{2M}, C_{2D}$ Denotes the complexities of WSF real

Addition, FFT-QSPA real addition, multiplication and division.

A_{ni1}, A_{ni2} denotes the no of iterations for first stage and second stage decoding. P_{ss} denotes the probability of entering the second stage.

Step 8: Calculate bit error rate (BER) and frame error rate (FER). Large K_1 demands less computational complexities with a performance loss compared to FFT-QSPA while large K_1 achieves an excellent performance with large computation complexities compared to WSF.

2.2 Binary LDPC Codes

Finite field (FF) LDPC code is in terms of real number operations for decoding LDPC codes [8]. The WSF computational complexity roughly consists of four phases: pre-processing, flipping position, function updating, selecting of flipping bit(s) in one symbol and loop detection. The soft iterative FFT-QSPA includes check node updating, variable node updating and tentative decision.

Euclidean Geometry (EG) LDPC code put either in cyclic or quasi-cyclic form. Consequently their encoding can be achieved in linear time and implemented with simple feedback shift registers [9]. Construction of H matrix represent lines and columns represent points, to ensure regularity of H matrix since two columns do not have more than one position with common 1's and number of lines is constant. The sparsity of H matrix can be obtained by $\rho \ll n$ and $\gamma \ll J$ and thus the constructed matrix can be considered as a low density parity check matrix [10].

2.2.1 Hybrid Weighted Symbol-Flipping Algorithm

With the above notations the HWSF algorithm is as follows:

Step 1: Creation of the dataset for Euclidean Geometry and Finite field LDPC codes.

Step 2: To set the parameter initialization.

Step 3: Adding the AWGN (Additive white Gaussian noise) in the channel.

Step 4: Apply the BPSK modulation.

Step 5: Calculate the Bit error rate (BER) and Frame error rate (FER)

3. SIMULATION RESULTS

3.1 Computation Complexities Required for Decoding Nonbinary LDPC Code for Hybrid Weighted Symbol Flipping Algorithm

The global complexity of HWSF is substantially lower than that of FFT-QSPA due to the first stage low complexity WSF algorithm [11]. The computation complexity for decoding of the same bit length with various algorithms at 4 dB [12].

Table 1. Comparison of Hybrid Weighted Symbol Flipping Algorithm

Decoding Algorithm	Nonbinary Addition	Nonbinary Multiplication	Nonbinary Division
Existing System FFT-QSPA	430941	528280	48820
HWSF	147115	66326	6129
Proposed System HWSF	91337	45688	5708

3.2 Weighted Symbol Flipping Algorithm

Table 2. Bit Error Value

Input Matrix	Iteration=5	Iteration=8
N=3,M=3	2	3
N=20,M=40	3	5
N=40,M=80	8	9
N=100,M=200	26	28
N=200,M=400	32	54

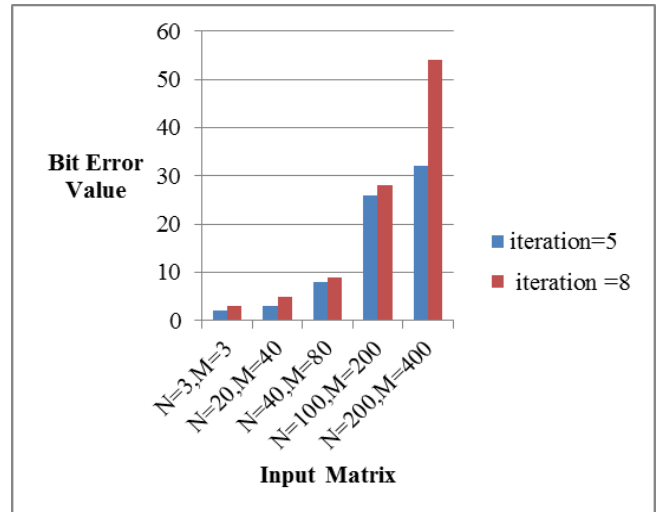


Fig 1: Bit Error Value, iteration=5 and iteration=8

Simulations results are obtained using MATLAB 2013. For various iterations the bit error value is calculated using WSF algorithm.

3.3 BER and FER Performance Analysis of HWSF Algorithm for Nonbinary LDPC Code

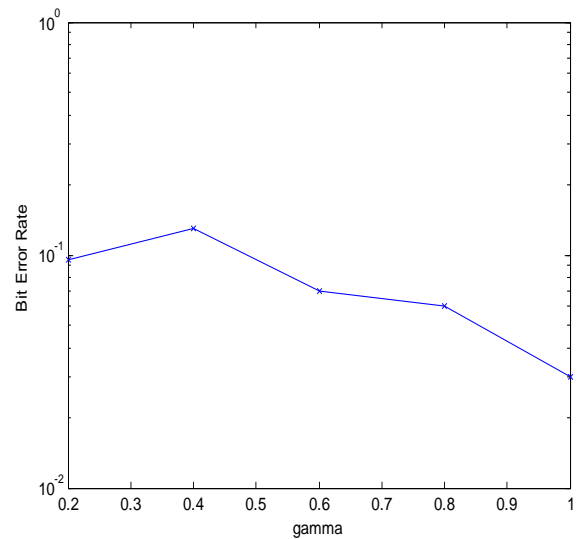


Fig 2: Weighting factor γ in HWSF algorithm for Nonbinary LDPC code, Iteration=10

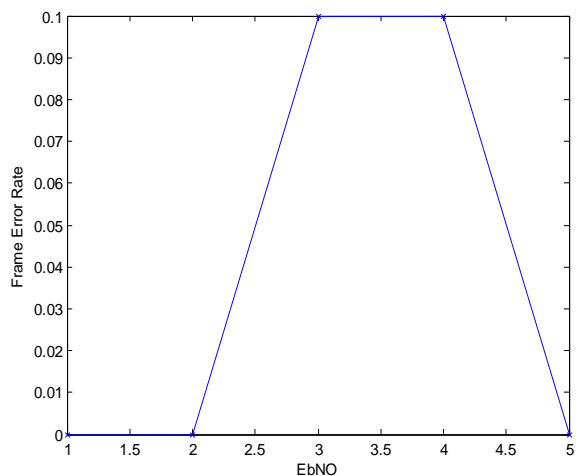


Fig 3: FER performance of HWSF algorithm for Nonbinary LDPC code, Iteration=10

In Fig.2 the bit error rate or bit error ratio (BER) is the number of bit errors divided by the total number of transferred bits during a studied time interval [13]. Ratio of data received with errors to total data received. Used to determine the quality of a signal connection in Fig.3. Small packets has low packet error rate, high packetization overhead, large packets has high packet error rate, low overhead [14]. It depends on bit error rate, energy consumption per transmitted bit.

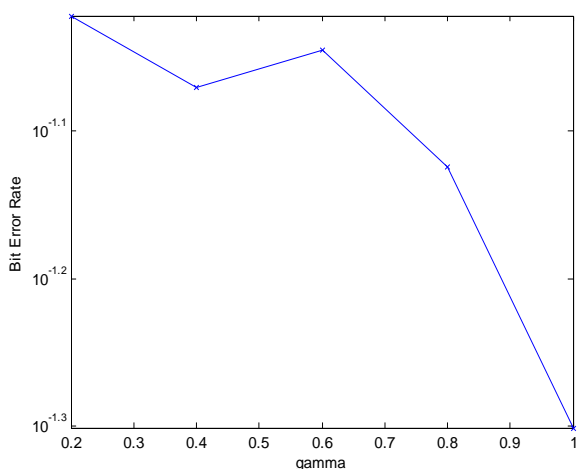


Fig 4: BER performance of HWSF with SNR=20

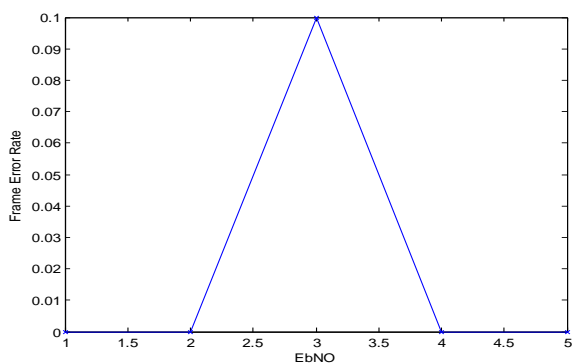


Fig 5: FER performance of HWSF with SNR=20

3.4 Simulation Results for Binary LDPC Code

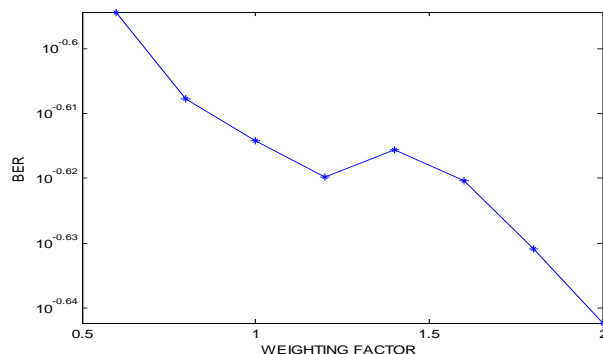


Fig 6: Weighting factor γ in HWSF algorithm for FF LDPC code

Simulation results for binary LDPC code are obtained using MATLAB 2013. All the simulations are conducted over an AWGN channel with BPSK modulation. The maximum no of iterations is chosen to be 200 for the WSF algorithm. Assume that the weighting factor γ keeps constant for all iterations [15].The effect of γ on the BER of the 16-ary (510, 1020) FF LDPC code.

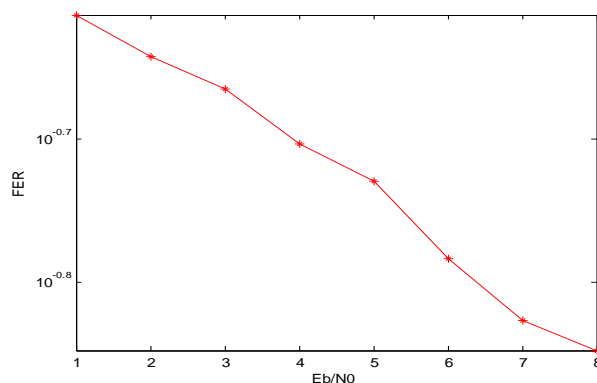


Fig 7: FER performance of HWSF algorithm for FF LDPC code

Consider the 16 ary (510, 1020) regular cyclic Euclidean geometry (EG) LDPC code over $GF(2^9)$.

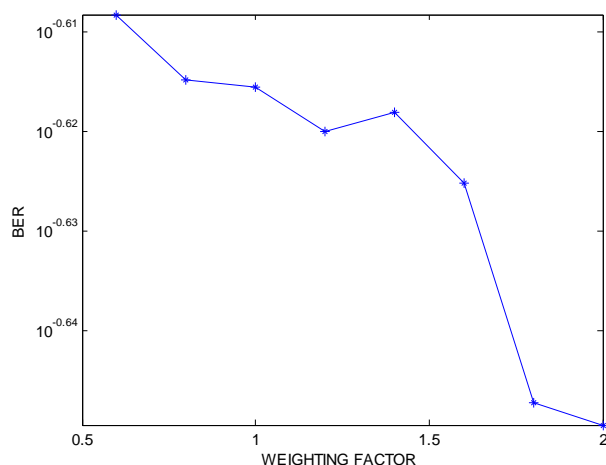


Fig 8: Weighting factor γ in HWSF algorithm for EG LDPC code

In Fig.7 the performance of this code decoded with the proposed HWSF algorithm (150 iterations for the first stage and 50 iterations for the second stage). For comparison, the performances of the FFT-QSPA and WSF algorithm with 50 iterations are used [16]. The proposed HWSF algorithm is approximately 0.11dB inferior to FFT-QSPA and also HWSF algorithm converges faster than the WSF algorithm at low SNRs. And it performs no coding gain loss from FFT-QSPA with 50 iterations [17]. The specific complexity depends on the number of iterations and the operations per iteration. The global complexities of HWSF are lower than that of FFT-QSPA.

From the simulations results HWSF decoding algorithm itself presents a good performance with are reduced complexity originated from WSF.

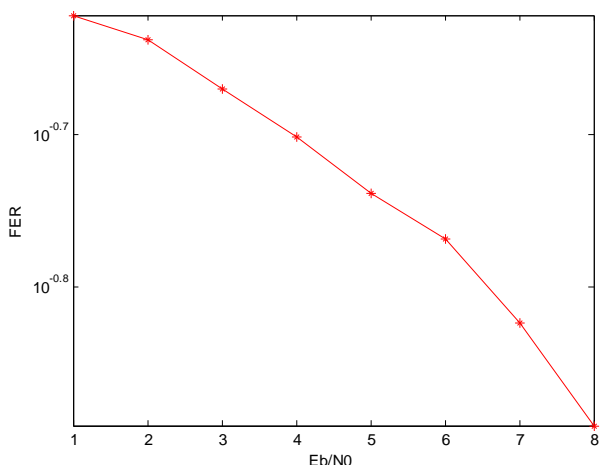


Fig 9: FER performance of HWSF algorithm for EG LDPC code

3.5 Comparison results for Nonbinary and Binary LDPC Code

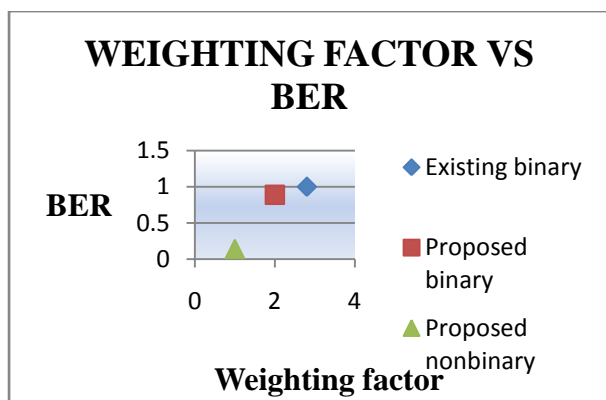


Fig 10: Comparison result for BER in Nonbinary and Binary LDPC code

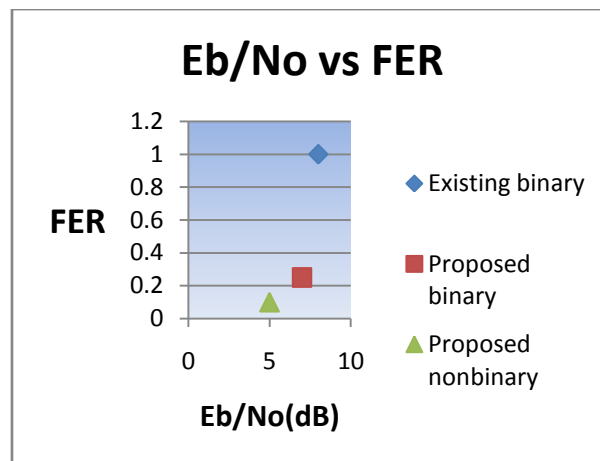


Fig 11: Comparison result for FER in Nonbinary and Binary LDPC code

Comparison results of Nonbinary and Binary LDPC code shows the reduction in BER and FER computation.

4. RESULTS AND DISCUSSION

The proposed method combines with the weighted symbol flipping algorithm and fast Fourier transform q-ary sum product algorithm. By combining those algorithms the complexity is reduced in Hybrid Weighted symbol flipping algorithm. If medium between transmitter and receiver is good i.e. if message is send from transmitter to receiver, signal to noise ratio (SNR) is high then Bit error rate (BER) is very small. E_b/N_o maintains the same average error rate as in coherent BPSK system, so probability of error (POE) is smaller. The value of γ at given SNR is used for which the algorithm generates smallest BER for decoding nonbinary LDPC codes. Some conclusions are reached on the choices of γ by the above simulations in Fig.6 and Fig.8. (1) the degradation of the performance is relatively small with different γ at low SNRs;(2) the optimal value of γ decreases slowly as the SNR increases. The optimal choice of given γ at each SNR is determined through simulation. It is observed that at lower SNRs, the error rate is less sensitive to the value of γ . But in this case if no of iteration is increased; BER is increased as well as FER is decreased.

5. CONCLUSION

A two stage hybrid decoding algorithm HWSF is proposed, which combines WSF algorithm and the existing FFT-QSPA for Nonbinary and Binary LDPC codes. The usage of bit flipping algorithm removes the need for global minimum, instead using bit local operations. Simulation results show that the HWSF can achieve better error performance and also has lower computation complexity. This distinct advantage makes it is used for high speed, low power consumption equipment's. Future work will look at improving performance of the HWSF algorithm with lowest number of iterations for decoding nonbinary LDPC code and also LDPC code can be used as a FPGA implementation using hardware kit.

6. REFERENCES

- [1] Davey M C, Mackay D, “Low density parity check over GF(q)”, IEEE Communication Letters, 1998, 2(6):165-167.
- [2] Chen C, Bai B M, Wang X M, et al, “Nonbinary LDPC Codes Constructed Based on a Cyclic MDS Code and a Low Complexity Nonbinary Message-passing Decoding Algorithm”, IEEE Communication Letters, 2010,14(3):239-241.
- [3] Li J, Zhang X D, “Hybrid Iterative Decoding for Low Density Parity Check Codes Based on Finite Geometries”, IEEE Communication Letters. 2008, 12(1):29-31.
- [4] Liu B, Dou G Q, Tao W, et al, “Efficient Stopping Criterion for Hybrid Weighted Symbol Flipping Decoding of Nonbinary LDPC Codes,” IEEE Communication Letters, 2011, 15(3):337-339.
- [5] Mohamed Ismail, Justin Coon, Imran Ahmed, Simon Armour, Joseph McGeehan, “Turbo Adaptive Threshold Bit Flipping for LDPC Decoding”, IEEE Wireless communications letters, vol. 2 no. 1, February 2013.
- [6] Chen Qian, Weilong Lei, Zhaocheng Wang, “Low Complexity Decoder With Modified Sum-Product Algorithm”, Tsinghua Science and Technology pp57-61 Volume 18, number 1, February 2013.
- [7] Chao-Cheng Huang, Chi-Jen Wu, Chao-Yu Chen, Chi-chao Chao, “Parallel Symbol-Flipping Decoding for Non-Binary LDPC Codes”, IEEE communications letters, vol. 17, no. 6, June 2013.
- [8] Song SM, Zhou s, et al, “A Unified Approach to the Construction of Binary and Nonbinary Quasi-Cyclic LDPC Codes Based on Finite Fields”, IEEE Transactions Communications, 2009, 57(1):84-93.
- [9] Bo Zhou, Jingyu Kang, Ying Yu Tai, “High Performance Non-Binary Quasi-Cyclic LDPC Codes on Euclidean Geometries”, IEEE Transactions On Communications, vol. 57, no. 5, May 2009.
- [10] Juntan Zhang, Jonathan S. Yedidia, and Marc P. C. Fossorier, “Low-Latency Decoding of EG LDPC Codes”, Journal Of Light wave Technology, vol. 25, no. 9, September 2007.
- [11] Chen C Y, Huang Q, Chao c, et al, “Two Low Complexity Reliability-Based Message-Passing Algorithms for Decoding Nonbinary LDPC Codes”, IEEE Transactions on Communications, 2010, 58(11):3140- 3147.
- [12] Declercq D, Fossorier M, “Decoding algorithms for nonbinary LDPC Codes over GF (q)”, IEEE Transactions on Communications, 2007, 55(4):633-643.
- [13] Zeng L Q, LAN L, Tai Y Y, et al, “Construction of Nonbinary Cyclic, Quasi-Cyclic and Regular LDPC Codes: a Finite Geometry Approach”, IEEE Transactions on communications, 2008, 56(3):378387.
- [14] Chung-Li Wang, Xiaoheng Chen, Zongwang Li, Shaohua Yang, “A Simplified MinSum Decoding Algorithm for Nonbinary LDPC Codes”, IEEE Transactions on communications, vol. 61, no. 1, January 2013.
- [15] Gabi Sarkis, Saied Hemati, and Warren J. Gross, “Stochastic Decoding of LDPC Codes over GF(q)”, IEEE Transactions on Communications, vol. 61, no. 3, March 2013.
- [16] Liu Haiyang, MA Lianrong, Chen Jie, “Multistep Linear Programming Approaches for Decoding Low-Density Parity Check codes”, Tsinghua Science and Technology Volume 14, Number 5, October 2009.
- [17] Francisco Garcia-Herrero, and Mark F. Flanagan, “Serial Symbol-Reliability Based Algorithm for Decoding Non-Binary LDPC Codes”, IEEE Communications Letters, vol. 16, no. 6, June 2012.