An Efficient System On-Chip Interconnect using Modified Smart Bias Circuit -2014

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ABSTRACT
The most promising scheme for high-speed low power communication over long on-chip interconnects is Current-mode signaling (CMS) with dynamic overdriving scheme. A variation tolerant dynamic overdriving CMS scheme is proposed. The proposed CMS scheme employs a smart bias circuit in transmitter side. The smart bias is energy efficient and it reduces the delay. Current-mode signaling (CMS) scheme improves speed and reduces dynamic power consumption and it overcomes the drawback of voltage mode signaling. Although it consumes static power, it has a direct tradeoff between speed and static power. As the rise and fall delay is equal thereby it increases the throughput. However the voltage swing is decreased, the noise margin of data communication system get reduced. Dynamic over-driving is adopted for variation analysis which improves the energy, delay and EDP value over voltage mode signaling scheme.

Keywords:
Current Mode Circuit, Dynamic Over-Driving, On Chip-Global Interconnects, Modified Smart Bias.

1. INTRODUCTION
The most promising scheme for high-speed low power communication over long on-chip interconnects is Current-mode signaling (CMS) with dynamic overdriving. An On-Chip Communication Network (OCCN), also known as an On-Chip Network (OCN), is the entire interconnect fabric for a SOC. Voltage-mode circuits often use higher loop gains than current-mode circuits, and thus the CMS circuits are often made less complex than the voltage-mode circuit. Current mode signaling is considered to be faster compared to voltage mode signaling. The CMS have potential for reaching low delay, lower power consumption and smaller area.

Our proposed CMS bias scheme is implemented in 180nm CMOS technology. However the proposed CMS bias circuit consumes static power and exhibit a direct tradeoff between speed and static power. Dynamic overdriving is adopted for variation analysis. At times of transition high voltage and high voltage swing is produced, so to maintain 0/1 at a particular state, the voltage swing should be reduced. This can be achieved through dynamic overdriving scheme. However CMS-bias scheme reduces the voltage swing of the line, it reduces the noise margin of data communication.

In advanced CMOS technologies speed and power consumption plays major role of on-chip interconnect network Many alternate buffers repeaters and signaling schemes were developed in recent past years to achieve high-speed low-power communication over a long on-chip interconnect [2]-[12]. The current mode signaling scheme eliminates the drawbacks of previous schemes at the same time it increases the speed and reduce the power consumption.

Current mode signaling (CMS) scheme has the potential to improve both speed and dynamic power consumption [1]. It consumes much less power compared to the improved repeater circuits (such as self-timed repeaters [5] and boosters [3]) and signaling schemes such as near speed of light communication [6] and transition-aware signaling [4] as shown in [7]. However the basic current mode signaling scheme consume static power and exhibit direct tradeoff between speed and static power [1]. Capacitively coupled driver based low swing signaling schemes are proposed in [10] and [11]. The Capacitively coupled driver based signaling scheme consumes much less energy than the basic CMS scheme [1].Further, the scheme in [11] employs a channel equalization technique, at the receiver end to improve eye opening. The dynamic overdriving scheme [8],[9] proposed produces more improvement in energy and power consumption. Hence adopted dynamic overdriving CMS scheme for variation analysis.

The transmitter and receiver circuit of the CMS scheme employs a feedback [8] in Fig.1 , which increases the delay. The Performance of the scheme proposed creates mismatches between the transistor parameter in the transmitter and receiver[8]. The dynamic overdriving CMS scheme has been proposed. The proposed scheme employs a smart bias circuit in the transmitter. The operation of the circuit does not rely on the matching of the transistor parameters of the transmitter and the receiver [1].

2. CMS-Fb SCHEME WITH DRIVER PRE-EMPHASIS TECHNIQUE
Driver pre-emphasis is the technique of supplying large current/voltage to the line during transitions of input and very small current/voltage in the steady state. The transmitter has a [8] strong driver and a weak driver. The strong driver supplies a large current to the line during transition and the weak driver provides a small steady-state current to the line. NAND and NOR gates turn on the strong driver for a short duration. The duration is controlled by a feedback inverter. The strong driver is turned off after the line voltage (at the transmitter end) VMTx crosses the switching threshold of the feedback inverter.

At the receiving end, the line voltage is held near the receiver employs a feedback which makes the line voltage (at the receiving end) VMRx swing around which is the switching threshold of inverter-amplifier. The inverter following the inverter-amplifier takes the output to CMOS logic levels.

VMTx and VMRx are to be different as transmitter and receiver are placed far apart (More than 1.5 mm). Consider a case where VMTx is less than VMRx and steady-state voltage swing on the line is less than | V MTx – VMRx |

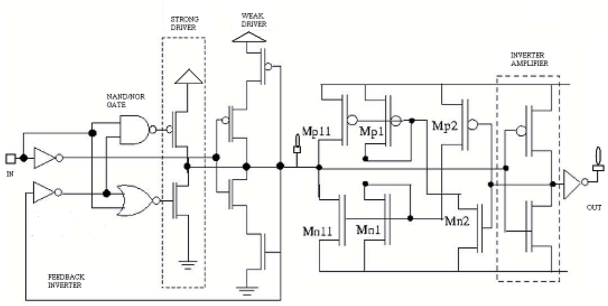


Fig 1: CMS scheme with driver pre-emphasis- CMS-Fb circuit

In this case, when input is constant "0", the receiver tries to hold the line voltage at VMRx which is more than VMTx. As a result, the strong driver is turned on to pull the line voltage below VMTx. Once the line voltage is puled below VMTx, the strong driver is turned off. However, now as the receiver is suppose to hold the line voltage at VMRx , the line voltage rises to VMRx which in turn activates strong driver. This way voltage on the line swings between and even if input is constant logic "0" .

During "0" to "1" transition in the input, the strong driver is turned off well before voltage at the receiver end has crossed VMRx . During "1" to "0", the strong driver is active even after line voltage at the transmitter end has crossed .As a result, delay of the scheme for "0" to "1" transition is more than for "1" to "0" transition. Similarly, if , V MTx > VMRx the line voltage keeps fluctuating even when input is constant at logic "1" and "1" to "0" transition is slower than "0" to "1" transition. If the steady-state voltage-swing on the line is more than the difference between V MTx and VMRx, the line voltage does not swing while the input is constant. However, the delay of the scheme during "0" to "1" and "1" to "0" transitions differ by a large amount which causes significant reduction in the throughput of the scheme.

3. PROPOSED SMART BIAS CMS SCHEME

3.1 Macro Model

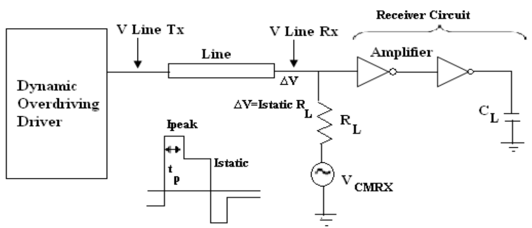


Fig 2: Macro model of dynamic overdriving CMS scheme

A macro model (Fig 2) of dynamic overdriving CMS scheme is developed to deliver the effects of different design parameters on the performance signaling schemes (see Fig.2.)[1]. The proposed CMS scheme and a existing CMS scheme (CMS-Fb) are implemented in 180-nm CMOS technology. Our analysis shows that delay of the line is a strong function of the large current supplied to the line during transition ,(I peak) the duration for which this large current is given (tp) and the voltage swing on the line ΔV = Istatic RL [1]. CMS scheme produce high throughput, for high throughput the rise and fall delay of the link should be equal. The peak current supplied by the driver during high to low and low to high should be equal.

3.2 Transmitter and Receiver Circuit

The Fig 3 shows the proposed CMS scheme (CMS-Bias) transmitter and receiver. The proposed Transmitter employs two driver(strong and weak driver) with NAND and NOR gates like in CMS –Fb scheme. In the proposed transmitter, the delay element controls the strong driver (as soon as driver turned on) but in CMS-Fb feedback controls the driver, so delay increases. The strong and weak drivers employ single transistor current sources. The proposed receiver uses a diode connected pMOS and nMOS (terminating inverter) followed by an inverter chain. The terminator inverter holds the line voltage near its switching threshold. Inverter amplifier (IA) and subsequent inverters amplify the small line voltage swing to digital logic levels.

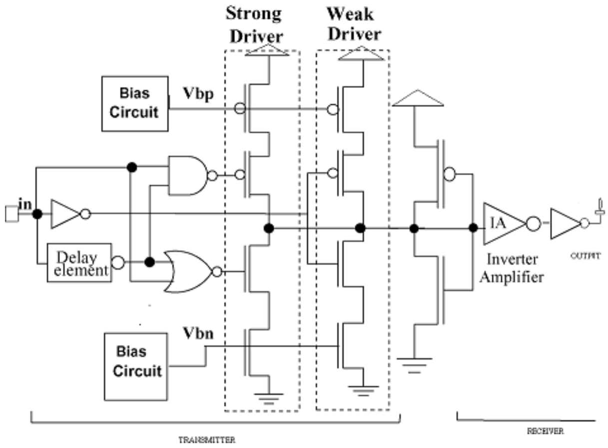


Fig.3: Proposed current-mode signaling scheme (CMS-Bias)

3.3 Bias Generation Circuits

The proposed bias circuit is derived from the various conventional bias circuits.

1. In Fig 4(a), Resistance based bias circuit. The circuit exist a direct tradeoff between area and power consumption and it works only on extreme corners.

2. In Fig 4(b), one such bias circuit is implemented in [13].Diode connected transistor based bias circuit, it employs two channel transistor ,long channel transistor act as load and short channel transistor as sensor device. Long channel transistors are less susceptible to process variation and it consumes large area.

3. In Fig 4(C), Two step compensation technique, to perform process compensation in two stages: fine and coarse compensation. In this circuit the load transistor in the final stage is the current source compensated by the coarse bias circuit.

4. In Fig 4(d), Diode connected device with extra sensor, the other solution is to employ two sensor transistors and a long channel transistor.

5. In Fig 5(a), Corner aware bias circuit, shows the final bias circuit employed in the proposed CMS scheme. Fig 5(b) shows the probability distribution function of the drain current of a transistor based bias circuit in 180-nm technology. This bias circuit produce less area and the terminating inverter in the bias circuit produce exact square wave, so the throughput increases. This bias circuit is also known as smart bias circuit.

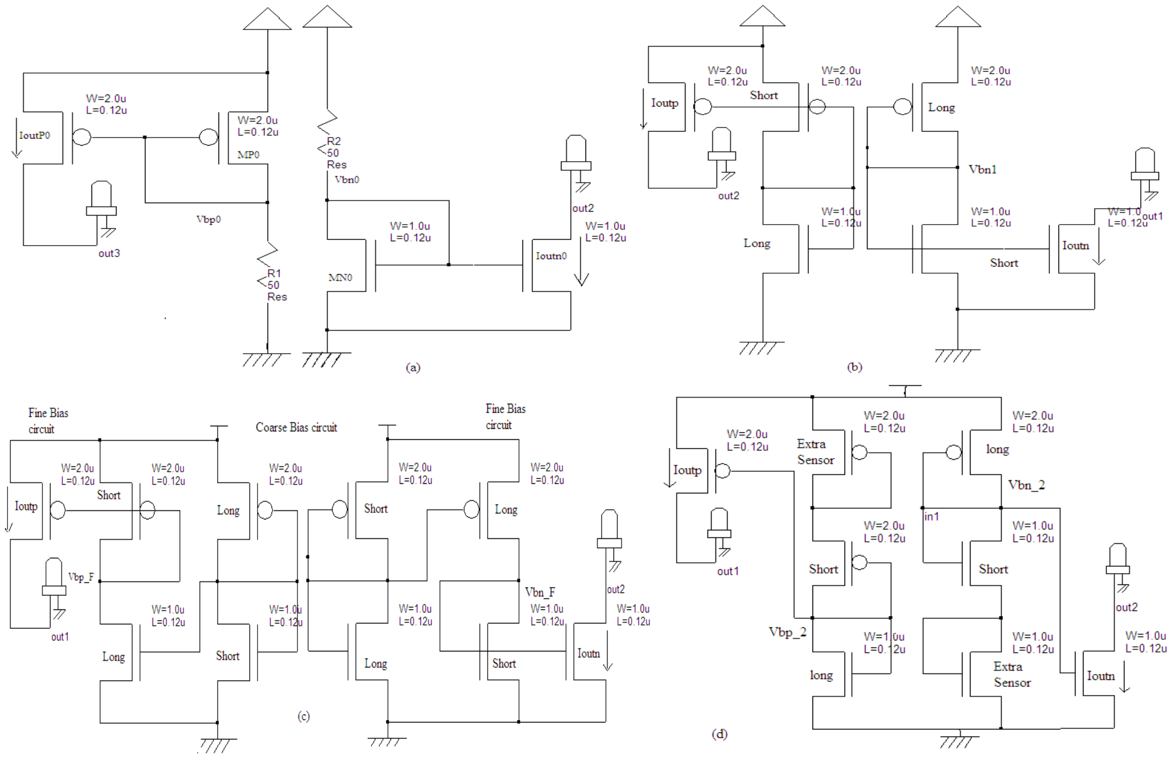


Fig. 4: Derivation of the proposed corner-aware bias circuit. a) Resistance based; b) diode-connected transistor based; c) two step (fine-coarse) compensation; d) diode-connected devices with extra sensor.

The transmitter and receiver circuits do not have any local feedback connections. As a result performance of the proposed circuit does not rely on matching of the transistor parameters between transmitter and receiver circuit. The terminating inverter and IA are designed and placed close to each other in the receiver, so that their switching thresholds are nearly the same under all process conditions [1]. The terminating inverter makes rise and fall delay of the system equal, so the throughput of the proposed system is increased. All bias circuit is been analyzed and the values is been tabulated

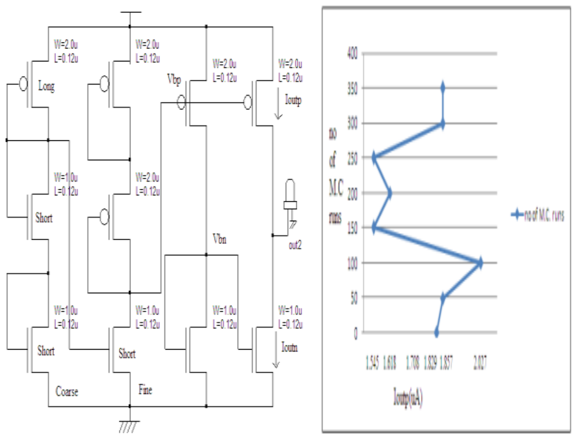


Fig 5(a) Proposed corner-aware bias circuit (b) probability density function of output curve

3.4 Scalability of the Modified Smart Bias Circuit

Design and performance of the proposed circuit in scaled down technologies are analyzed in this subsection [1]. Transmitter circuit employs digital circuits such as NAND, NOR, and inverters (in the delay element) which scale well with scaling of transistor features. It also employs switched current sources in the strong driver and weak driver [1] .Even with reduced voltage headroom and leaky switches in scaled down technologies, the strong and weak drivers can be designed with large current supplies during input transition and very small during steady-state. As long as dynamic overdriving property of the transmitter is maintained, the signaling scheme allows very high data-rates while consuming very little energy. The Receiver circuit employs inverters which scale well with technology nodes. The proposed scheme is designed in180-nm process.

4. DESIGN AND IMPLEMENTATION OF MODIFIED SMART BIAS CMS SCHEME

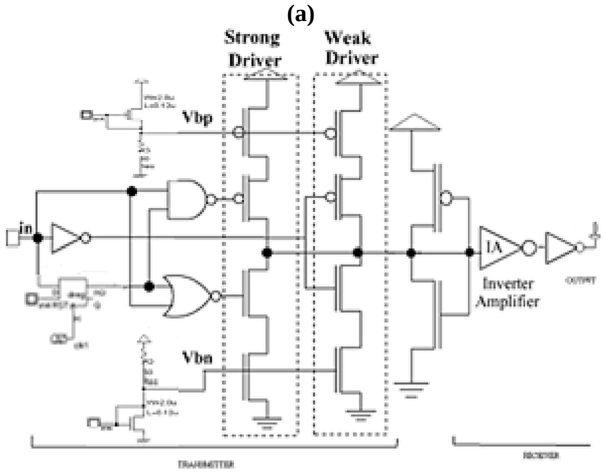
The modified smart bias CMS scheme is similar to CMS scheme with dynamic overdriving.. The proposed Transmitter employs two driver (strong and weak driver) with NAND and NOR gates like in CMS with dynamic overdriving scheme. In the proposed transmitter, the delay element controls the strong driver (as soon as driver turned on).The terminating inverter and inverter amplifier is present at the receiver end. Two modified smart bias is been implemented.

Table 1: Performance Comparison of CMS Bias circuit

PARAMETERS	RESISTANCE	DIODE CONNECT	TWO COMPENSATION	EXTRA SENSOR	CORNER AWARE
Vdd	2.5V	2.5V	2.5V	2.5V	2.5V
Power-WO.C	0.546 mv	0.936mv	1.736 mv	0.623 mv	1.572mv
Power –W.C	0.546 mv	0.936mv	1.736 mv	0.623 mv	1.574 mv
Frequency	391 MHz	391 MHz	391 MHz	391 MHz	391 MHz
Energy (pJ)	6.98 mv	3.83 mv	7.82 mv	7.26 mv	5.95 mV
Rise delay (ns)	0.68 ns	1.28 ns	2 ns	0.8 ns	1.2 ns
Fall delay (ns)	0.68 ns	1.28ns	2 ns	0.8 ns	1.2 ns
Powerdissipation	0.675mw	1.24 mw	1.6 mw	0.75 mw	1.4 mw
crosstalk	0.7 v	1.25 v	2.1 v	0.8 v	1.25 v
Final voltage	0.7 v	1.20 v	2 v	0.8 v	1.25 v
Maximum Idd	0.7 mA	1.175mA	2 mA	0.8mA	1.25 mA
No of transistor	4	6	10	8	10
EDP (pJ x ns)	4.7464	4.596	15.64	5.808	7.14

The smart bias circuit is modified by adding pmos and nmos circuit with pull down and pulls up resistance respectively and replaces the delay element as D-latch. The D- Latch is an electronic device that can be used to store one bit of information. If the data on the D changes state then the output Q since the clock pulse is high, follows the input, D to logic 0, the last state of the D input is trapped and held in the latch. And in another bias circuit terminator inverter bias circuit, But the major drawback in terminator inverter biasing is, it exhibit a direct tradeoff between power and delay while the resistance with pmos and nmos reduce both power and delay

(a)



(b)

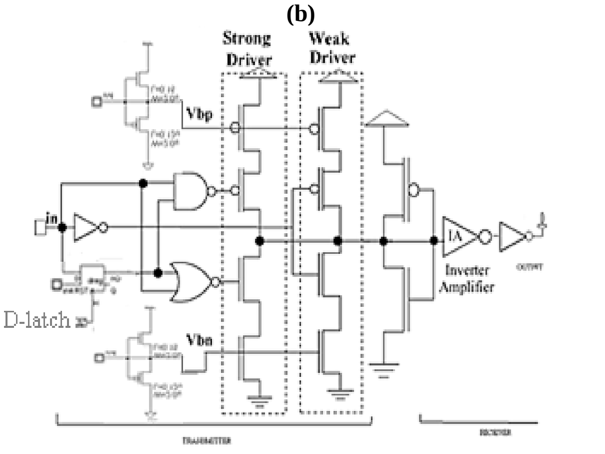


Fig 6 (a): Modified Smart Bias CMS Scheme D-latch with resistance circuit (b) Modified Smart Bias CMS Scheme with terminating inverter

5. PERFORMANCE AND COMPARISON OF CMS-Fb, SMART BIAS CMS, AND MODIFIED SMART BIAS CMS SCHEME SIMULATIONS AND RESULTS

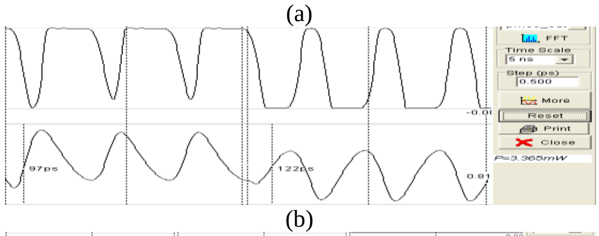
5.1 Performance in Nominal Conditions

Table 1 Summarize the performance comparison of various CMS bias circuit results. As discussed earlier compare the simulation results of various CMS bias circuit scheme. Tabulate the parametric values of various bias circuits.

Table 2 summarizes simulated results of the CMS schemes under nominal operating condition with V_{dd}=1.8V. Frequency measurements of 2 x 1 Mux-Demux based scheme show that delay of CMS-bias scheme is less that of CMS-Fb scheme.

The various Current mode signaling schemes parametric values is estimated In the CMS scheme, dynamic power consumption is much less than static power consumption. In CMS-Bias scheme inverter amplifier in the receiver and bias circuit in the transmitter consume very less static power compared to dynamic power. The transmitter of CMS-Fb scheme does not have a bias circuit but the feedback inverter consumes more power and also improves the delay. CMS-Bias scheme consumes much less energy as compared to CMS-Fb scheme but the drawback is, it consumes slightly more active area than CMS-Fb scheme.

(a)



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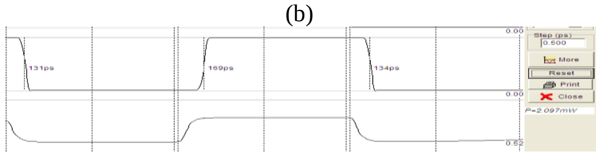

(c)

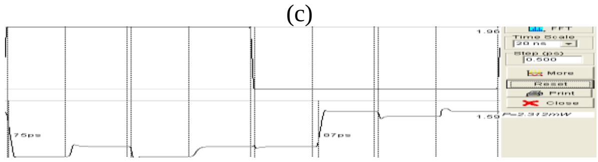

Table 2: Performance Comparison of CMS Scheme

PARAMETER	CMS-Fb SCHEME	SMART BIAS CMS SCHEME	MODIFIED SMART BIAS CMS SCHEME with resistance
Vdd	1.8V	1.8V	1.8
Power-WO.C	3.302 mw	2.097 mw	1.542 mw
Power –W.C	3.310 mw	2.109 mw	1.535mw
Frequency	33.26 GHz	5.24GHz	4.95 GHz
Energy	274.81 pJ	483.20 pJ	234.93pJ
Delay (ns)	1.17	0.819	0.146
EDP (pJ x ns)	321.52	395.74	34.299
Rise delay	0.585	0.409 ns	0.073 ns
Fall delay	0.585	0.409 ns	0.0.73ns
Power dissipation	1.603mw	1.996mw	1.477 mW
Crosstalk	32000V	32000V	32000V
Final voltage	1.047 V	0.021 V	1.465 V
Maximum Idd	1.429mA	2.635 mA	1.468mA
Number of transistors	14	20	12

(d)

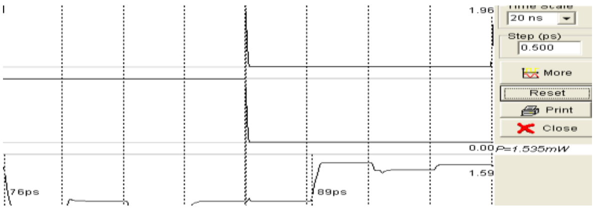

Fig 7. Waveform Of Power And Delay Analysis Of (A) CMS-Fb (B)CMS Scheme (C) Modified Smart Bias With Terminator Inverter (D) Modified Smart Bias With Resistance

6. PERFORMANCE OF THE PROPOSED CMS SCHEME IN COMPARISON WITH OTHER SIGNALING SCHEMES

Table 3: Performance of various signaling scheme

Signaling Scheme	Delay (ns)	Energy (pJ)	Power (mw)	No of transistors
CMS-Fb	1.17	483.15	3.302	14
CMS Smart Bias	0.819	254.81	2.097	20
CMS Modified Smart Bias (With Resistance)	0.073	234.93	1.535	12

Table 3: shows performance of recent energy-efficient signaling schemes for on-chip long wires. Energy consumption of the proposed signaling scheme (CMS-Bias) is

the lowest of all. CMS-smart Bias and modified smart bias is been implemented in 180-nm CMOS technology. As the rise and fall delay is equal the throughput increases. Thus the performance of the system also increases. The CMS smart bias scheme reduces the power consumption, reduces the delay and improves the speed.

7 APPLICATION TO IMPROVE THE CURRENT MODE SIGNALING SCHEME

7.1Delay Measurement Scheme

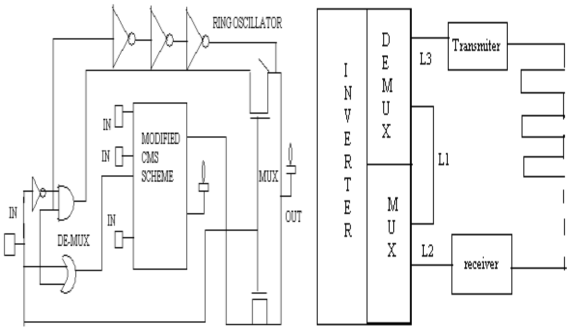

Fig 7(a): Delay Measurement Scheme Using Modified Smart Bias CMS Scheme (b) Block Diagram Of Delay Measurement Scheme

The modified smart bias CMS scheme is placed with ring oscillator via multiplexer and de-multiplexer. In this paper (4X1) Mux-Demux, is comparatively more efficient, than (4X1) Mux-Demux .since it produce absolute delay and limts the supply noise. The multiplexer (demultiplexer) exhibit the same delay for all inputs (outputs), where the delay corresponding to the multiplexer and demultiplexer get cancelled [1]. In this session, comparison of delay measurement scheme with CMS-Smart bias scheme and modified smart bias scheme is estimated. The delay measurement scheme produces tradeoff between power and delay.

Table 4: Performance of Delay Measurement Scheme

Parameters	Smart bias CMS Scheme	Modified smart bias cms scheme with resistance
Power(mW)	**1.834**	**1.188**
Delay(ns)	**4**	**8**

8. CONCLUSION

In this paper, the repeater less signaling schemes for on-chip long interconnects is determined. A dynamic overdriving with current mode signaling scheme is proposed in this paper. The proposed scheme uses a novel bias circuit (ie) modified smart bias circuit for the transmitter, based on a judicious combination of long and short channel MOSFETs [1]. Energy efficiency and power efficiency is been demonstrated in proposed CMS scheme with 180 nm CMOS technology. The proposed scheme consumes 1.590 mw power and it reduce the delay to 0.514 ns, and the area is also been reduced to 12 transistor In all cases, the proposed CMS modified smart bias scheme with resistance circuit remains faster than logic circuit with negligible compromise on the energy consumption .

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