Testable Sequential Circuits using Conservative Toffoli Gate

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ABSTRACT
Testing of Sequential circuits can be done by two test vectors (all 1's and all 0's) if the circuits were based on the conservative logic. The circuit is made to be tested by designing the circuit with the help of Reversible logic gates. Toffoli gate is used as reversible gate in this paper. Sequential circuits such as latches, flip flops are designed with the help of conservative logic reversible gate. Therefore, testing does not require any scan path access to the internal memory cell since only normal mode and test mode are required for testing. Equivalent circuit of the Toffoli gate is presented which achieves the fault coverage. The objective of this paper is to reduce the number of test vectors. Fault coverage is also achieved rather than designing the circuit with fredkin gate. Power consumption may also reduce when compared with the fredkin gate.

Keywords
Conservative logic, Reversible gate, Fredkin gate, Toffoli gate.

1. INTRODUCTION
Conservative logic is a logic family which reflects the property that there is equal number of one's in the inputs as in the outputs. It can be reversible or irreversible in nature. The Reversible logic gate is mainly preferred due to its low power dissipation. This gate exhibits the property of reversibility which is nothing but the circuit has one to one mapping between input and output vector, and also represents for each input vector there is an unique output vector and vice versa. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments

Conservative logic is said to be reversible only when the circuit possess the above property of reversibility .Otherwise, conservative logic is irreversible. Reversible logic has received great attention in the recent years due to reduced power dissipation than other logic. It has wide applications in low power CMOS design and Optical computing, DNA computing, quantum computation and nanotechnology. Due to the information loss, energy dissipation occurs in irreversible circuit computation.

Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and vice versa. Any sequential circuit can be tested by having only two test vectors (all 1's and all 0's) when the circuit is based on conservative logic. It has the advantage of eliminating the scan path access to the internal memory cell. The designs of latches, flip flops are presented based on reversible conservative logic gate.

There are number of existing reversible logic gates such as Fredkin gate, Feynman gate, Peres gate, Toffoli gate. Fredkin gate is used for designing such testable sequential circuit is presented. Thereby avoiding the usage of scan path access to the internal memory cell. Henceforth, testing time can be reduced. Testable sequential circuit can have normal mode and test mode. In the normal mode, the circuit will have feedback but in the test mode, the circuit is made as suitable by disrupting the feedback. So, the circuit is to be tested by only two test vectors (0's and 1's).

This paper involves: Section 2 represent the background dealt with this paper. Section 3 represents testable sequential circuits such as reversible gate based latch and reversible gate based flip flops. Section 4 tabulates the comparison of toffoli gate with fredkin gate. Section 5 shows the simulation results and Section 6 represents the conclusion.

In addition, QCA is one of the emerging nanotechnologies which exhibits the low power compared to CMOS. Equivalent circuit is used instead of QCA designer to improve the fault coverage than fredkin gate. This circuit consists of logical devices – Majority Voter (MV), Cross Wire (CW), Inverter (INV), LShapedWire (LSW), Fan Out (FO). These are basic devices, each of which having its own property. FO of the toffoli gate is 2 which means that output is drawn by two ways to other logical device whereas the Majority voter choose the majority of the inputs as its output. INV inverts the input in the absence of fault. LSW just pass the value from one logical device into other and finally, CW also performs the passage of 0's and 1's from one device into another.

2. BACKGROUND
2.1 Reversible Fredkin Gate
Reversible gate is a logical gate with one-to-one mapping i.e., for each input vector, there is a unique output vector and vice versa. Also known as reversible conservative logic. Fanout at the output is not allowed. The designs presented in this paper are based on conservative reversible (three inputs: three outputs) Fredkin gate shown it can be described as mapping (*A,B*, and *C*) to (*P* = *A,Q* = AB + AC, and *R* = AB + AC),where *A,B*, and *C* are the inputs, and *P,Q*, and *R* are the outputs, respectively.

The operation involves: Whenever the first input (say A) is 1, the swapping of inputs B and C is done at the output. Otherwise, output is same as input. This logic gate possess 6 majority voters

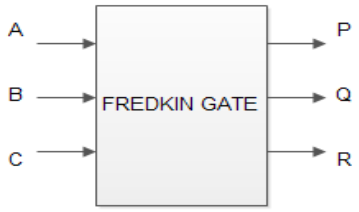


Figure 1: Fredkin gate

2.2 Reversible Toffoli Gate

The Sequential circuits are designed using the fredkin gate achieves only the limited fault coverage. In order to improve that Toffoli gate is a universal gate, also known as controlled-controlled-not gate is used. It has 3 inputs and 3 outputs. The operation of the toffoli gate involves: If the first two bits say A and B are 1, this gate inverts the third bit. Otherwise, output remains the same as inputs. It requires the MVof 2 , FO of 2, LSW of 4, CSW of 2. INV is not required. Swapping of inputs are not done for the outputs. Table I shows the truth table of Toffoli gate, and it can be seen tha this gate produces the output as in the inputs only when the first two bits are set to 1. in addition, it preserves the one-to-one mapping feature of reversibility.

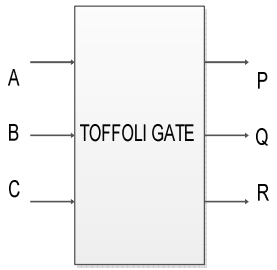


Figure 2: Toffoli gate

2.2 Conservative Logic

A conservative logic gate is any Boolean function that is invertible and conservative. The property of conservative logic is that the number of one's in the inputs is equal to the number of one's in the outputs. It is well known that, under the ordinary rules of function composition (where fan-out is allowed), the two-input NAND gate constitutes a universal primitive for the set of all Boolean functions.

In conservative logic, an analogous role is played by a single signal-processing primitive, namely, the toffoli gate, defined by the truth table 1. In the case of toffoli gate, the number of one's in each input is equal to that of the number of one's in each output.

Table 1: Truth table of toffoli gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

This computing element can be visualized as a device that performs conditional crossover of two data signals as one. otherwise, the same input is reflected to the output.

3. SEQUENTIAL CIRCUITS USING CONSERVATIVE TOFFOLI GATE: LATCHES AND FLIP FLOPS

The sequential circuits are made suitable to be tested by only two test vectors with the help of conservative toffoli gate [5]. Therefore the circuit is suitable for testing thereby scan path access is not required and testing time is reduced. Sequential circuits such as Latches and flip flop (DET flip flop and Master-Slave flip flop) are considered.

3.1 Reversible Gate based D Latch

Latch is the basic element used to store the data in digital design. Sequential circuits are mainly preferred mainly because of its memory. D latch is considered in this paper, designed by using reversible gate say the toffoli gate rather than fredkin gate and tested by all zero's and all one's shown in the figure 2. This is coded in verilogHDL. This circuit involves normal mode and test mode.

In the Normal mode, control signals (say C1 and C2) are set to 01.Then the sequential circuit will operate as D latch without any fan-out problem. Test mode involves control signals which are set to C1C2=00(all 0's).So that the design can be tested with the respective vector. Thus stuck at 1 fault can be detected. It is same as that for the stuck at 0 faults to be detected; both the C1 and C2 are set to 11. Then the design will disrupt the feedback in test mode and take care of the fanout.

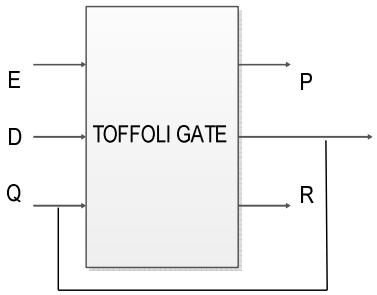


Figure 3: Reversible gate based D Latch.

The Reversible gate based circuit with the respective control signals are shown in the figure 3,4,5. Unidirectional stuck at fault are then detected. These two test vectors are long enough to detect all faults present in the circuit.

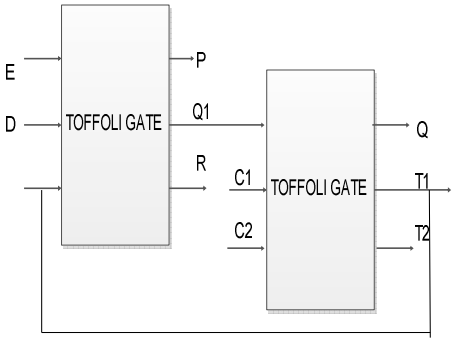


Figure 4: Design under normal mode

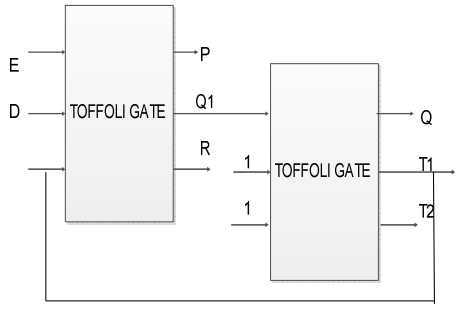


Figure 5: In test mode by passing test vector of all 1's

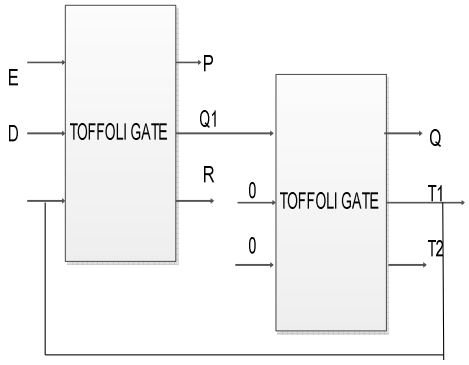


Figure 6: In test mode by passing test vector of all 0's

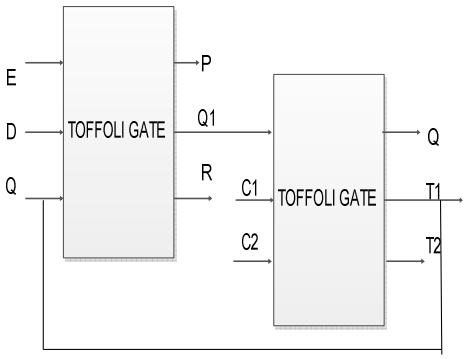


Figure 7: Negative enable toffoli gate based D latch

The negative enable D latch is also coded and tested by using the test vectors. It is illustrated in the figure 6.This latch is activated only when the enable is negative or E=0.In this design, the second toffoli gate will take care out of the fan out and the design can be tested.

3.2 Reversible Gate based Master slave D Flip Flop

Flipflop is another storage element used to store one bit of information. The only difference between latch and flip flop is that enable signal. Flip flops such as Master-slave flip flop and DET flipflop are considered to design the testable sequential circuits toffoli gate is used in order to make the design to be tested by two test vectors. Like the Reversible gate based D latch, this design consists of normal mode and test mode.

Hence the faults are detected and the testing time is reduced rather than the designs are tested using the scan path. For the Master slave D flip flop, the figure 7 represents consist of Positive enable D latch acts as master and slave where the negative enable D latch is acts as slave. The control signals mc1, mc2, sc1 and sc2 are set to 01. The control signals are set to 01 for the normal mode.

In the test mode, all the stuck at 0 fault can be detected by setting the control signals(mc1,mc2,sc1,sc2) to 1111.Likewise, all the stuck at 1 fault can be detected by passing the test vector of all zeros (i.e.)0000.D flipflop is considered for this design because the output is preserved from its input.

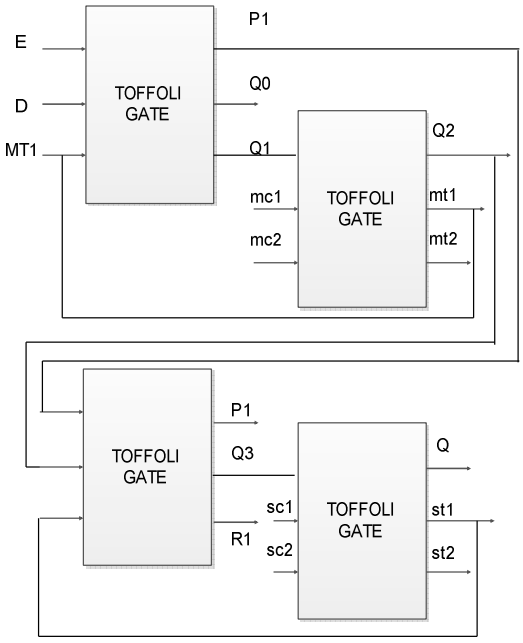


Figure 8: Reversible gate based Master slave D flipflop

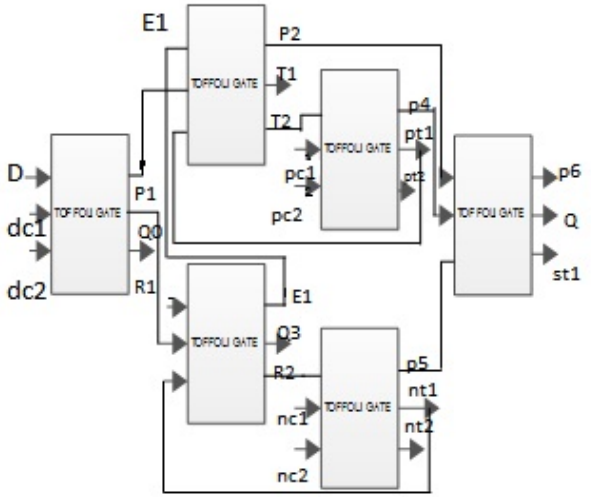


Figure 9: Reversible gate based DET flipflop

The wholesome design can be implemented using the toffoli gate since it is a reversible gate. The reason is that reversible gate exhibits low power dissipation compared to the CMOS. Both the test vectors 0000 and 1111 will break the feedback in the test mode.

3.3 Reversible Gate based DET Flip Flop

The above design method is same as that for designing the DET flipflop which is coded and simulated. In the Master slave flipflop, the sampling and storing the input data at both positive and negative edges (the rising and the falling edge) of the clock cannot be possible. In order to overcome this, DET

flipflop is used (illustrated below). The advantage of this design is that the data rate can be maintained and frequency is reduced to half when compared with the master slave flipflop.This design is illustrated above(figure 8). The design consists of positive enable and negative enable flipflop along with the 2:1 mux at the output to pick one of the results from the design. Both the positive enable flipflop, negative enable flipflop are in parallel but the fan out is not allowed since it is reversible and control signals such as pc1,pc2,nc1,nc2. The same procedure is applied for the test mode and normal mode.

In addition, the equivalent circuit for toffoli gate is designed to improve the fault coverage. Instead of using the QCA designer, this circuit is designed and coded in order to avoid single/missing cell defects. It requires only 2 majon rity voters,4 LSW,CSW's, 2 FO and no need of inverter. It acquires less area because of reduced logical devices. Thereby, power consumption may be reduced to some extent.

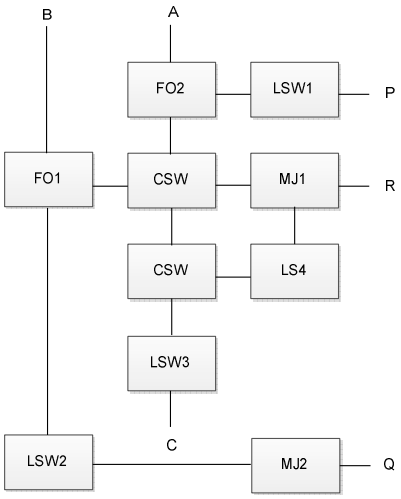


Figure 10: Equivalent circuit of toffoli gate

4. COMPARISON OF TOFFOLI GATE WITH FREDKIN GATE

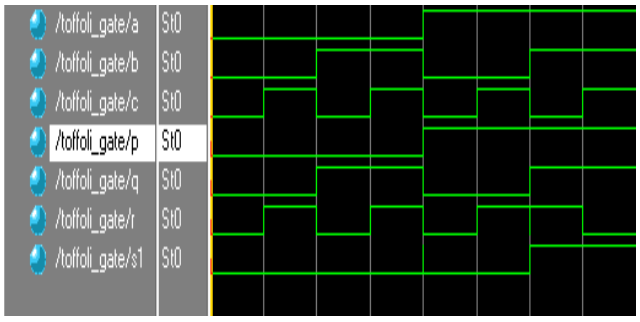
The toffoli gate is preferred since it has the advantage of having 2 majority voters and swapping is not required. Therefore power drawn may be reduced when compared to fredkin gate. Since only two test vectors are used in this case, testing time can be reduced.

The following table shows that the comparison between toffoli gate and fredkin gate.

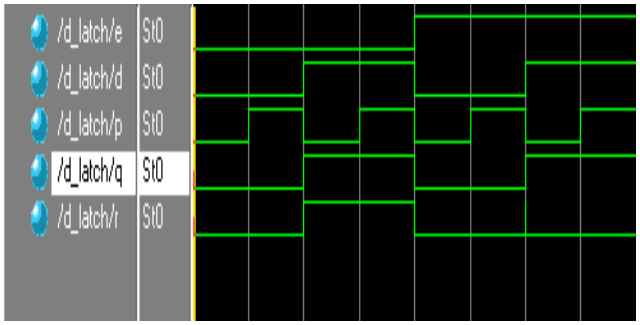
Table 2. Fredkin gate Vs Toffoli gate

Parameters	Fredkin gate	Toffoli gate
MJs	2	6
Total cells	246	216
Fault coverage	62%	Improved to 74%

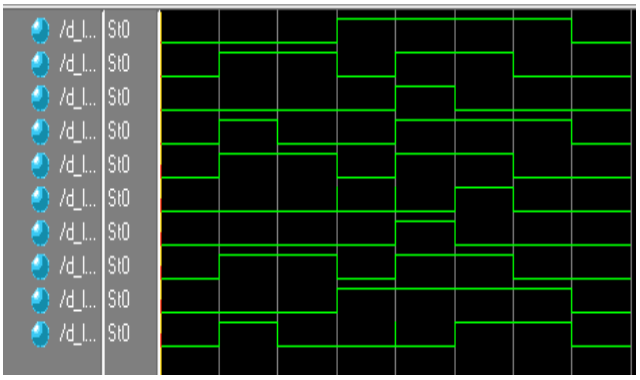
5. SIMULATION RESULTS



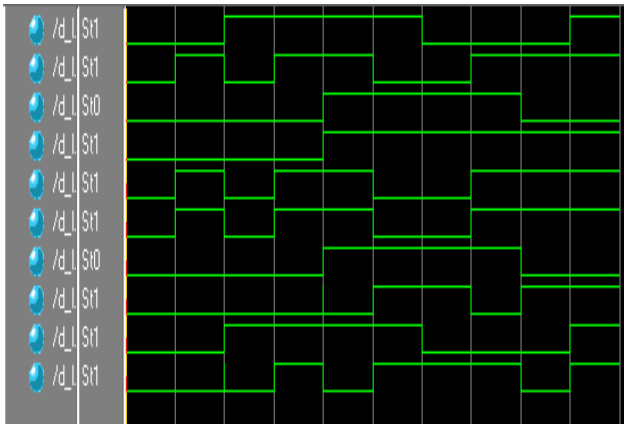
Toffoli gate



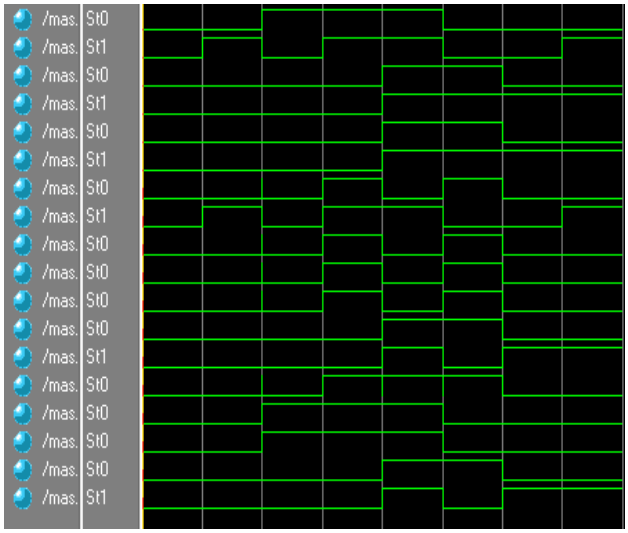
Toffoli gate based D latch



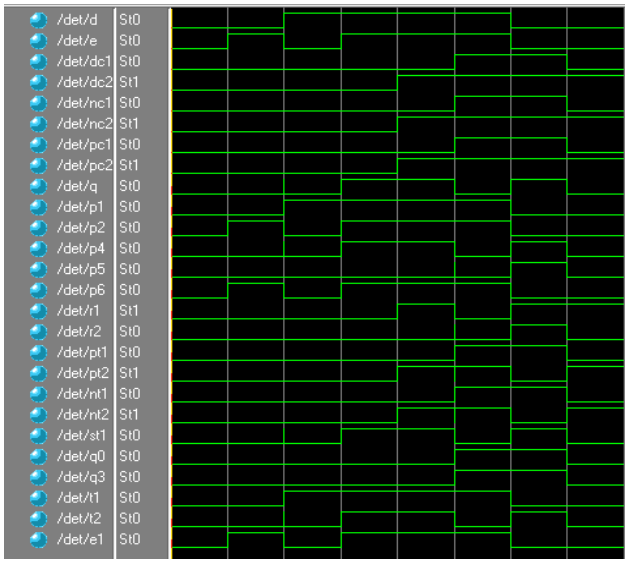
Toffoli gate based D latch with controlled inputs



Toffoli gate based negative enable D latch



Toffoli gate based master slave D flipflop



Toffoli gate based DET flipflop

6. CONCLUSION

Sequential circuits are basically used for testing. Instead of scan path access to the internal memory cell, the circuits are designed by the reversible gate especially toffoli gate instead of fredkin gate. The designs of reversible gate based latch, flipflop are made. Since those circuits are based on conservative logic and the circuits are made to be changed by reversible gates, the entire design can detect all possible stuck at 1 fault that can be found by having test vector of all zero whereas all possible stuck at zero fault can be found by all ones. Thereby, testing time may be reduced to some extent. Fault coverage and low power is achieved. Table 2 shows the comparison of the gates and shows an improvement in Fault coverage and reduction in area. Thus testing time is reduced.

7. REFERENCES

[1] E. Fredkin and T. Toffoli, "Conservative logic," *Int. J. Theor. Phys.*,vol. 21, nos. 3–4, pp. 219–253, 1982.

[2] Himanshu Thapliyal and Saurabh Kotiyal,"Design of testable reversible sequential circuits", IEEE Transaction on very large scale integration systems., vol. 21, no. 7, july 2013.

[3] sk.noor mahammad and kamakoti veezhinathan ," constructing online testable circuitsusing reversible logic, IEEE transactions on instrumentation and measurement, vol. 59, no. 1, january 2010.

[4] H. Thapliyal and N. Ranganathan, "Design of reversible sequential circuits optimizing quantum cost, delay and garbage outputs," acm j. emerg. technol. comput. syst., vol. 6, no. 4, pp. 14:1–14:35, dec. 2010.

[5] Himanshu Thapliyal and Nagarajan Ranganathan," design of reversible sequential circuits optimizing quantum cost, delay, and garbage outputs"

[6] Jie Ren and Vasili K. Semenov,progress with physically and logically reversible superconducting digital circuits, IEEE transactions on applied superconductivity, vol. 21, no. 3, june 2011

[7] Design, synthesis and test of reversible circuits for emerging nanotechnologies, vlsi (isvlsi), 2012 ieee computer society annual symposium.

[8] M. Hasan, A. Islam, and A. Chowdhury, "Design and analysis of online testability of reversible sequential circuits," in Proc. Int. Conf. Comput.Inf. Technol., Dec. 2009, pp. 180–185.

[9] M. Pedram, Q. Wu, and X. Wu, "A new design for double edge triggeredflip-flops," in Proc. Asia South Pacific Design Autom. Conf., 1998, pp. 417–421.

[10] H. Thapliyal, M. B. Srinivas, and M. Zwolinski, "A beginning in the reversible logic synthesis of sequential circuits," in Proc. Int. Conf.

[11] Military Aerosp. Program. Logic Devices, Washington, DC, Sep. 2005, pp. 1–5.

[12] P. Kartschoke, "Implementation issues in conservative logic networks," M.S. thesis, Dept. Electr. Eng., Univ. Virginia, Charlottesville, 1992.

[13] J. Ren and V. K. Semenov, "Progress with physically and logically reversible superconducting digital circuits," IEEE Trans. Appl. Superconduct., vol. 21, no. 3, pp. 780–786, Jun. 2011.

[14] Md. Saiful Islam, "A Novel Quantum cost efficient reversible full adder in nanotechnology".

[15] Prashant. R. Yelekar, Prof. Sujata S.Chiwande "Introducton to reversible logic gates and its application" in National Conf, 2011.

[16] Sujata S. Chiwande, Shipa S.Katre, Sushmita S.Dalvi, Jyoti C Kolte, "Performance analysis of sequential circuits using reversible logic", Int journal, vol. 2,Issue 1 ,Jan 2013.

[17] Raghava Garipelly, P.Madhu kiran, A.Santhosh "A review on reversible logic gates and its implementation",Int Journal,vol.3, Issue 3, Mar 2013.

[18] Himanshu Thapliyal, Nagarajan ranganathan,"Design of reversible sequential circuits optimizing quantum cost, delay, and garbage outputs".