Impact of Fin Shape on FINFET Performance

Jyothi A
Student
College of Engineering
Chengannur
Alappuzha
Kerala, India

T E Ayoob Khan
Associate Professor
Electronics Department
College of Engineering
Chengannur
Alappuzha
Kerala, India

Nisha Kuruvilla, PhD
Electronics Department
College of Engineering
Chengannur
Alappuzha
Kerala, India

Shahul Hameed T A, PhD
Associate Professor
Electronics Department
TKM College of Engineering
Kollam
Kerala, India

ABSTRACT
FinFET has been a proven modification of the classical structure of MOSFETs to overcome short channel effect. But the leakage current due to corner effect in trigate FinFET posed impediments in its way. Fin cross section shape of FinFET has considerable impact on leakage performance. In this paper trapezium and inverse trapezium PC FinFETs with various top and bottom width of fin are studied. Results show that rounding the corner and tapering the fin reduce the leakage and improves I_{on}/I_{off} ratio.

General Terms
FinFET, Leakage

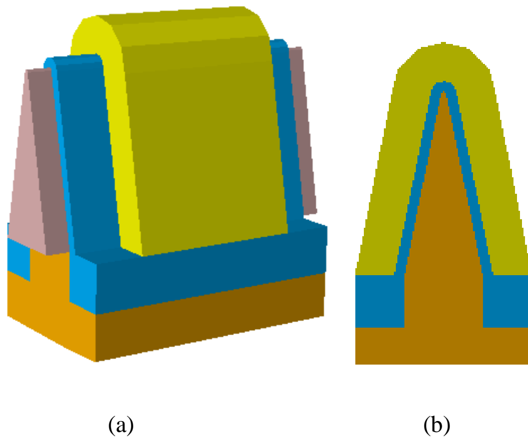
Keywords
PC-FinFET, Corner effect, Multithreshold

1. INTRODUCTION
Miniaturization has been the watchword of the electronics industry [1] for many decades which is achieved by scaling of MOSFETs. It has contributed tremendously to the growth of semiconductor industry and in fact served as the fulcrum of its unimaginable growth in recent years. The shrinkage of the feature size of the device has led to many new challenges and such effects are consummated as short channel effects (SCE) which include V_{th} roll-off, hot carrier effects, drain induced barrier lowering (DIBL), increase in subthreshold swing and leakage currents, etc. Hence there attained a point where industry has met with a stalemate with bulk devices as it was hardly possible to move further with Moore's predictions. Power consumption and process variation effects were the important limiting factors of the scaling of conventional transistors beyond 22nm. The Solution to supersede these effects demand performance boosters, like use of novel materials and non-classical device structures to continue further scaling.FinFET transistors have emerged as novel devices having superior controls over short channel effects (SCE) than the conventional MOS transistor devices[2].FinFETs which provide multithreshold circuits of very low leakage without any area overhead and no requirement of additional mask. However, FinFET exhibit certain undesirable characteristics such as corner effects, quantum effects, tunneling etc. which deteriorates the performance by increasing the leakage current [3].In Trigate FinFET the premature inversion of the corners occurs due to the charge sharing effect between two adjacent gates. This causes the formation of independent channels with different threshold voltages, explained by the phenomenon cornereffect [3] [4].The mobile carrier densityin the corner of trigate FinFET is higher than the other regions and the corner regions are comparable with the planar surface channel region in small dimension devices. A larger part of the current is carried by the corners which can switch on the device. As dimensions are decreasing the effect of corner role on On-state current is increasing and the electron density distributions at the corners are higher compared to the other portion of the channel. In fact, this deteriorates the performance. Rounding the corner has been proposed as one of the ways out and FinFET with round corners is called Partially Cylindrical FinFET (PC-FinFET) [5]. For the same channel length the top fin size for desirable on and off state performance can be optimized with the change in shape of fin from round shape corner to tapered shape fin[6]. In this paper the effect of fin shape on FinFET performance is studied by rounding and tapering the fin.The different PC FinFET structures by various fin top width and various fin bottom width are simulated and compared Threshold voltage, Subthreshold swing, I_{off} and I_{on}/I_{off} ratio.

2. DEVICE SIMULATION
As the FinFET device structure is complex, 3D device simulation is necessary. So in this work all the FinFET device structures have been simulated using 3D device simulator. All the simulations are done without considering quantum confinement and tunneling. This analysis on the 22-nm bulk nFinFET Technology Computer Aided Design (TCAD) model with key geometries given in the Table 1. below. All other model parameters take the default value unless otherwise specified.

Table 1:Key geometries of simulated structures

L	Gate Length	34nm
H	Height of the Fin	35nm
W_{bottom}	Width of the Bottom of the active fin	15nm
W_{top}	Width of the top of the active fin	15nm



(a) (b)

Fig. 1:a) Trapezium PC FinFET device structure with $W_{top=}$1nm and $W_{bottom=}$15nm b)cross section of this device.

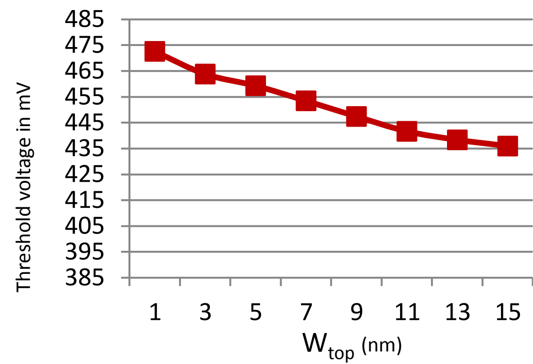
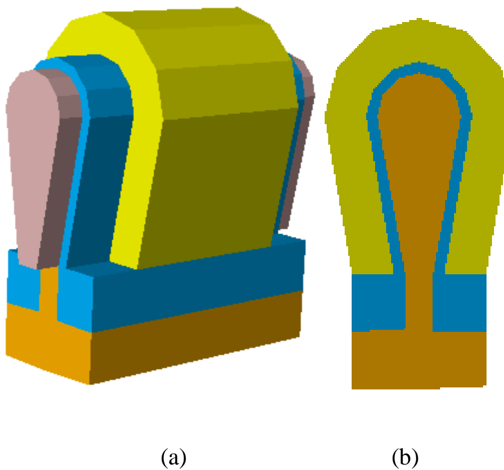


Fig. 3:Threshold voltage of Tz PC FinFET v/s W_{top}



(a) (b)

Fig. 2:a)Inverse trapezium PC FinFET device structure with $W_{top=}$15nm and $W_{bottom=}$5nm b)cross section of this device

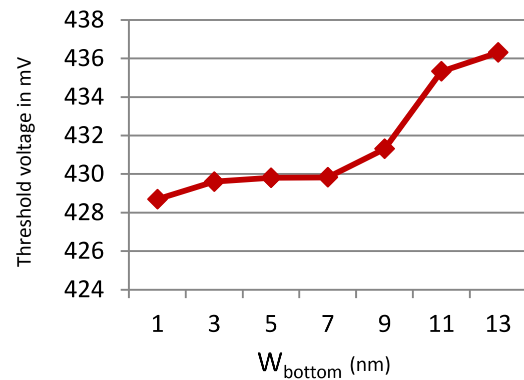


Fig. 4:Threshold voltage of inverse Tz PC FinFET v/s W_{bottom}

3. RESULT AND DISCUSSION

All the simulations are done with body doping concentration 1E18 cm^{-3} and gate work function is 4.6eV for minimizing the leakage.Here all the results are compared with PC FinFET of W_{top} = W_{bottom} =15nm. First studied the variation of threshold voltage with W_{top} and W_{bottom}.V_{th} is extracted using the maximum transconductance method with V_d=0.05 V.It is observed that threshold voltage increases when W_{top} ofTrapezium (Tz) PC FinFET decreases. Threshold voltage is within the range 435mV to 472mV when W_{top} varies from 15nm to 1nm as shown in the Figure 3. And threshold voltage decreases when W_{bottom} of inverseTz PC FinFET decreases. Threshold voltage,V_{th} is within the range 435mV to 428mV when W_{bottom} varies from 15nm to 1nm as in the Figure 4.

While observing the Subthreshold swing,SS decreases with decrease in W_{top} .The SS is extracted at a gate voltage (Vg) of 0.3 V.As in the Figure 5. sub threshold swing total range is 10mV/Dec by fin shape variation from rectangular (W_{top}=15nm) to triangular (w_{top}=1nm).Sub threshold swing is less than 92mV/Dec. Sub threshold swing also decreases with decrease in W_{bottom}. The total range of SS is 12.8mV/Dec as the W_{bottom} varies from 15nm to 1nm as in Figure 6.

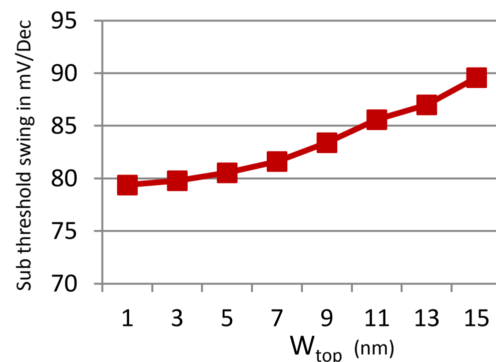


Fig. 5: Subthreshold swing of Tz PC FinFET v/s W_{top}

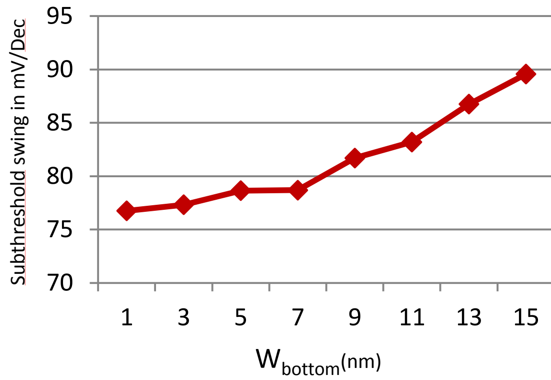


Fig. 6:Subthreshold swing of inverse Tz PC FinFET v/s W_{bottom}

Inverse trapezium PC-FinFET structure has more perimeter compared to trapezium PC-FinFET structure with same fin widths. So On current is high in Inverse trapezium PC-FinFET. The leakage current is concentrated in the middle of the fin.In trapezium PC-FinFET leakage current is concentrated in the bottom side so corner leakage current less compared to Rectangular FinFET and Inverse trapezium PC-FinFET. Reducing the top fin width enables leakage reduction. Compared to PC FinFET with W_{top}= W_{bottom}=15nm,there is 97.48% reduction in I_{off} and improved I_{on}/I_{off} ratio.The results shown in Figure 7 and Figure 9.The graph in Figure 8 and Figure 10 shows leakage current and I_{on}/I_{off} in Inverse trapezium PC-FinFET. The W_{bottom} variation from 15nm to 3nm provides 95.31% reduction at the cost of 4.7% reduction in saturation current. In triangular FinFET ($W_{top=}$1nm) PC FinFET leakage current increases due to tunneling. So Trapezium PC-FinFET gives better leakage performance.

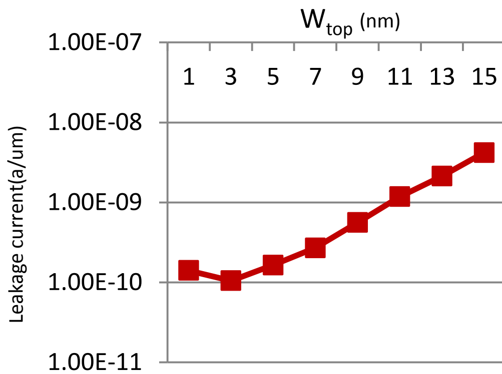


Fig. 7:Leakage Current ofTz PC FinFET v/s W_{top}

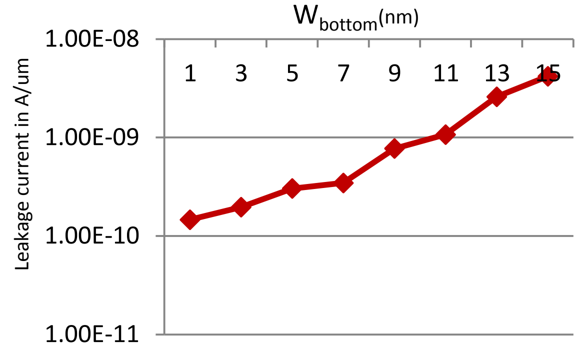


Fig. 8: Leakage Current of inverse Tz PC FinFET v/s W_{bottom}

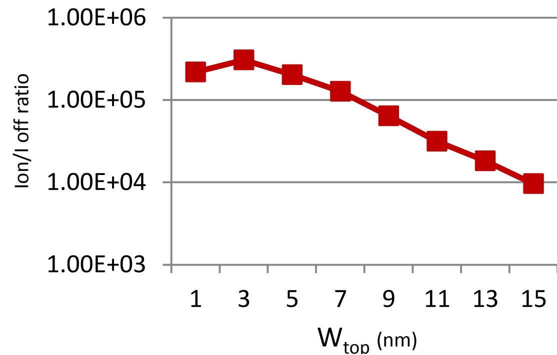


Fig. 9:I_{on}/I_{off} ratio of Tz PC FinFET v/s W_{top}

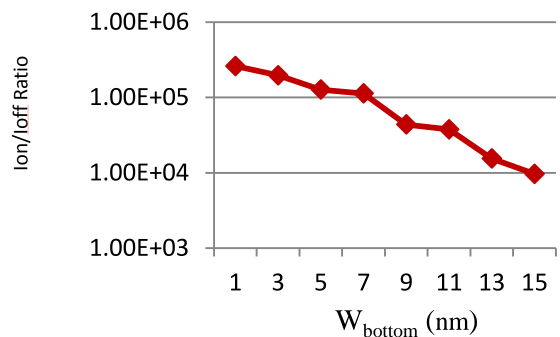


Fig. 10: I_{on}/I_{off} ratio of inverseTz PC FinFET v/s W_{bottom}

All the parameters extracted listed in the Table 2 and Table 3.All graphs are plotted based on values in these tables.

Table 2. Extracted parameters of trapezoidal PC-FinFETs

W_{top} (nm)	V_{th} (mV)	SS (mV/Dec)	Leakage current (A/µm)	I_{on}/I_{off} ratio
1	472.59	79.37	1.41E-10	2.19E+05
3	463.82	79.78	1.05E-10	3.07E+05
5	459.3	80.53	1.64E-10	2.03E+05
7	453.462	81.607	2.69E-10	1.28E+05

9	447.4	83.392	5.61E-10	6.42E+04
11	441.654	85.579	1.18E-09	3.16E+04
13	438.349	86.9895	2.13E-09	1.82E+04
15	435.946	89.577	4.18E-09	9.64E+03

Table 3.Extracted parameters of inverse trapezoidal PC-FinFETs.

W_{bottm} (nm)	V_{th} (mV)	SS mV/Dec	Leakage current (A/µm)	I_{on}/I_{off} ratio
1	428.69	76.76	1.46E-10	2.60E+05
3	429.6	77.33	1.96E-10	1.96E+05
5	429.8	78.65	3.04E-10	1.27E+05
7	429.836	78.69	3.45E-10	1.13E+05
9	431.309	81.7	7.73E-10	4.38E+04
11	435.33	83.2	1.07E-09	3.76E+04
13	436.31	86.76	2.59E-09	1.55E+04
15	435.946	89.577	4.18E-09	9.64E+03

4. CONCLUSION

In this work the impacts of fin shape on FinFET performance in 22nm bulk PC-FinFET are evaluated. Here performance parameters such as threshold voltage, subthreshold swing, leakage current and I_{on}/I_{off} ratio of trapezium PC-FinFET and Inverse trapezium PC-FinFET with different fin width are compared. From the results, it is vivid that Fin shape has considerable impact on leakage performance. Reducing W_{top} results in thinner fin and consume no additional IC area (FinFET foot print is not affected). So fin shaping is the area effective low leakage method. The fin shaping technique can be utilized to generate ultralow leakage FinFETs and multi threshold FinFETs.Compared to rectangular and inverse trapezium PC-FinFET, trapezium PC-FinFET gives better leakage control, high I_{on}/I_{off} ratio and threshold voltage range. Hence trapezium PC-FinFETs shall be proposed as one of the viable choices for Ultra low leakage and Multi threshold applications.

5. REFERENCES

[1] S. Cristoloveanu"How Many Gates Do We Need in A Transistor: One, Two, Three or Four??" *Romanian Journal of informationscience and technology*, Volume 11, Number 1, 2008, 17-28

[2] D. Hisamoto, W. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T. King, J. Bokor, and C. Hu, "FinFET—A self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*,vol. 47, no. 12, pp. 2320–2325, Dec. 2000.

[3] Mayur Bhole, Aditya Kurude, Sagar Pawar "FinFET-Benefits, Drawbacks and Challenges" *International Journal Of Engineering Sciences and Research Technology*,pp. 3219-3222,November 2013

[4] A.N. Moulai Khatira, A. Bouazzaa, B. Bouazza" Corner effects sensitivity to Fin geometry variations in Tri-gate SOI-FinFET"*Journal of Electron Devices*, Vol. 18, 2013, pp. 1549-1552

[5] Sanjeev Rai, Jyotsna Sahu, Wanjul Dattatray, R. A.Mishra, and Sudarshan Ti-wari "Modelling, Design, and Performance Comparison of Triple Gate Cylindrical and Partially Cylindrical FinFETs for Low-Power Applications"*International Scholarly Research Network ISRN Electronics*, Article ID 827452, 7 pages,doi:10.5402/2012/827452

[6] Brad D. Gaynor and Soha Hassoun, Senior Member, IEEE, "Fin Shape Impact on FinFET Leakage With Application to Multithreshold and Ultralow-Leakage FinFET Design" *IEEE transactions on electron devices,* vol. 61, no. 8,pp.2738-2744 august 2014

[7] Y. Li and C.-H. Hwang, "Effect of fin angle on electrical characteristics of nanoscale round-top-gate bulk FinFETs," IEEE *Trans. Electron Devices*, vol. 54, no. 12, pp. 3426–3429, Dec. 2007.

[8] R. Giacomini and J. A. Martino,"Trapezoidal cross-sectional infiuence on FinFET threshold voltage and corner effects,"*J. Electrochem. Soc*., vol. 155, no. 4, pp. H213-H217, 2008.

[9] Suman Lata Tripathi and R. A. Mishra,"Design of 20 nm FinFET structure with round n corners using side surfaceslopevariation",*Journal of Electron Devices*,Vol. 18, 2013

[10] Rudolf Theoderich Bühler,, Renato Giacomini1, Marcelo Antonio Pavanello1and João Antonio Martino"Fin Cross-Section Shape Influence on Short Channel Effects of MuGFETs"*Journal Integrated Circuits and Systems* 2012; v.7 / n.1:137-144

[11] P. Magnone, A. Mercha, V. Subramanian, P. Parvais, N. Collaert, M. Dehan, S. Decoutere,G. Groeseneken, J. Benson, T. Merelle, R. J. P. Lander, F. Crupi, and C. Pace"Matching Performance of FinFET Devices With Fin Widths Down to 10 nm"IEEE electron device letters, vol. 30, no. 12, December 2009,pp.1374-1376

[12] M. Poljak, V. Jovanovi´c, and T. Suligoj, "Suppression ofcorner effects in wide-channel triple-gate bulk FinFETs,"*Microelectronic Engineering*, vol. 87, no. 2, pp. 192–199, 2010