High Level Application Independent Optimum Voltage and Frequency Prediction for Low Power Systems

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ABSTRACT
Increasing complexity and higher performance requirements of modern integrated circuits have naturally led to very high power consumption. Dynamic voltage scaling (DVS) is well studied and known to be successful in reducing energy consumption. Dynamic frequency scaling (DFS) is another technique to reduce energy consumption. As technology scale to nanometre, leakage power will become prominent. In this paper the effect on energy consumption of the system while applying both DVS and DFS analysed. This study shows that by applying DFS with DVS the total energy consumption get decreased. For energy estimation process in this work high level power estimation method is used.

General Terms
Low Power, Power estimation

Keywords
DVS, DFS, Energy

1. INTRODUCTION
As technology scales down the number of transistors integrated on a single chip get increases and that lead to increased power dissipation. Static power become dominant in lower technology node [1]. The power dissipation affect the characteristics of a system. Although performance still remains a basic design target, energy consumption has become a critical factor for a system, particularly after the explosion of the portable devices market. So for portable electronic device which are powered by batteries, power is a critical design metric. The designers nowadays gives more important to Power estimation and optimisation. Types of estimation process include low level power estimation and high level power estimation. Low level power estimation method based on bottom-up design approach. It uses complete details about internal hardware structure of a circuit block. Bottom-up models can be built with high accuracy because the circuit level implementation is available. However, bottom-up models are not enough. Certain parts of the design (typically 25% or more) will consist of application-specific logic blocks that have not been previously designed [2].In higher technology node it is not feasible to use low level power estimation method. MahadevamurtyNemani and FaridN. Najm [2] proposed high level power estimation method to surmount this problem. In high level power estimation being at the higher level of abstraction, the power at lower levels of abstraction is predicted with a little amount of information from bottom levels. It estimate the power based on area complexity and average switching activity [3].

Power dissipation consist static and dynamic components. The main components contribute to dynamic power dissipations are charging and discharging of capacitors and short circuit current [4]. CMOS device scaling led to increase in leakage power dissipation. This is mainly due to the proportionally reduced threshold voltage level with the supply voltage which decreases at a speed of 0.85 per generation [5]. Leakage current mainly consists of subthreshold current and reverse bias junction current. Threshold voltage lowering results in larger leakage current. Study has shown that leakage power is responsible for over 42% of overall power dissipation in the 90-nm generation and can exceed above half in recent 65-nm technology. Fig. 1 shows a system wide power composition for a typical system-on-chip (SoC).

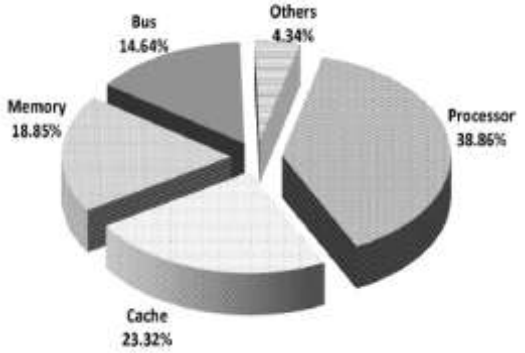

Figure 1: System-wide Power Consumption Breakdown of a Typical System on Chip

From Figure 1 it can be observed that processor, cache, memory and bus mainly contribute to the total power dissipation of the system. Wang et.al [6] applied two power reduction technique Dynamic Voltage Scaling (DVS) and Dynamic Cache Reconfiguration (DCR) to the system and analysed the energy variation. Lee et.al propose application ofboth Dynamic Voltage Scaling (DVS) and Dynamic Frequency Scaling (DFS) on a system to reduce power consumption [7].

2. PROBLEM DEFINITION
Applying DVS and DFS lead to reduction in energy consumption. This work aim to find the optimum voltage and frequency for a low power system while applying Dynamic Voltage Scaling (DVS) and dynamic Frequency Scaling (DFS) for a 65nm technology node

3. DESIGN METHODOLOGY
Total energy consumption is calculated by using energy models. In this work separate energy models for processor,

memory, cache and bus were used. Basic energy models are described in [8]. Every model contain dynamic as well as static energy. The existing works utilize incomplete energy models of the system components [9]. In this work, the ignored components short circuit power [13] which causes dynamic power dissipation and gate leakage which adds to static power dissipation are incorporated in the energy models of the system components.

3.1 Processor Energy Model

Dynamic energy of the processor is

$$E_{dyna} = P_{dyna} * C_C * t_{cycle} + E_{short} \quad (1)$$

Where P_{dyna} is the dynamic energy of the processor, C_C is the number of clock cycles, t_{cycle} is the clock cycle length and E_{short} is the short circuit energy. Static energy of processor is [8]

$$E_{sta} = P_{sta} * C_C * t_{cycle} + E_g \quad (2)$$

3.2 Main Memory Energy Model

Dynamic energy of main memory is

$$E_{dynamem} = N_{acc} * E_{acc} + E_{short} \quad (3)$$

Where N_{acc} is the number of times it access to the memory, E_{acc} is the amount of energy needed for single access and E_{short} is the short circuit energy of main memory [8].

3.3 Bus Energy Model

The average dynamic power consumption of various system buses can be calculated by [10]. Static energy of bus is given by

$$E_{sta} = P_{sta} * C_C * t_{cycle} + E_g \quad (4)$$

and dynamic energy of bus is given by

$$E_{dynabus} = (P_{dynaoffc\ hipL1} + P_{dynaoffc\ hipL2} + P_{dynaonc\ hip}) * C_C * t_{cycle} + E_{short} \quad (5)$$

$P_{dynaoffchipL\ 1}$ is power dissipation during L1 cache access. $P_{dynaoffchipL\ 2}$ is the power dissipation due to L2 cache access. $P_{dynaonc\ hip}$ is power dissipation during onchip access. The system consist L1 and L2 caches. System buses are need to access both these caches. So the power consumption while on chip and off chip access are considered.

3.4 Cache Memory Energy Model

Dynamic energy for cache memory is given by

$$E_{cachedyna} = (N_{acc} * E_{acc}) + (N_{miss} * E_{miss}) + E_{short} \quad (6)$$

Energy dissipated during cache access and cache miss. Both of this considered here. N_{acc} is number of cache access, E_{acc} is energy needed for one access. N_{miss} is the number of cache miss and E_{miss} is the energy needed for a single miss. Static energy is

$$E_{cachesta} = P_{sta} * C_C * t_{cycle} + E_g \quad (7)$$

Micro architectural simulator Simplescalar [11] is used in this work to collect the simulation parameters which are used as inputs to the energy estimation frame work. To evaluate the effectiveness of this approach, a benchmark binary is selected. The benchmark binary used here is *cjpeg* which is a component of Mediabench [12] benchmark suit. Cjpeg does image compression. MediaBench composed of multimedia programs which are written in high level language. Some values that are constant for a particular technology node are also need for calculating total energy. This was obtained from [8].

4. RESULTS AND DISCUSSION

The sim-outorder simulator implements a very detailed out-of-order issue superscalar processor with a two-level memory system and speculative execution support. This simulator is a performance simulator, tracking the latency of all pipeline operations. The output of this simulator give the values required. It substituted in the energy models. The energy model get validated using Matlab.

The obtained result is going to discuss in two sections. In the first section the effect of voltage scaling on total energy get analysed. It already mention that there are 4 important power consuming parts are there in a system. That are processor, memory, bus and cache. So here effect of voltage scaling on these four parts analysed separately. By analysing the total power consumption the optimum voltage and frequency for the system get observed.

In the next section integrated DVS and DFS technique was applied on the system and the effect on total energy get observed. This was analysed with a 3D plot. The optimum frequency voltage values obtained and compared with previously obtained one.

4.1 Processor Energy

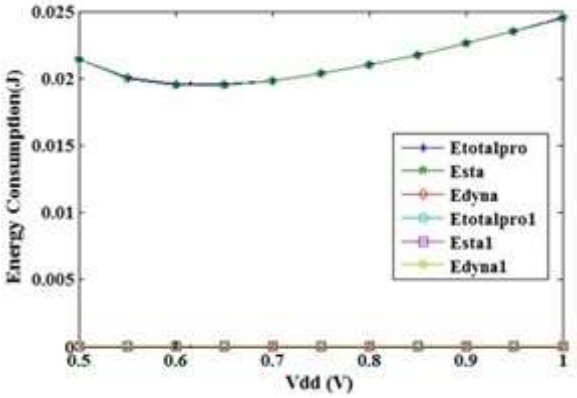

Figure 2: Processor Energy

The plot obtained for processor energy is shown in Figure 2. Equation (1) and (2) used to obtain this plot. The plot contains dynamic energy, static energy, energy when processor is on and total energy consumed by the processor when the benchmark circuit *cjpeg* is run on it. Because of updated energy model the energy get increased. Here short circuit energy and gate leakage energy considered. Due to this the critical speed of the system also varies. The critical speed for processor voltage scaling defines a point beyond which the processor speed cannot be slowed down otherwise DVS will no longer be beneficial [9]. $E_{totalpro}$ is the total energy consumed by the processor, E_{sta} is static energy consumed by the processor, E_{dyna} is dynamic energy consumed by the processor.

4.2 Processor +Cache Energy

The plot obtained for cache energy is shown in Figure 3. Equation (6) and equation (7) used to plot this graph. The total energy dissipation get increases because here energy models are updated with short circuit energy E_{short} and gate leakage energy E_g. Due to this the critical speed of the system also

varies. The system contains two cache named L1 and L2. Power consumed by both caches considered here. E_{total} is the sum of processor and cache energy. $E_{totall\ 2}$ is total energy of L2 processor. $E_{totalpro}$ is the total energy consumed by the processor. $E_{cachestal\ 2}$ is static energy of L2 cache. $E_{cachedynl\ 2}$ is dynamic energy of L2 cache. $E_{cachesta\ 22}$ is the static energy of L1 cache. $E_{cachedynal\ 22}$ is dynamic energy of L2 cache.

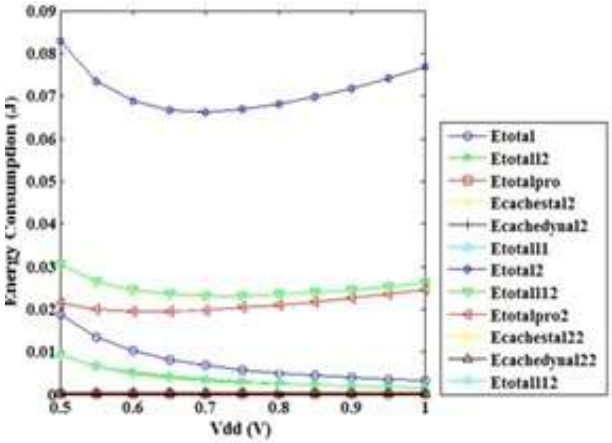

Figure 3: Processor + L1/L2 Cache Energy

4.3 Processor+L1/L2 Cache + Main Memory Energy

The plot obtained for main memory energy is shown in Figure 4. Equation (3) is used to plot this. There is clear hike in power dissipation due to the short circuit power and gate leakage current of device.

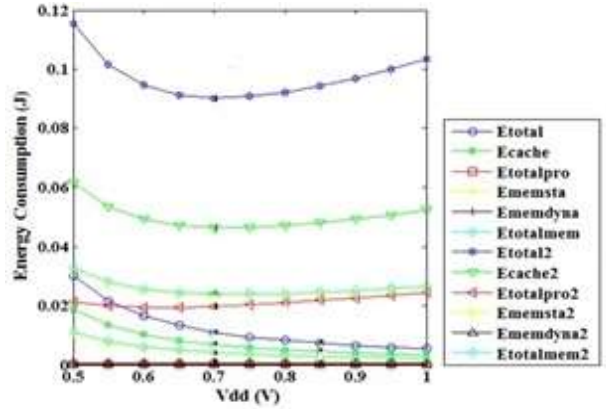

Figure 4: Processor+Cache+Memeory Energy

Critical speed is obtained at low voltage compared to earlier works. $E_{memdyna}$ is dynamic energy of memory. E_{memsta} is static energy of memory. $E_{totalmem}$ is total memory energy.

4.4 Total Energy Consumption of System while Applying DVS

Figure 5 shows total energy consumption of a system while applying DVS. E_{cache} is cache energy of the system. $E_{dynabus}$ is dynamic energy of the bus.E_{stabus} is static energy of the bus. $E_{totalmem}$ is the total memory energy.$E_{totalpro}$ is the total energy of the processor. $E_{totalbus}$ is the total energy of the bus. E_{total} is the total energy of the system. From this plot it can be obtained 0.7V as optimum voltage for the system.

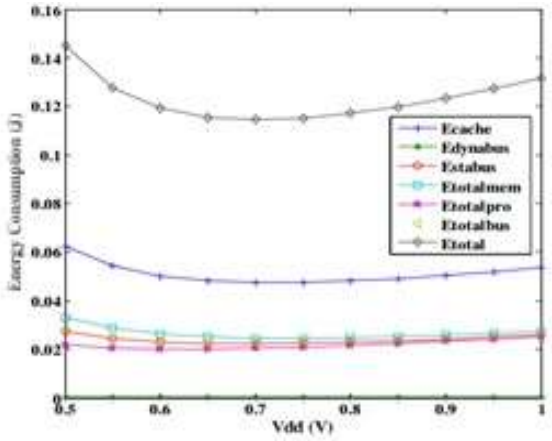

Figure 5: Total Energy Consumption of a System While Applying DVS

Figure 6 shows the 3D plot of figure 5. From this plot it can be obtained that optimum frequency for the system is 1.36 GHz. So while applying dynamic voltage scaling at a voltage of 0.7V and frequency of 1.36GHz minimum energy obtained.

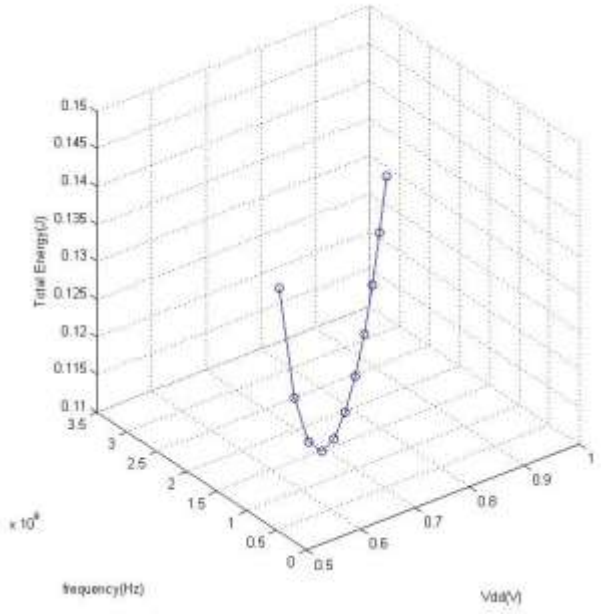

Figure 6: Total Energy of System while Applying DVS in 3D

4.5 Total Energy Consumption of System while Applying Integrated DVS and DFS

Figure 7 shows the variation in energy while applying both DVS and DFS. From this it can be observed that the total energy consumption get decrease to 0.0087J. Here the optimum voltage and frequency is 0.7V and 20.45 GHz. Here the frequency get changed to20.45GHz. So while applying DVS and DFS the total energy decreased.

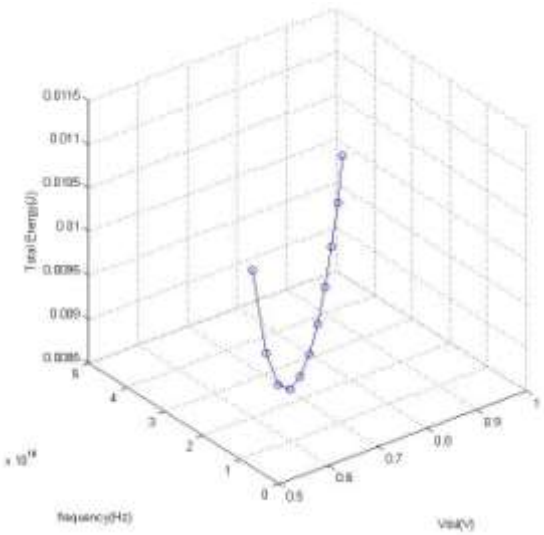

Figure. 7: Total Energy of System while Applying DVS and DFS

Table 1: Comparison of Energy

	Voltage (V)	Frequency (GHz)	Total Energy (J)
DVS only	0.7	1.36	0.1120
Integrated DVS and DFS	0.7	20.45	0.0087

Table 1 shows that the variation in energy while applying DVS and integrated DVS and DFS. Here it can be observed that the total energy consumption get decreases while applying integrated DVS and DFS.

5. CONCLUSION

High level power estimation method is a fast and easy method to estimate total energy of the system. By using energy models total energy consumption of the system can calculate. DVS and DFS are two energy reduction techniques. By integratingDVS and DFS the energy consumption of the system reducesfurther. The optimum frequency get changed here.Using high level method the optimum voltage and frequency can be identified. Here the optimum voltage and frequency get identified using the simulation method. It is not at all easy to do the simulation every time to find this. So a mathematical model for the optimum frequency and voltage can be modeled by analyzing

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