Design of 1-Bit DAC for Delta-Sigma Modulator

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ABSTRACT
This paper presents design methodology and comparison of a 1-bit DAC in both 180 nm and 90 nm CMOS technologies. A 1-bit digital-to-analog converter (DAC) is designed and simulated in 180 nm and 90 nm CMOS technologies using Cadence Virtuoso tool. This DAC can be used in the feedback path of Delta-Sigma modulators. Delta-Sigma ADC is the most robust type of ADC which is highly immune to noise compare to that of ordinary analog-to-digital converters.

General Terms
Digital-to-Analog conversion, Digital, Analog

Keywords
DAC, Delta-Sigma Modulator,90 nm,180 nm

1. INTRODUCTION
Nowadays, wireless communication systems are of higher demand because of its portability and low power nature. There is a strong tendency to move the development of wireless communication systems from analog domain to digital domain, since digital systems have higher stability and flexibility than analog systems. In reality all the natural signals are analog in nature. Hence the use of analog to digital converters in the field of communication applications increases day by day. In order to convert analog signal to digital domain in the presence of noise a high resolution ADC is required. Usually the analog-to-digital converters operate at Nyquist frequencies; and are called Nyquist rate converters. But the speed of these converters is very low when used communication systems compared to oversampling converters. So these converters can be replaced by Delta-Sigma A/D converter, which is an oversampling noise shaped data converter. Delta-Sigma A/D converter is one of the most suitable types of ADC in wireless communication applications [1]. The Delta-Sigma A/D converter posses the properties of oversampling and noise shaping, which makes them the most attractive choice as noise immune, high resolution and low power data converters. Due to the technology advancement, Delta-Sigma A/D converters are being adapted for high frequency applications involving several GHz frequencies. This paper illustrates design and performance evaluation of 1-bit DAC to be used in the realization of Delta-Sigma Modulator.

2. DELTA-SIGMA MODULATOR
A simple block diagram of Delta-Sigma A/D converter is shown in Fig 1. The Delta-Sigma A/D converter contains Delta-Sigma modulator and a digital decimator filter. Since the output of the modulator is digital and it contains high frequency noise components, digital low pass filter is used to remove the high frequency components. The decimator filter used slows down the data rate [2].

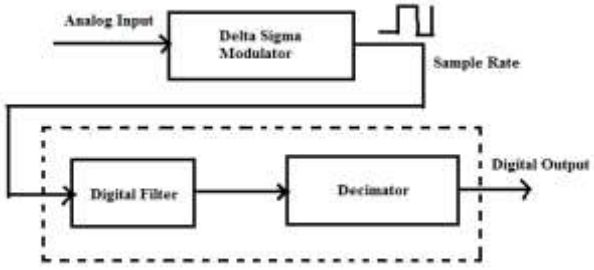


Fig 1: Block Diagram of DS ADC

The basic block diagram of Delta-Sigma modulator is shown in Fig 2. The key components of a Delta-Sigma modulator include an integrator, 1-bit comparator and a 1-bit DAC. The noise shaping process is done by the integrator stage, which pushes the noise present in the signal band out. Then the output of this integrator is consumed by a 1-bit comparator and corresponding digital output is produced [3]. This digital output is fed back to the input side for comparison with the analog input. The comparison could be achieved only between compatible types of signals. So a 1-bit DAC is employed in the feedback path to make the feedback signal compatibility with the input analog signal. The difference between DAC output and analog input signal is obtained using difference amplifier. The error signal produced by the difference amplifier is given to the integrator [4] Delta-Sigma modulators are available in two configurations, Discrete-Time (DT) Delta-Sigma modulator and Continuous-Time (CT) Delta-Sigma modulators. CT Delta-Sigma modulator is predominantly used in wireless applications because it has high BW, high operating speed and lower power consumption compared those of the other [5]. Oversampling is the process of taking more samples per second than required by the Nyquist rate converters. The noise spectral density is gets spread over wide range of frequencies and hence the noise component in the signal band gets reduced considerably. Second property improving the performance is the noise shaping [6]. In this process the quantization noise density is reduced in the signal band by pushes the noise signals out of the signal band [7].

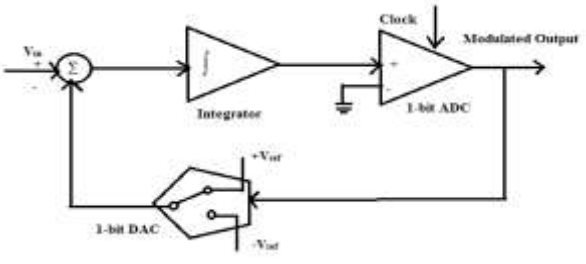


Fig 2: Block Diagram of DS Modulator

Delta-Sigma A/D converters now becoming the most suitable solution for standard wireless systems since it is an oversampling converter, delta-sigma modulators can achieve high BW by increasing the oversampling ratio (OSR) [8].

3. DAC

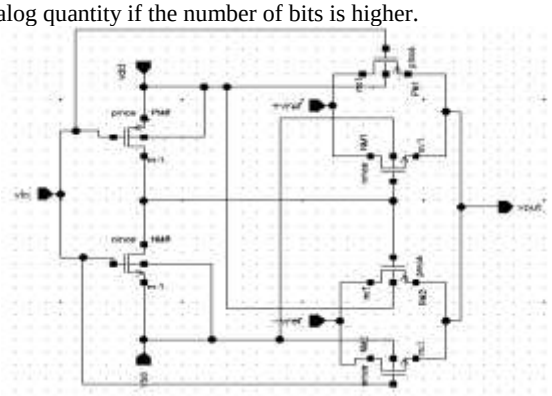
3.1 Requirement of DAC in Delta-Sigma Modulator

Even if the operation of communication systems are carried out by digital signal processing (DSP) core, the signals present at the input and output ends of these systems are always continuous time signals. So these kinds of systems usually need a analog-to-digital converter (ADC) at input end, and a digital-to-analog converter at the output end. A digital-to-analog converter with high resolution and small area is highly useful in such systems. This work presents a 1-bit DAC designed for Delta-Sigma modulator.

As mentioned in the working of delta-sigma modulator, the difference between analog input signal and analog output of the feedback DAC is consumed by the modulator. The signal that appears at the output of ADC is always in digital form. So, before feeding it back to the summing amplifier, it must be converted to analog form. This is done by the feedback DAC. DAC plays an important role in the proper working of Delta-Sigma modulator. Usually Delta-Sigma modulators use 1-bit DAC, since multi-bit implementations will increase the cost [9].

3.2 1-bit Digital-to-Analog Converter

Basically, digital-to-analog conversion is the process of converting a digital value or code to a voltage or current. This analog value is always proportional to the digital value. The Fig 3 shows a basic block diagram of N-bit DAC. 2^N input codes are possible in an N bit DAC. This DAC contains an analog reference voltage V_{ref}, supply voltage V_{dd} and analog output. Supply voltages as well as the reference voltage will be same in some cases. Both analog-to-digital and digital-to-analog conversions are important for a digital processing system. A DAC is usually a vital part of any ADC [10]. The output of a digital-to-analog converter is not a true analog quantity, because it can take only specific values. So, the output of a DAC is always a pseudo-analog quantity. Since the analog output produced is proportional to the digital input, as the number of input bits is increased the step size gets reduced. Because of this feature the output is more like an analog quantity if the number of bits is higher.



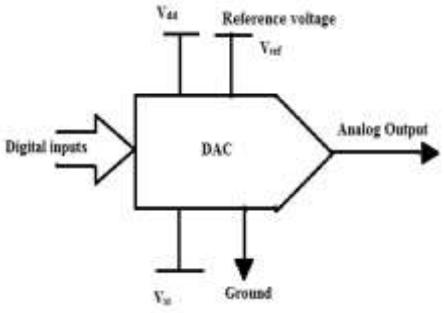
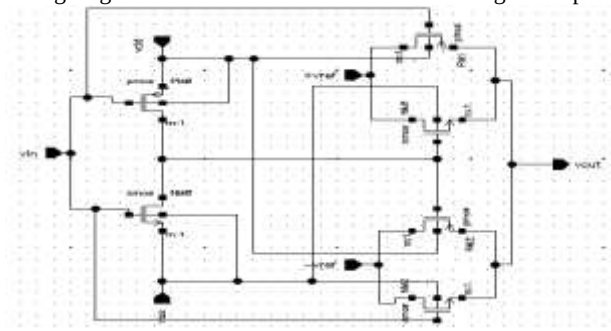


Fig 3: Block Diagram of DAC

For this particular application, digital input to the 1-bit DAC is provided by the comparator designed using operational amplifier. As shown in the block diagram of the modulator the DAC converts the digital output to an analog signal and feeds back to the integrator. Since it is a 1-bit DAC, the resultant analog signal also has two levels as the digital input



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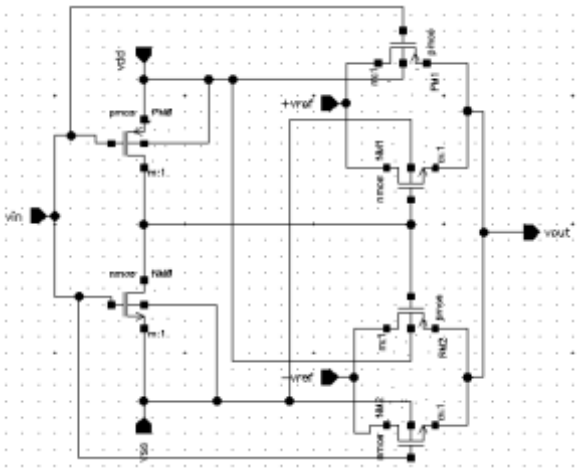

Fig 4: Circuit Diagram of 1-Bit DAC

The circuit of 1 bit DAC in 180 nm CMOS process is shown by the Fig 4. This circuit contains two transmission gates and an inverter. In this circuit two reference voltages are used. For this particular case, $+V_{ref}$ is taken as +2.5 V and V_{ref} is taken as –2.5 V. And the operation of the circuit can be explained by two cases. If the input is 1, then output of the DAC is $+V_{ref}$ and if the input is 0, then DAC output is V_{ref}. This logic is implemented using a 2×1 multiplexer circuit. Output of the comparator act as the select lines of the multiplexer to select the 1-bit digital input [11]. Transmission gates are controlled by the output of comparator and its inverted output is obtained from the inverter [12].

4. SIMULATION RESULTS

The design of 1-bit DAC is implemented in 180 nm and 90nm CMOS process using Cadence Virtuoso tool and the schematic diagram of DAC is shown in Fig 5. The simulation results obtained are given as follows:

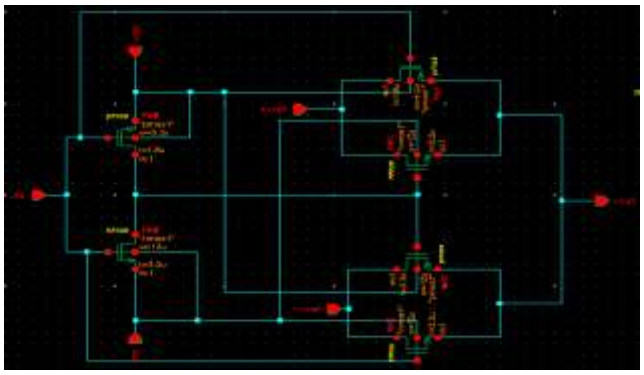

Fig 5: Schematic of 1-Bit DAC

4.1 Transient Analysis

The transient response of 1-bit DAC implemented in 180 nm and 90 nm CMOS processes are shown in Fig 6 and Fig 7 respectively.

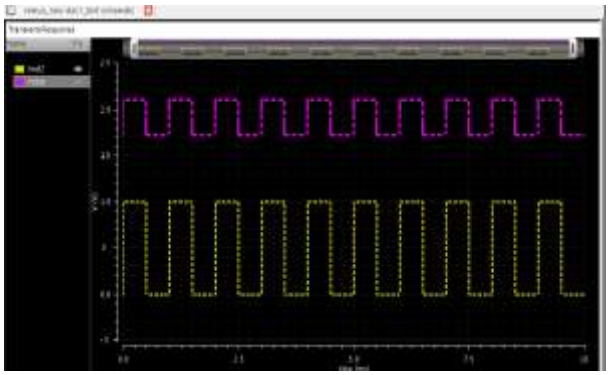

Fig 6: Output of DAC in 180 nm Technology

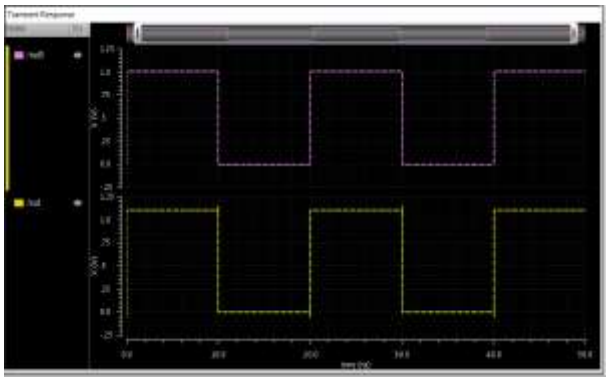

Fig 7: Output of DAC in 90 nm Technology

4.2 Power Analysis

Power dissipation comparison of the two implementations is carried out by the power analysis process supported by the platform. The power dissipated from a circuit can be quantified as:

$$P=VI \quad (1)$$

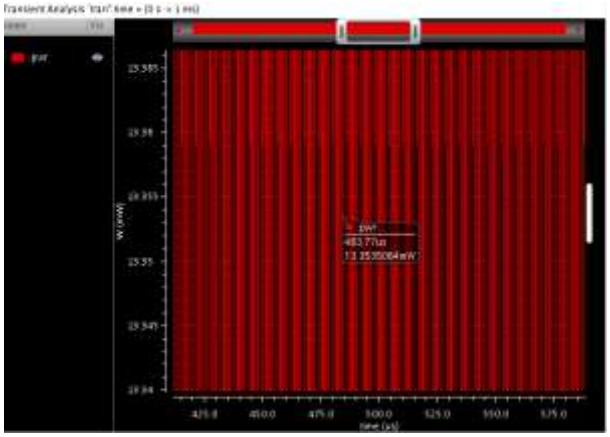

Fig 8: Power Spectrum in 180 nm Technology

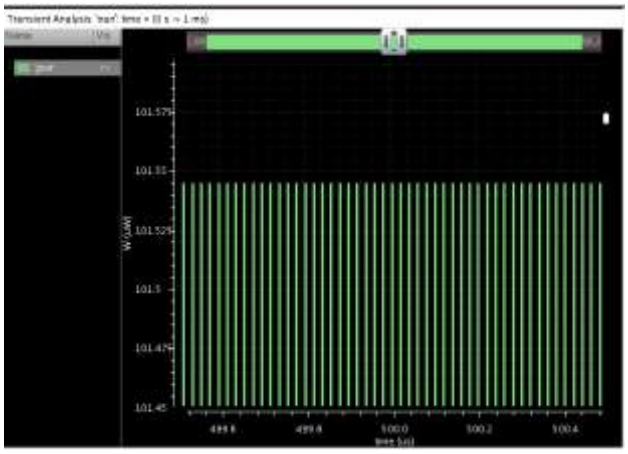

Fig 9: Power Spectrum in 90 nm Technology

The power dissipation of 1-bit DAC in 180 nm and 90 nm is different, since the dissipated power directly proportional to supply voltage. In 180 nm CMOS process technology the supply voltage used is 1.8 V and that of 90 nm is 1 V. So that power dissipation is higher in 180nm technology. The Table 1 shows the power dissipation comparison of 1 bit DAC implemented in 90 nm and 180 nm CMOS process. The power spectrum of 180 nm and 90 nm is shown by Fig 8 and Fig 9.respectively.

Table 1. Performance Parameters of 1-Bit DAC

Technology	180nm	90nm
Supply Voltage	1.8 (V)	1(V)
Average Power	13.48(mW)	0.138(mW)

5. CONCLUSION AND FUTURE SCOPE

In this paper a 1-bit DAC for Delta-Sigma modulator is implemented in both 90 nm and 180 nm CMOS technologies. The input voltage for 90 nm technology is 1V and that of 180 nm technology is 1.8V.This is simulated using Cadence Virtuoso tool, and the results obtained are compared. The power consumption of DAC in 180 nm technology is 13.48 mW and it is very much larger when compared with the power dissipated (0:138mW) in 90 nm technology. In the designing of delta-sigma modulator DAC plays an important role. In this paper a basic DAC is designed, in future instead of this basic DAC opamp based DAC can be implemented for DSM. This will improve the performance of DSM.

6. REFERENCES

[1] K. Dobson, S. Ahmadi, and M. Zaghloul, "A 1.2 ghz band-pass sigma delta analog to digital modulator with active inductor based resonators," in Proceedings of the World Congress on Engineering and Computer Science, vol. 2, 2012.

[2] R. Schreier and G. C. Temes, Understanding delta-sigma data converters, vol. 74. IEEE press Piscataway, NJ, 2005.

[3] B. P. Brandt, D. E. Wingard, and B. A. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," Solid-State Circuits, IEEE Journal of, vol. 26, no. 4, pp. 618– 627, 1991.

[4] J. A. Cherry and W. M. Snelgrove, Continuous-time delta-sigma modulators for high-speed A/D conversion: theory, practice and fundamental performance limits, vol. 521. Springer Science & Business Media, 2000.

[5] A. Tabatabaei and B. A. Wooley, "A wideband band pass sigma-delta modulator for wireless applications," in VLSI Circuits, 1999. Digest of Technical Papers. 1999 Symposium on, pp. 91– 92, IEEE, 1999.

[6] I. Galton, "Noise-shaping d/a converters for ds modulation," in Circuits and Systems, 1996. ISCAS'96., Connecting the World., 1996 IEEE International Symposium on, vol. 1, pp. 441–444, IEEE, 1996.

[7] Y. Li and L. He, "First-order continuous-time sigma-delta mod-ulator.," in ISQED, pp. 229–232, 2007.

[8] J. A. Cherry and W. M. Snelgrove, "Clock jitter and quantizer metastability in continuous-time delta-sigma modulators," Cir-cuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on, vol. 46, no. 6, pp. 661–676, 1999.

[9] R. J. Van de Plassche, "Cmos integrated analog-to-digital and digital-to-analog converters," vol. 2, Kluwer Academic Publish-ers Dordrecht, 2003.

[10] M. Kosakowski, R. Wittmann, and W. Schardein, "Statistical averaging based linearity optimization for resistor string dac architectures in nanoscale processes," in SOC Conference, 2008 IEEE International, pp. 261–266, IEEE, 2008.

[11] D. A. Johns and K. Martin, "Analog integrated circuit design," John Wiley & Sons, 2008.

[12] R. L. Geiger, P. E. Allen, and N. R. Strader, "Vlsi design techniques for analog and digital circuits," vol. 90, McGraw-Hill New York, 1990.