Low Power Implementation of Low Drop-Out Voltage Regulator for Mobile Platforms

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ABSTRACT
Power management in a battery operated device can be done with the help of voltage regulators. This work proposes the design of a low drop out (LDO) regulator that provides the required supply voltage to different modules of the battery operated devices. The system is designed in 180nm technology with 1.8 V supply. Low power implementation of the design can be achieved using the self-sustainability of the regulator. The proposed regulator system can be made as selfsustainable by providing the 1.8 V regulated output as the supply for some blocks of the system. So the battery voltage is no longer required for the functioning of those blocks. The current gain of the operational amplifier has been improved by adding a buffer stage after the common source amplifier. This buffer will improve the ability of the LDO regulator to drive large capacitive and resistive loads.

Keywords
Low Drop Out, power management, voltage regulator, self-sustainability.

1. INTRODUCTION
Battery can be used to source all the systems that are designed above 0.5u-0.6u technology, theoretically. When we use a voltage regulator in between the battery and the system, the battery life can be improved considerably. So for the circuits that are designed in 0.18u technology and below, voltage regulator is a must. As most cell phones operate with single cell battery nowadays, these regulators will be very useful to achieve better efficiency as the power consumed is proportional to square of the applied voltage. Currently the manufacturers are aiming at low power methodologies to improve the battery life and also the life of the components [12].

Nickel Cadmium (NiCad), Nickel Metal Hydride (NiMH) or Lithium Ion (Li-Ion) batteries are typically used by most of the consumer electronic devices. Li-Ion batteries are having battery voltages of 4.2/3.7 V. It means the maximum voltage it can charge up to is 4.2V and its nominal or the average voltage is 3.7V. It will be dead it when reaches 3.0V and the cut off circuitry disconnects the battery.Operating a system directly from this unregulated battery source will cause the system to fail. As the battery voltage is not a constant throughout the operation of the system a voltage regulator is a must for every battery operated devices. Here a Low Drop-Out (LDO) voltage regulator is used to provide regulated voltages for the different modules of the mobile devices. Due to low drop out nature these regulators have high efficiency compared with other types of regulators.

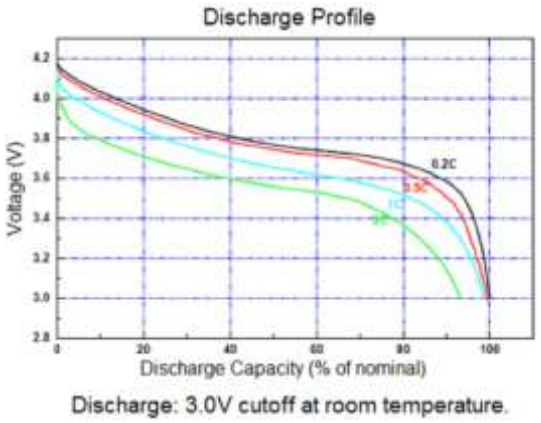

Fig 1: Battery Profile [14]

Figure 2 shows the voltage distribution profile in a mobile device. LDO regulators provide the regulated supply voltage to different modules like Base Band circuitry, Receiver/Transmitter section and Power Amplifier section. They require voltages in the range 2.8V, 1.8V and 1.5V. LCD display, SIM card etc. are handled using Boost converters like charge pump and SMPS.

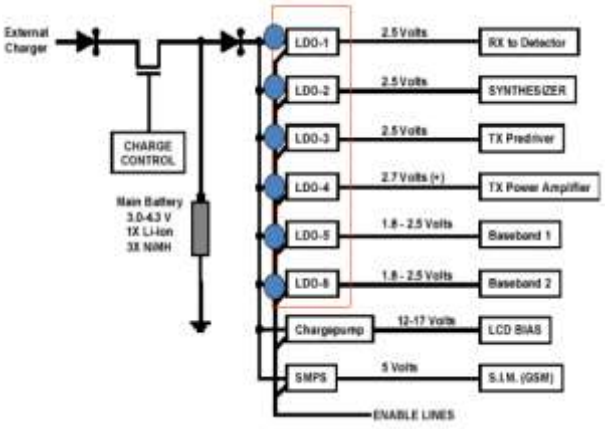

Fig 2: Mobile phone Voltage distribution [12]

2. PROPOSED DESIGN
The proposed LDO voltage regulator design provides 1.8V of regulated voltages from the battery source. Low power operation can be attained by self-sustaining the system. It means to use regulated 1.8V output as the source for some of the blocks of the design such as two stage operational amplifiers and start-up circuit. It is possible only if the system is stable in the closed loop operation. The voltage reference for the regulator is provided by using a voltage source [5] [7] [14].

Internal block diagram of the proposed LDO consists of mainly four parts [2] [6].

- Reference voltage
- Error Amplifier circuit
- Pass transistor block
- Feedback network

The battery supply is provided at the source terminal of the PMOS pass transistor block. The dropout of the voltage regulator appears across this block. The voltage divider network will feed back the output voltage to one of the input terminals of the error amplifier. The other input is provided by the reference voltage and the error value is used to control the pass transistor block. The error amplifier tries to reduce the difference between feedback voltage and the reference voltage. The turn on/off of the pass transistor block depends on this error amplifier output. So this pass transistor block acts as the gate for the system. The error amplifier and start up circuits of all three LDOs are supplied from the 1.8V output. So the battery voltage is not required to power those blocks after the system attains its stability [8] [11].

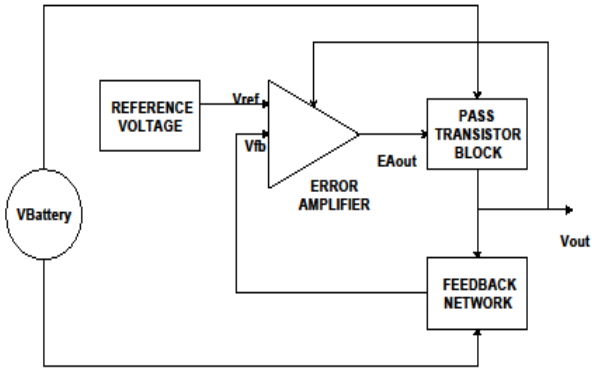

Fig 3: LDO Internal Block diagram

3. EXPERIMENTATION APPROACH

Cadence Virtuoso IC design tool kit version IC6.1.6 was used for the experimental set up. Tools available in this kit are ADE, Layout XL, Spectre and Assura. ADE is used for schematic entry, Spectre is used for simulation, Layout XL is used for drawing the layout and Assura is for extracting the parasitic effect. Figure 5 shows the complete Cadence virtuoso IC design flow [13].

The width (W) and length (L) of the transistors are designed based on the technology used. In 180nm technology the minimum supply voltage that can be provided is 1.8V and the maximum is 3.3V. For this design the L value of transistor is fixed as 1um (2 - 5 times of technology used) and the W value is designed for each transistor available in the entire circuit. The simulation can be done using the ADE (Analog Design Environment) tool and analysis like DC, AC, transient, pole-zero, stability etc. can be carried out. The result obtained at this stage is ideal as we haven't considered the parasitic that will affect the circuit during placement and routing. Layout XL tool is used for drawing the layout and its verification can be done by checking the DRC (Design Rule Check) and LVS (Layout Versus Schematic) using the Assura tool. Parasitic are extracted by RC extraction feature and they are back annotated to the schematic and are re-simulated to find out the exact output. If they are matching GDSII file can be extracted and can be send to the foundry for fabrication. If required output is not obtained the whole process needs to be repeated from the design stages.

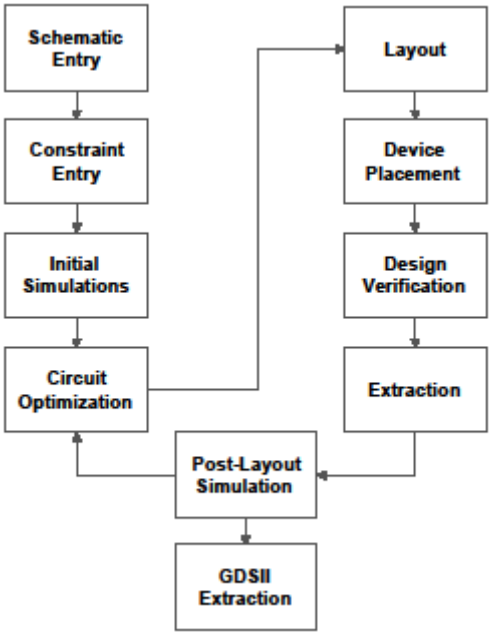

Fig 4: Design Flow using Virtuoso [13]

4. EXPERIMENTAL RESULTS

The proposed LDO regulator is designed using 180nm technology. The complete chip layout view of the three regulators is shown in figure 6. The area of the chip is only 0.007 sq. mm. The LDO is capable of operating from 3V to 5V which covers the typical battery voltage ranges.

4.1 Drop-Out Voltage

Drop-out voltage is the minimum input/output differential voltage where the circuit begins to stop regulation. Typical drop-out voltages range from 0.1 to 1.5V.

- The drop-out voltage of LDO is 200 mV

4.2 Transient response and Power plot

The transient response shows that the self-sustained LDO regulator is regulating correctly for the entire time duration. The total power consumed by the regulator system is only 0.745mW. The power consumption is reduced by more than half in this self-sustained mode. In the normal case it was 1.85mW. About 1.1mW of power dissipation was reduced by implementing this method.

4.3 Line regulation

The input supply is made as a pulse source varying from 3V to 4.3V, which is the maximum voltage of a battery source. The time period of the pulse is selected as 1 ms.It is having a pulse width of 500 us with rise time, fall time and delay time of 10 ns.

- Line regulation of LDO is 5.55mV/V

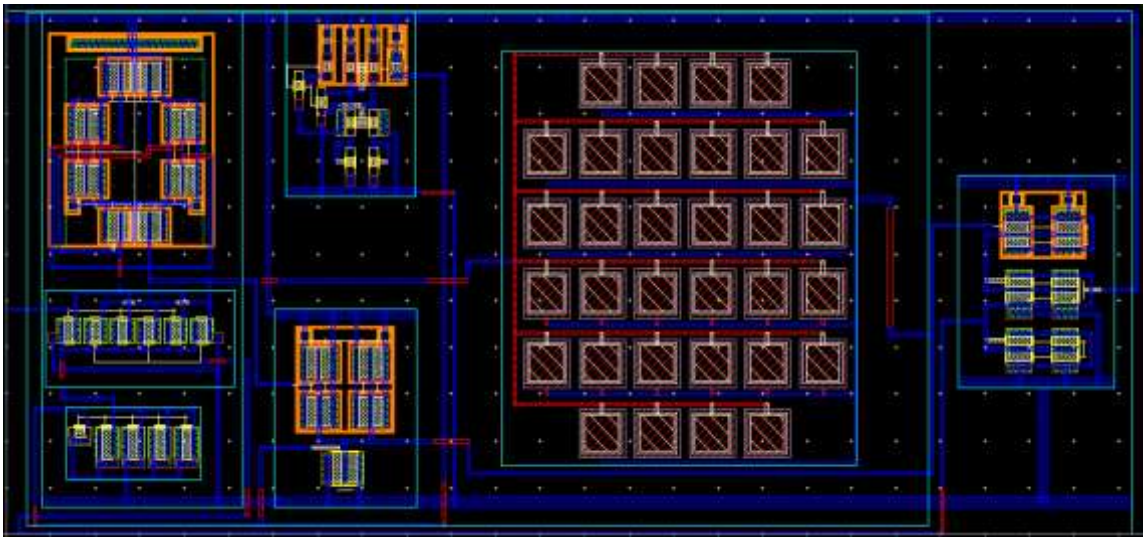

Fig 5: Layout

4.4 Load regulation

The load current is varied from 0 to 20mA using a current pulse source. The time period of the pulse is selected as 1 ms.It is having a pulse width of 500 us with rise time, fall time and delay time of 10 ns.

- Load regulation of LDO is 221 uV/mA

Table 1.Performance Comparison

Design Parameter	2010 [3]	2011 [4]	2012 [1]	This Work
Technology (um)	0.5	0.18	.09	0.18
Drop out (mV)	190	210	150	200
Load cap.(uF)	1	1	1	1
Resr (mOhm)	-	20	1	30
Iout max (mA)	100	50	100	20
Line reg. (mV/V)	120	38	24	5.55
Load reg. (uV/mA)	0.25	0.3	0.24	0.22
Area (mm sq.)	0.0142	0.0395	0.00059	0.007

5. CONCLUSION

This work proposes a low power implementation of LDO voltage regulator module for the mobile platform. This LDO also improves the battery life and provides isolation to sub-circuits within the device. LDOs usually steps down the voltage supplied by the battery source. The proposed work provides fixed output voltages of 1.8V.Low power operation of the regulator is achieved by making the regulator a self-sustained one. When the circuit becomes stable, the regulated 1.8V output can be used to power some system blocks, so the battery source is not needed to power them. Total power consumption of the system was 1.85mW in the normal operation. By attaining the self-sustained mode it was reduced to 0.745mW. So the power is reduced by more than half using this method.

In the layout the effect of parasitic are reduced by the method of fingering the transistors. Multipliers are used for attaining symmetry of the layout. The layout of the regulator drawn can be optimized by carrying out common centroid and inter digitization techniques to transistors that require high priority of matching but routing will be complex and area consumed will be more. So layout should be optimized considering the power reduction in mind.

6. ACKNOWLEDGEMENT

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