Novel Architectures of Load Side Power Conditioning Units for Micro-Satellites

Adithya S N
Undergraduate Student
Electrical and Electronics dept.
Acharya Institute of Technology
Bangalore

Raghu Raman.S
Project Assistant
Power Electronics Group
Indian Institute of Science Bangalore

ABSTRACT

Micro-Satellites ,consist of many controllers, controlling circuits, sensors, actuators, telemetric equipment, data acquisition systems and storage systems to monitor and control the satellite operations. These have different power requirements and must be turned ON or OFF depending upon the satellite operation for better utilization of the electrical energy available in limit. These functions are fulfilled by the Power Conditioning Unit (PCU) present on each of the above mentioned circuits. PCUalso protects these devices from faults such as short circuit, open circuit, over current and over temperature, gives feedback of ON/OFF status and fault status to the on board Microcontroller (µC) in regular intervals thereby forming a close loop system.As it is a Micro-Satellite, PCU design must be compact and must use as few components as possible to make it less bulky without compromising on its objectives. This paper describes PCU, its objectives,different architectures of PCU depending on number of loads and operational speed requirements, how the objectives of PCU and its design are achieved, devices used in the designs and different protocols used for communication.

General Terms

Electrical fault detection, closed loop control, novel architectures for power conditioning units.

Keywords

Micro-satellites, Power Conditioning Unit (PCU), I2C Communication Protocol, 1-Wire Communication Protocol, Electrical and Addressable switch.

1. INTRODUCTION

The primary designsof a load side power conditioning unit for micro – satellites [1&2] were completed as a part of a summer internship at IISc, Bangalore. A power conditioning unit (PCU) is placed on everyload (i.e., controllers, controlling units, sensors etc.,) the satellite houses to perform various pre-defined tasks namely, supply regulated power to all the electrical loads, turn on or off electrical loads on the satellite depending upon the requirement, continuously monitor the efficient functioning of these loads and communicate the status of these loads through a feedback to an onboard processor/controller and to identify the type of electrical fault (if any) at the load side and turn off loads during faults. These objectives were successfully attained. This was designed keeping in mind the fixed number of loads the satellites would house, communication speed requirements and several other parameters. The design had lots of limitations and was not flexible. In case, there was a requirement to increase the number of loads the satellite would host or there was a demand for higher communication speeds, the design could not function normally. A resultant decrease in the communication speedwas observed due to the increase in number of loads. The power conditioning unit must be able to diagnosefaults and turn off that particular load at fault. Now if the system is functioning at lower communication speeds, then the damage to that particular load during faulty operations would be worsened.

This paper overcomes such limitations and proposes novel architectures of PCU depending on number of loads and operational speed requirements. The paper explains the basic architecture of a PCU in the succeeding paragraph, describes the different building blocks of the PCU i.e. the voltage regulator, electrical switch and the addressable switch, explains PCU communication by briefing about I2C[3] and 1-wire protocol[4] with their application in each of the novel architectures and finally discusses the different architectures of PCU in the succeeding sections.

The basic block diagram of Power Conditioning Unit (PCU) is shown in Figure 1**.** It basically consists of four blocks.

- Addressable switch:This is used for PCB addressing and identification via communication bus.
- Electrical switch:This is used to switch ONor OFF power to the circuit.
- Regulator:This regulates voltage from unregulated voltage bus based on load requirements.
- Feedback circuit: This gives feedback about on/offand faultstatus of the load.

The components chosen for all the designs should satisfy the functions of all the four basic blocks and should fulfill all the earlier outlined objectives of PCU. The details of the devices used for different designs of PCU are given in next section.

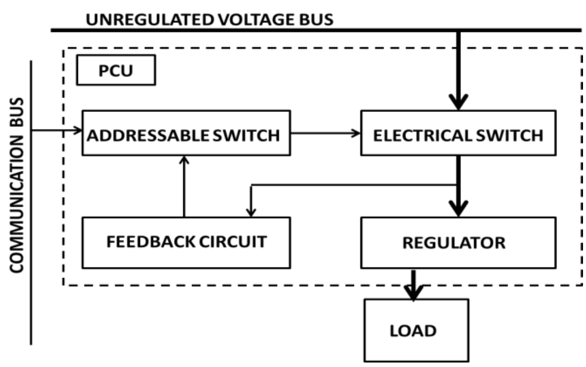

Fig 1 : Basic Block Diagram of PCU

2. COMPONENTS USED IN THE PCU DESIGN.

2.1. Electrical switch

The Electrical Switch (IPS7081)[5], used in all the designs of the paper, is a five terminal Intelligent Power Switch (IPS) with built in short circuit, over-temperature, ESD protection, inductive load capability and is capable of providing adiagnostic feedback.The special feature of providing a diagnostic feedback is utilized in all the different architectures discussed in this paper. The diagnostic feedback helps us to identify whether the load is functioning normally or is at faulty condition. Faults like open load, short circuit and over temperature can be detected from the feedback obtained.

Table 1gives the logical status of three pins of the IC; IN, OUT and DG help in determining the type of fault each load has undergone.

Table 1. Logic table for determining type of fault

OPERATING CONDITIONS	IN	OUT	DG
Normal	H	H	H
Open Load	L	H	H
Short-circuit to Ground	L	L	L
Over temperature	H	L(cycling)	L

2.2 Voltage regulator

The Voltage regulator (TPS5450) [6] is a wide input voltage range, high-output current PWM based step down DC-DC converter that integrates a low resistance high side N-channel MOSFET. Its features are-Wide Input Voltage Range: 5.5 V to 36 V, upto 5-A continuous (6-A Peak) output current,high efficiency greater than 90% enabled by 110-mΩ Integrated MOSFET Switch, Wide Output Voltage Range adjustable down to 1.22V with 1.5% initial accuracy,,18μA shut down supply current,improved line regulation and transient response by input voltage feed forward,system protected by overcurrent limiting, overvoltage protection and thermal shutdown,–40°c to 125°c operating junction temperature range. Figure 2 shows the application circuit for an input voltage of range 9v-15v to 3.3v output. This application circuit was simulated and designed using Texas Instruments utility software SWITCH PRO **[7]**

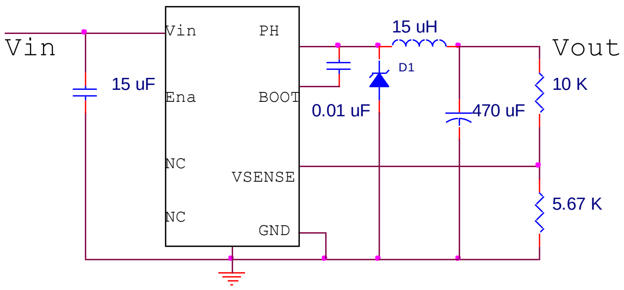

Fig 2 : Application circuit. TPS 5450

2.3 1-Wire master

The 1- Wire Master DS2482-800[8]is an I2C-to-1-Wirebridge device that interfaces directly to standard (100 kHz max) or fast (400kHz max) I2C masters to perform bidirectional protocol conversion between the I2C master and any downstream 1-Wire slave devices. Relative to any attached 1-Wire slave device, theDS2482-800 is a 1-Wire master. Internal factory trimmed timers relieve the system host processor from generating time-critical 1-Wire waveforms, supporting both standard and Overdrive 1-Wire communication speeds. To optimize 1-Wire waveform generation, the DS2482-800 performs slew-rate control on rising and falling 1-Wire edges and has a programmable feature to mask the fast presence pulse edge that some 1-Wire slave devices can generate. Programmable strong pull-up features support 1-Wire power delivery to 1-Wire devices such as EEPROMs and sensors. The DS2482-800 combines these features with eight independent 1-Wire I/O channels. The I2C slave address assignment is controlled by three binary address Inputs, resolving potential conflicts with other I2C slave devices in the system. The typical operating circuit of DS2482-800 is shown in Figure 3**.**1-Wire Master DS2482-800 is equivalent to eight DS2482-101[10]. DS2482-800 adds flexibility to the design of PCU by significantly increasing the number of loads (1-Wire Slaves) to which it can address.

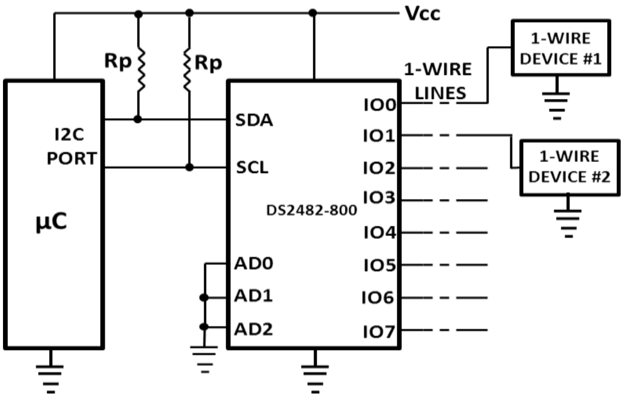

Fig 3 : Typical operating circuit

2.4 1-Wire slave

The 1-Wire Slave DS2408[9]is an 8-channel, programmable I/O 1-Wire chip. The operation is controlled over the single-conductor 1-Wire bus. Device communication follows the standard Dallas Semiconductor 1-Wire protocol. Each DS2408 has its own unalterable and unique 64-bit ROM registration number that is factory lasered into the chip. The registration number guarantees unique identification and is used to address the device in a multi-drop 1-Wire net environment. Multiple DS2408 devices can reside on a common 1-Wire bus and can operate independently of each other. The DS2408 also supports 1-Wire conditional search capability based on PIO conditions or power-on-reset activity; the conditions to cause participation in the conditional search are programmable. The DS2408 has an optional V_{CC} supply connection. When an external supply is absent, device power is supplied parasitically from the 1-Wire bus. When an external supply is present, PIO states are maintained in the absence of the 1-Wire bus power source. The RSTZ signal is configurable to serve as either a hard-wired reset for the PIO output or as a strobe for external circuitry to indicate that a PIO write or PIO read has completed.

2.4.1 Block Diagram of DS2408

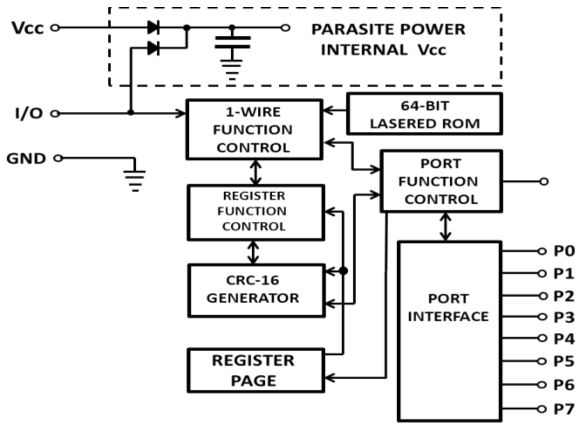

Fig 4: Block Diagram of DS2408

3. PCU COMMUNICATION

Two different communication protocols used in these architectures are -

1. I2C (Inter-Integrated circuit) Protocol [3]
2. 1-wire protocol [4][11][12][13]

3.1 I2C (Inter-Integrated Circuit) protocol

Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognized by a unique address — whether it's a microcontroller, LCD driver, memory or keyboard interface — and can operate as either a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.The I2C-bus is a multi-master bus. This means that more than one device capable of controlling the bus can be connected to it.

In this particular design the I2C protocol is only used in the communication between the microcontroller and the chip DS2482-800 which is the 1-Wire Master and a bi-directional Protocol convertor from I2C to 1-Wire.1-Wire Master controls the operations of PCU according to the instructions given by the microcontroller in I2C to it using 1-Wire Protocol. As Microcontrollers cannot communicate directly with the 1-Wire slave devices we have to use a protocol convertor DS2482-800.

3.2 1- Wire protocol

Most of the communication circuitry in the design follows 1-wire protocol**.**Dallas 1-Wire devices are unique in a way that only one wire in addition to ground is needed to communicate with a device. Power supply and communications are handled through only one connection. To communicate with a Dallas 1-Wire device, only one general purpose I/O pin is needed.

1-Wire is a device communications bus system designed by Dallas Semiconductorthat provides low-speed data, signaling and power over a single signal. 1-Wire is similar in concept to I²C, but with lower data rates and longer range. One distinctive feature of the bus is the possibility to use only two wires: data and ground. It uses an internal 800pF to store charge during communication. Communication is asynchronous and half-duplex, and it follows a strict master-slave scheme. One or several slave devices can be connected to the bus at the same time. Only one master should be connected to the bus.The bus is idle high, so there must be a pull-up resistor present.All devices connected to the bus must be able to drive the bus low. An open-collector or open- drain buffer is required if a device is connected through a pin that cannot be put in a tri-state mode.Signaling on the 1-Wire bus is divided into time slots of 60µs. One data bit is transmitted on the bus per time slot. Slave devices are allowed to have a time base that differs significantly from the nominal time base. This however, requires the timing of the master to be very precise, to ensure correct communication with slaves with different time bases.

Every 1-Wire device contains a globally unique 64 bit identifier number stored in ROM. This number can be used to facilitate addressing or identification of individual devices on the bus. The identifier consists of three parts: an 8 bit family code, a 48 bit serial number and an 8 bit CRC computed from the first 56 bits. A small set of commands that operate on the 64 bit identifier are defined. These are called ROM function commands.

All 1-Wire devices follow a basic communication sequence

1) The master sends the "Reset" pulse.
2) The slave(s) respond with a "Presence" pulse.
3) The master sends a ROM command. This effectively addresses one or several slave devices.
4) The master sends a Memory command.

Note that to reach each step, the last step has to be completed. It is however not necessary to complete the whole sequence. IC DS2482-800,the 1-Wire Master, converts I2C protocol to 1-Wire protocol.IC DS2408 is 1-Wireeight Channel Addressable Switch, is a 1-Wire Slave,primarily used for PCB identification.Therefore each load will have a unique address and can be accessed using thisIC. The addressing of loads, controllingoperations related to power and faults mentioned are completed using the1-Wire protocol.

4. CASE STUDIES

The basic functional block diagram of PCU and its master is shown in Figure 5.The eight I/O lines of DS2482-800 is similar to eight 1-Wire Bus.1- Wire Slave devices (DS2408 Addressable Switch) can be connected to each of these I/O lines.

The value of N in Figure 5 depends on total capacitance of 1-Wire Bus and 1-Wire Slave[4]. The number of 1-Wire slaves to be connected and the drive capability of 1-Wire Bus are heavily associated with the total capacitance load on the 1-Wire Bus, as each 1-Wire slave device can add about 100pF of capacitance to the 1-Wire Bus.

With standard speed of 1-Wire Bus which is 15.3kbps the total capacitive load of the 1-Wire bus should not exceed 1nF, otherwise the passive pull-up on threshold VIL1 may not be reached in the available time. With Overdrive speed which is 100kbps the capacitive load on the 1-Wire bus must not exceed 300pF [4][11][12]. Cable length will also add to the 1-Wire Bus capacitance. Not considering the length of cable, each 1-Wire Bus from the DS2482-800 can service ten 1-WireSlaves in Standard Mode and Three 1-Wire Slaves in Overdrive mode.

4.1 Circuit operation:

- Microcontroller (µC) initializes the 1-Wire master DS2482-800 for I2C communication.
- Depending on the operational requirements of the satellite µC gives instructions to the 1-wire master DS2482-800to turn ON the required loads.
- DS2482-800 initializes 1-Wire communication

  and communicates with its slaves (DS2408) one by one according to instructions from µC.
- After addressing each slave it takes feedback of its status.
- The status feedback is given to µC, if feedback signals a fault, that particular load is turned OFF and it continues to be in the same state till the fault is cleared.
- Feedback will be taken in regular intervals to monitor the ON/OFF status and Fault status which is reported to µC.
- Once the load recovers the fault it is turned ON if necessary.

The above mentioned steps will be a continuous process.

Typical functional diagram of each PCU block in Figure 5is given in Figure 6

From Typical functional diagram of PCU in Figure 6we can come to a conclusion that all the four basic blocks of PCU with reference to Figure 1 are satisfied viz.

- DS2408 – Addressable Switch
- IPS7081 – Electrical Switch
- TPS5450- Regulator
- DS2408+IPS7081- Feedback Circuit

All the objectives,mentioned below, of PCU are satisfied by the design

- TPS5450supplies regulated power to various satellites loads.
- IPS7081 continuously monitor the working of all loads through feedback via DS2408.
- µC located on main power board identifies the type of fault from data given by IPS7081 via DS2408 and DS2482-800 and gives necessary instructions to DS2482-800.

4.2 Case 1

Let the system operate at normal speed of 15.3 kbps**.**

As explained earlier, the number of one wire slaves that can be connected to each bus depends on the net capacitance of the slave and the bus. At the mentioned speed the number of slaves that can be connected to each bus is limited to ten. The value of capacitance not to be exceeded is 1nF. So in this particular design the maximum number of slaves that can be connected to DS2482-800 is limited to 80 i.e. 10 in each I/O line as there are 8 I/O lines the total number is 80 as shown in Figure 7

4.3 Case2

Let the system operate at the normal speed of 15.3kbps. Let the number of loads be >80**.**

Since the system is operating at normal speed but with a higher number of loads (> 80). 1-wire net capacitance connected to each bus cannot exceed the value of limit capacitance (1nF) or ten loads per bus excluding bus capacitance for the given speed; hence the solution is to use a microcontroller with two I2C master ports (E.g. PIC24FJ128GA010). Using this, the objectives mentioned can be satisfactorily achieved as shown in Figure 8.

4.4Case 3

Let the system be operating at overdrive mode of 100 kbps.

Since the system is operating at overdrive speed the net capacitance of 1-Wire Bus must not exceed the value of limit capacitance (300pF) or three loads per bus excluding bus capacitance for overdrive speed. This design can be used where the operational speed is more significant for loads but the disadvantage of the design is we have to compromise with the number of loads. As shown in Figure 9we can only use this design for 24 loads excluding bus capacitance.

4.5 Case 4

Consider the case where there are certain loads which have to be operated at overdrive mode and other loads which are to be operated at standard mode**.**

In this case the solution is to use a microcontroller with two I2C master ports. One I2C master port is connected to 1-wire master (DS2482-800) which operates at overdrive speed which drives those certain loads which demands for higher operating speeds and another 1-wire master which drives the loads at standard speeds. So the maximum number of loads that can be operated is 104, out of which 24 operates at overdrive speed and 80 operating at standard speed. This is shown inFigure 10**.**

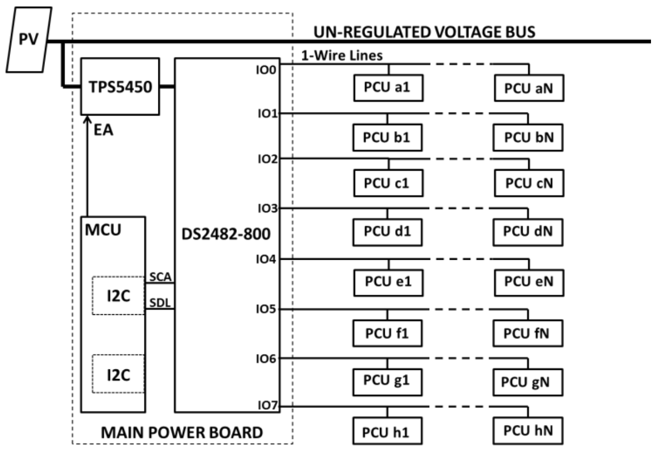

Fig5 : Basic functional block diagram of PCU

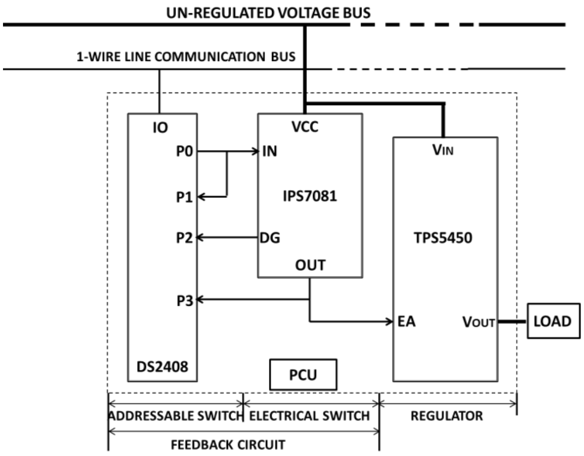

Fig 6: functional diagram of a PCU

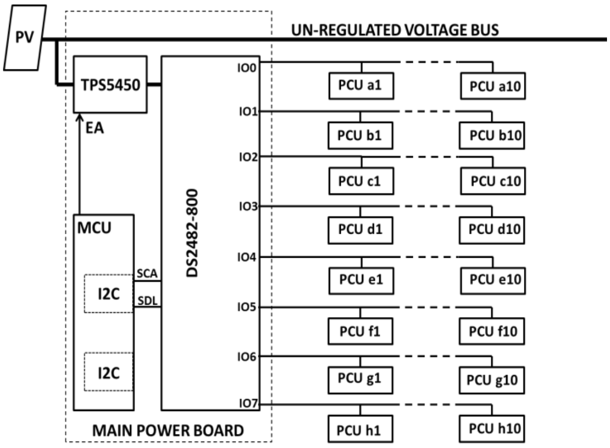

Fig 7:Typical operating circuit case 1

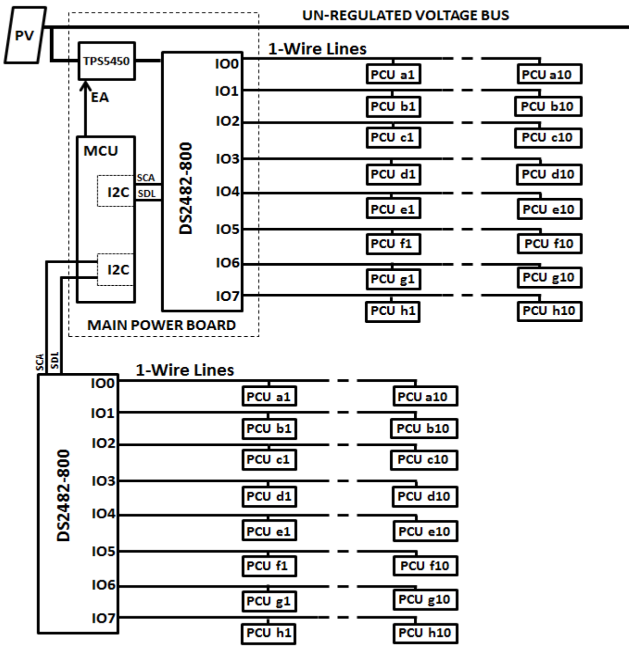

Fig 8: Typical operating circuit case 2

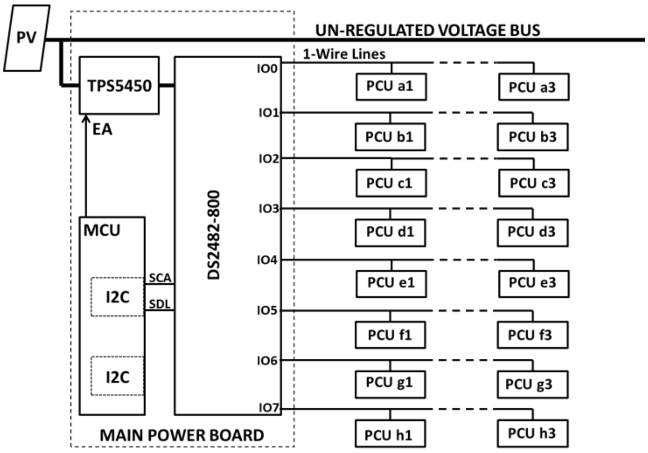

Fig 9: Typical operating circuit case 3

5. RESULT

The preceding section clearly attains all the objectives of PCU in each of its architecture. This paper successfully proposes several novel architectures of power conditioning units in a micro-satellite for different communication speeds and also based on the number of loads housed on a satellite. The paper also satisfactorily shows the flexibility of the power conditioning unit when the number of load increases or there is a demand for higher communication speeds, thus overcoming the design limitations of its previous versions.

Although these different power conditioning units' architectures were specifically designed for a micro-satellite, the same architectures with minor changes can be utilized for

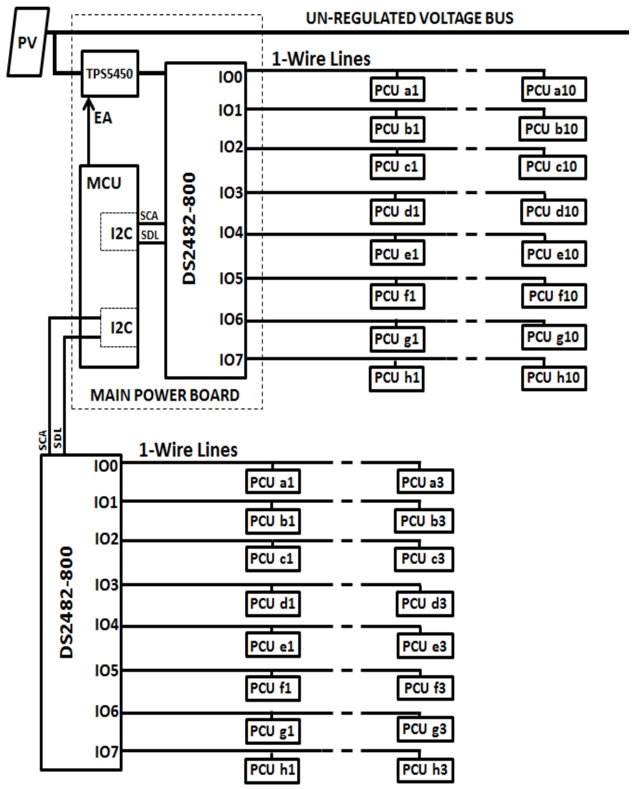

Fig 10: Typical operating circuit case 4

all the earlier outlined objectives to any system that has multiple communicable loads. Thus, it can be concluded that this paper proposes several architectures of a power conditioning unit (for different number of loads and communication speeds) that can be utilized in any electrical system having multiple communicable loads and also that figure 5 & 6, basic block diagrams of PCU, will be one of the standard building structures for every PCU henceforth designed.

6. ACKNOWLEDGMENTS

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