Embedded Data Acquisition System for High Energy Cosmic Ray Experiments

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ABSTRACT

In general, High energy Cosmic ray experiment deal with a large number of detector signals. A few prime signal parameters are need to be measured, recorded on a coherent detection of signals, called trigger. Triggers are random in time. It is also necessary to monitor continuously the performance of the detectors. Our project is aimed at developing a prototype of data acquisition system (DAQ) catering the need of such experiments. The Time-Over-Threshold measurement of participating pulses along with Time-stamp is recorded on a valid trigger and pulse counting rates, trigger rates are need to be monitored periodically. The prototype is planned for eight detector signals.

General Terms

Data acquisition system,embedded system

Keywords

FPGA,cosmic rays,data acquisition

1. INTRODUCTION

The extra-terrestrial Cosmic ray sources are studied directly by launching detectors in a satellite to detect the primary particles emitted by the sources. The rates of particles fall rapidly as its energy increases. Due to the restricted size of detectors in satellite, detection of high energy particles from the source becomes inefficient. These primary particles interact with earth atmosphere and produce a shower of secondary particles called air shower i.e. amplified detection area. Thus ground based experiments deploy a large number of particle detectors to sample cosmic ray showers and are efficient in detecting high energy particles by indirection detection of shower. The particle detector converts the energy to electrical signal and its pulse height is proportional to the sampled energy of the particle shower. Generally, high energy cosmic ray experiments deal with a large number of signals. We have planned to develop a prototype of 8 channel hardwired DAQ using Altera FPGA with minimum dead time for such experiments. On an external trigger, the DAQ system needs to process the signals, measure and record signal parameters like Time-Over-Threshold (TOT) of all 8 pulses along with time stamp, trigger rate and relevant event header. The counting rates of pulses are recorded periodically as monitoring data of detectors along with time stamp and monitor header. The TOT i.e. pulse width can be expressed as a mathematical function of its pulse height. The project is designed for slow pulse from adetector and pulse width is of the order 10s of micro sec. The pulse width of interest can be precisely and easily measured using simple digital circuits as compared to pulse height measurements. The measured data on a trigger and monitored data are transferred to a PC via USB. The data is stored in respective files for on-line or offline analysis.

2. IMPLEMENTATION

The design specification and functionality of the project are explained below.

2.1 Design Specification

- Time over threshold (TOT) of 8 analog signals need to be supported.
- TOT of 8 pulses are to be recorded on an external event trigger. TOT measurement is done with 16 bit dynamic range and resolution of 50ns.
- Time stamp is recorded with event and monitoring data up to days with a microsecond resolution.
- Monitoring of 8 signals periodically
- Serial connectivity using USB for data transfer and control.
- Graphic user interface in PC for control and recorded data presentation.

2.2 Functionality

The overall function is depicted in the block diagram of Figure 1. The system mainly consists of:

- Time Over Threshold converter

Analog pulses from the detector channels are translated into TOT digital signal using comparator. The front end card is designed for 8 channels. A manually adjustable common threshold control is provided for all the 8 channels. The digital signals in LVDS form are brought out in the FRC connector to the processing and DAQ card.

- Embedded Processing and DAQ system

2.3 The processing, monitoring and data acquisition logics are embedded into an Altera FPGA chip. The common bus architecture is used for connecting all the Event processing and Monitor processing modules. . The Event processing modules include Header, Event record number, time stamp, TOT data of 8 channels and Monitor Processing module are Header, Monitor record number, timestamp, Pulse rate of 8 channels. Bus controller controls the protocol during event reading and monitor reading cycle. The wait states are added to read cycle whenever processing modules or USB FIFO is not ready. The external trigger is accepted if system is not busy and latches the data in all event processing modules. Similarly a periodic monitor timer latches all the Monitor processing modules if system is not busy. The system is vetoed till the current process is completed. The event read

daisy chain and monitor read daisy chain are configured connecting respective processing modules in a desired sequence. The external trigger initiates the event read cycle sequencing desired number of write cycles to USB FIFO device host interface enabling the 8 bit data from selected processing module in the event read daisy chain onto common bus. The data from monitor processing modules are written to USB FIFO in monitor read cycle. The event data and monitor data are embedded with proper header.

- USB FIFO interface

The small add on board is designed using USB device FTDI make FT-245R chip and it supports a simple parallel 8bit half duplex communication between PC and embedded DAQ using simple IO protocol. The event data and monitor data are written to transmit FIFO of USB device by the embedded DAQ on each accepted trigger. The PC polls for USB data and extracts event and monitor data into separate files.

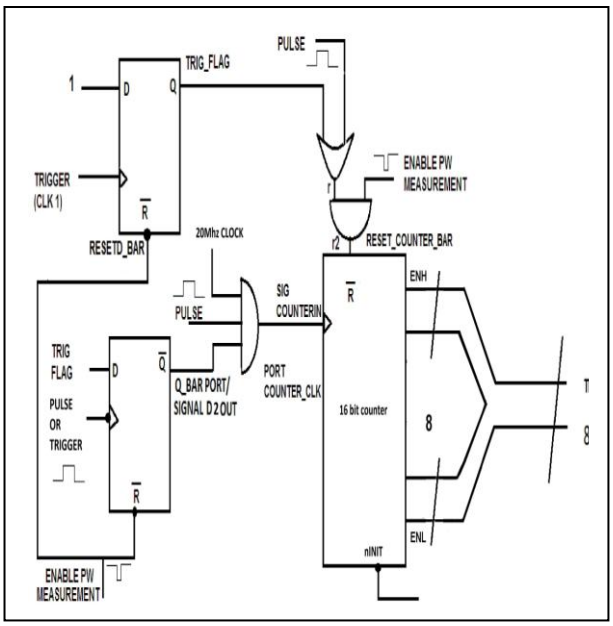

Figure 1: Basic block diagram

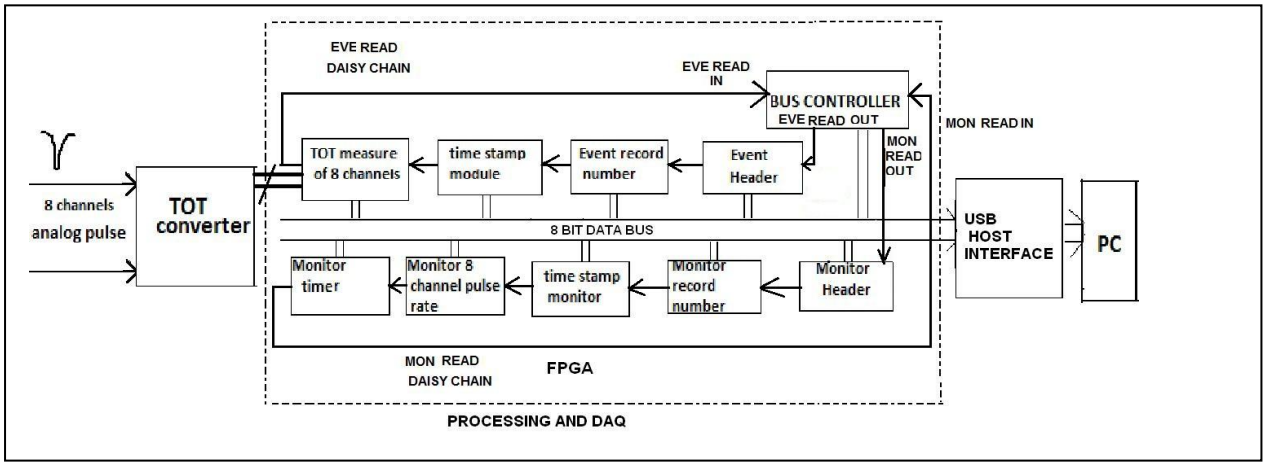

Figure 2.:Block diagram of pulse width

- User Interactive Software:

The user interactive software is planned for control and data transfer between DAQ hardware and PC. It is planned to be developed using FTDI drivers under Visual C environment.

3. SIMULATION AND RESULTS

The structural and modular approach is followed in bringing up the project. The codes were developed for each of the processing modules and validated by simulation. The codes were written in VHDL, compiled using Altera Quartus II and simulated using ModelSim-Altera. The components tested are detailed here after.

3.1 Pulse width measurement

Referring to Figure 2,the block diagramof pulse width measurement,the 16 bit counter counts the 20 MHz clock during a TOT pulse width and cleared at the trailing edge of pulse. The clearing is vetoed if there was a trigger. The data ready flag is set at either at trailing edge of pulse or trigger. The lower and higher byte of data is mapped to common bus during read cycle. The nINIT signal at the end of read will enable the logic for subsequent measurement of pulse width. The simulation result for one channel is shown in Figure 3.

3.2 FTDI FT-245 USB interface

The write read cycle of USB device interfacing is tested by simple IO port in loop with proper protocol is coded into FPGA and tested by simulation as well as by the hardware. The interface has been validated by sending and receiving the block of data between PC and IO port. The simple data transfer program in PC was developed in Visual C. Card circuit diagram is as shown in Figure 4. The protocol signals nTXE and nRXF are monitored for data transfer.

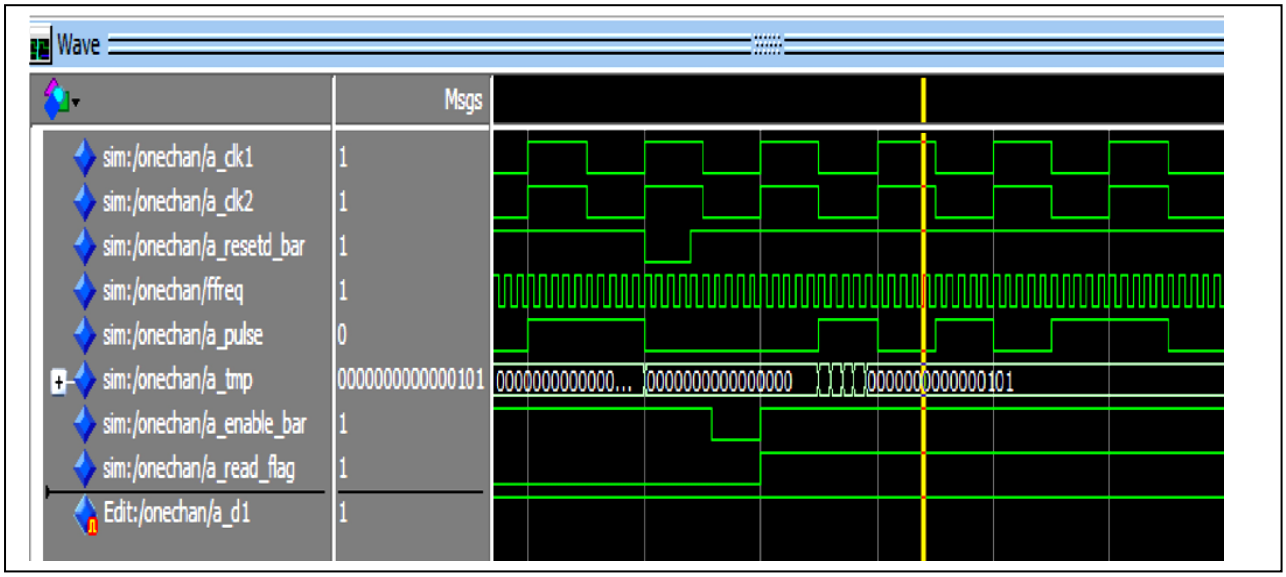

Figure 3. Simulation of pulse width measurement.

The simulation of the USB interface module is as shown in Figure 5.

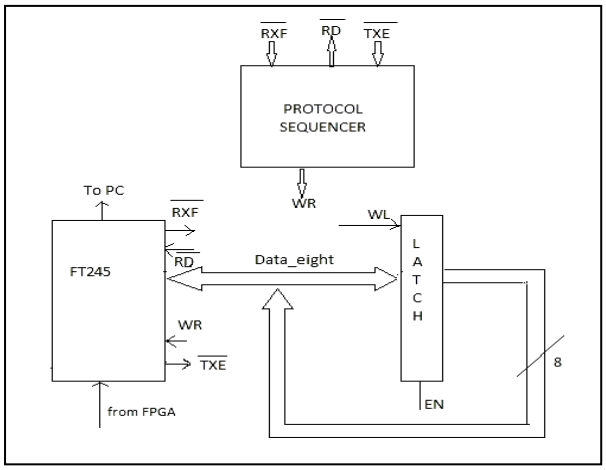

Figure 4. USB interface circuit diagram.

3.3 TOT converter

A 8 channel TOT converter using comparator IC LMH 7220 is under development and one schematic is shown in figure 6.

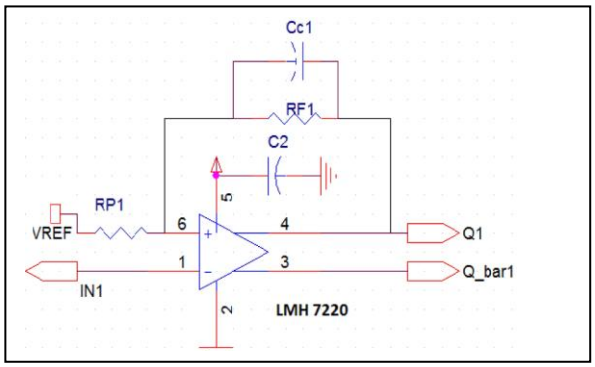

Figure 6. Comparator design.[1]

The threshold is variable within ± 1V and module supports both polarity pulses except for output logic inversion for positive polarity pulses.

3.4 Time Stamp

Event and Monitor data includes time stamp up to days with a resolution of 100 micro sec and logic diagram is shown in fig 7. The basic clock of 10 KHz is derived from a stable oscillator and the time counter is synchronized with a GPS. The time stamp is a 32 bit word and read by 4 read cycles byte wise.

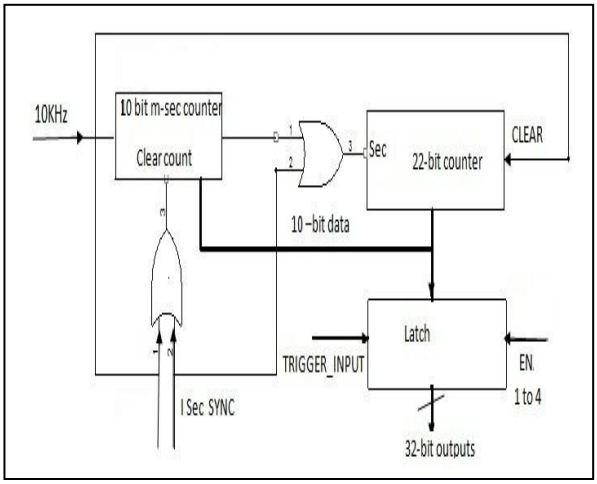

Figure 7. Event time stamp circuit diagram.

3.5 Bus Controller

Bus controller mainly handle's triggers as well as read out cycles. The external trigger is connected to Eve trigger and Monitor timer initiates Mon trigger. These trigger initiates respective latches to freeze the data in the processing modules. Trigger sensor senses the trigger with set priority. Eve trigger is at higher priority than Mon Trigger. The accepted trigger activates Read OUT signal in the daisy chain to start read cycle and reading endswhen it senses respective

Read IN signal. The Read cycle sequencer generates WR and Read clock signals in desired sequence to record the data in USB FIFO and to select the next data in daisy chain. The wait states are added if needed by the sequencer decided by looking at status of nTXE and Data ready signals.

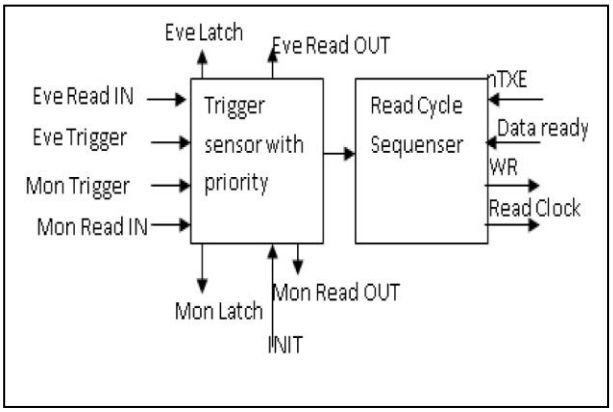

Figure 8. Bus controller circuit diagram.

4. CONCLUSION

The over all conceptual design is completed. The PCB for the front end 8 channel TOT board is under progress.The processing modules are individually coded and validated by simulation using Altera Quartus II and ModelSim. The project is planned to implement using Altera Cyclone III FPGA and schematic for the FPGA board is started. The codes are planned to be tested in Cyclone IV based Altera DE2-115 evaluation kit. The data transfer between USB device FT245 and PC is tested. The components of the project are to be burnt into FPGA and to be validated its functionality. Finally all the components are planned to be integrated and test the over all aspects of the system. On satisfactoty performance of integration, system will be exposed for field test with detector signals and physics data will be recorded.

5. ACKNOWLEDGMENTS

We take this opportunity to express our sincere gratitude towards Mr. S.S.Upadhya and Mr. Sudersan from the Tata Institute of Fundamental Research (TIFR), Colaba for their valuable guidance, engagement and help during this course of the project. We would also like to thank Mrs. Anuradha Mangle from the department of Electronics andTelecommunication of Fr. C. Rodrigues Institute of Technology, Vashi for her assistance, help, and valuable inputs.

We would also like to thank our Head of Department Dr. Milind Shah for his help and guidance during different stages of the project.

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