Temperature Dependence of Propagation Delay Characteristic in LECTOR based CMOS Circuit

Preeti Verma R. A. Mishra

Electronics & Communication Engineering Department, Motilal Nehru National Institute of Technology, Allahabad - 211004

ABSTRACT

Propagation Delay of CMOS circuit depends upon several parameters such as threshold voltage, supply voltage, cell size. Variation of threshold voltage may result in temperature inversion effect thus reducing the cell delay as temperature increases. Integrated circuits operating at scaled supply voltage consume low power at the cost of reduced speed. This paper presents the study of effect of temperature on propagation delay of LECTOR based NAND gate circuit and comparing that with conventional design for a temperature range 0f 25°C to 105°C.

Keywords

Leakage/Sub threshold current, threshold voltage, LECTOR circuit.

1. INTRODUCTION

The performance of the digital circuit depends upon the path delay in the circuit and the path delay depends upon the delay of cells and nets. Digital circuit designing typically assumes that with decreasing voltage and increasing temperature the cell delay increases but this assumption fails for low voltage applications because cell delay can decrease with increasing temperature values. This happens due to competitiveness between mobility and supply voltage to dominate cell delay. This phenomenon is called inverted temperature dependence [1].

LECTOR (Leakage Control Transistor) [2] is a technique for designing CMOS gates which significantly cuts down the leakage current without increasing the dynamic power dissipation. LECTOR yields better leakage reduction as the threshold voltage decreases and hence aids in further reduction of supply voltage and minimization of transistor sizes.

Propagation delay of a CMOS circuit is a function of active transistor's drain current and that is determined by temperature sensitive set of device parameters. Heat dissipation is a critical issue in circuit design. The temperature rise in a device can be described by the expression [3, 4]

$$T_C = T_0 + R_T I_d V_{ds} \tag{1}$$

Where I_d & $V_{ds.}$ are Drain current and Drain-source voltages respectively, R_T is the thermal resistance (it is replaced by thermal impedance of the device for dynamic case) and T_o is the ambient temperature.

There are many benefits for MOSFET operating at low temperatures, such as the improvement of sub-threshold swing, increase of carrier mobility, higher saturation velocity and operation speed, decreased leakage current, improved electro-migration and heat dissipation.

The two main parameters which are affected by temperature are-Threshold voltage & Carrier Mobility. As the temperature increases the threshold voltage and carrier mobility decreases but the drain current increases [5].

Threshold voltage is given by the following expression

$$V_T = \emptyset_{GS} - \frac{Q_{SS}}{C_{OX}} + 2\emptyset_F - \frac{Q_B}{C_{OX}} \tag{2}$$

Where Q_B is charge per unit area contained within surface depletion region given as $Q_B = -\sqrt{(2qN_A\varepsilon_{S_i}.| - 2\emptyset_F + V_{SB}|)}$, V_{SB} is source to substrate voltage,Q_{SS} is surface charge density per unit area, metal semiconductor work function is represented by $\emptyset_{GS}$,oxide capacitance per unit area is given as $C_{OX} = \varepsilon_{ox} / t_{ox}$, $\emptyset_F$ is Fermi potential, which is a function of doping denotes the difference between the intrinsic Fermi level and the Fermi level.

For a p-type semiconductor $\emptyset_{FP} = \frac{KT}{q} ln\frac{n_i}{N_A}$

Whereas for a n-type semiconductor (doped with a donor concentration N_D is given by $\emptyset_{Fn} = \frac{KT}{q} ln\frac{n_i}{N_D}$

Where n_i is given as $n_i^2 = A_0 T^3 \varepsilon^{-E_{GO}/kT}$, K is the Boltzmann constant, q denotes the unit charge, n_i is intrinsic concentration, N_A & N_D are acceptor & donor concentration respectively and Differentiating equation (2) with respect to temperature results

$$\frac{dV_T}{dT} = \frac{d\emptyset_F}{dT}[2 - \frac{1}{C_{OX}}\frac{Q_B}{2\emptyset_F}] \tag{3}$$

Where $$\frac{d\emptyset_F}{dT} \cong \pm\frac{1}{T}[\frac{E_{G0}}{2q} - \emptyset_F] \tag{4}$$

E_{GO} is the energy band gap at 0°K in electron volts.

Thus the intrinsic concentration n_i varies with temperature and so the Fermi potential ($\emptyset_F$) too.

The variation of mobility with temperature can be defined as

$$\mu(T) = \mu(T_0)(\frac{T}{T_0})^k \tag{5}$$

The mobility shows a variation of $T^{1.5}$ for the temperature range of -55 ^{0}C to +125 ^{0}C.The variation of mobility with temperature can be taken to a good approximation by 1/T dependence. Thus

$$\frac{1}{\mu_{eff}}\frac{d\mu_{eff}}{dT} \cong -\frac{1}{T} \tag{6}$$

Where μ(T) is the mobility at temperature T, μ_{eff} is the effective mobility, T_0 is reference(room) temperature in Kelvin, k is small positive constants.

And the drain current varies in opposite manner as [6, 7,8]

$$I_d \propto \mu(T)(V_{dd} - V_T(T))^\alpha \tag{7}$$

Where α is positive technological constant [9]

Equation (7) shows that the drain current varies directly with temperature i.e. the current increases with increasing temperature. Thus drain current increases with lower threshold voltage but drain current decreases with lower mobility. So at a given voltage and temperature values the final drain current is determined by the dominating trend. Fig 1 shows the variation of threshold voltage (V_T) with temperature [10]. It is very clear from this figure that the threshold voltage is decreasing with increasing temperature.

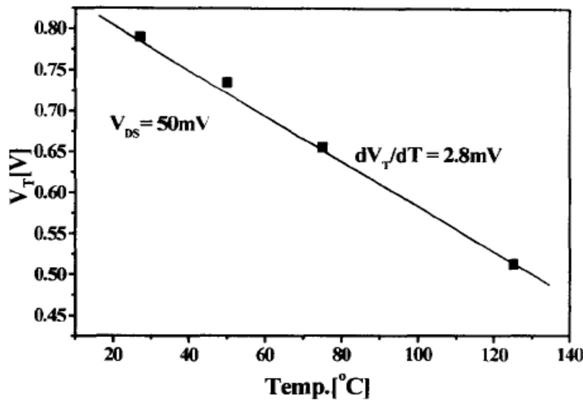

Fig 1: Threshold voltage Vs temperature

The source-to-drain or channel conductance g_{SD} of n-channel and p-channel MOS transistors decreases as the temperature increases .In each case , the channel conductance for small drain voltages is given by [11 , 12]

$$g_{SD} = \pm\mu_{eff} \frac{W}{L} C_O(V_G - V_T) \quad (8)$$

where positive sign is taken for n-channel and the negative sign for p-channel devices; μ_{eff} is the effective mobility of carriers in inversion layer, W is the channel width, L the channel length, and V_T is the threshold voltage. The temperature dependence of transconductance parameter can be derived from temperature dependence of mobility and threshold voltage variation.

Differentiating the above equation (8)

$$\frac{1}{g_{SD}}\frac{dg_{SD}}{dT} = [-\frac{1}{\mu_{eff}}\frac{d\mu_{eff}}{dT} - \frac{1}{(V_G - V_T)}\frac{dV_T}{dT}$$

The temperature coefficient (T.C.) of channel conductance is defined by $T.C. = \left[\frac{1}{r_{SD}}\frac{dr_{SD}}{dT}\right]100 = \left[-\frac{1}{g_{SD}}\frac{dg_{SD}}{dT}\right]100\ [\%/°C]$

Depending upon the gate voltage the temperature coefficient of device can be positive, zero or negative [13].

The variation of propagation delay τ_P is therefore given by

$$\tau_P \propto \frac{C_{out}\,V_{dd}}{I_d} \equiv \frac{C_{out}\,V_{dd}}{\mu(T)(V_{dd} - V_T(T))} \quad (9)$$

Thus as the carrier mobility (μ) decreases, the performance degrades , while the decrease in threshold voltage V_T makes the device faster. It can be concluded from equation (3) and (5) that the threshold voltage and mobility decreases as the temperature increases.

Fig. 2 shows the leakage current for several technologies for different temperatures [14]. It could be concluded from this figure that the sub-threshold current (I_{SUB}) is increasing with temperature for every process technology .

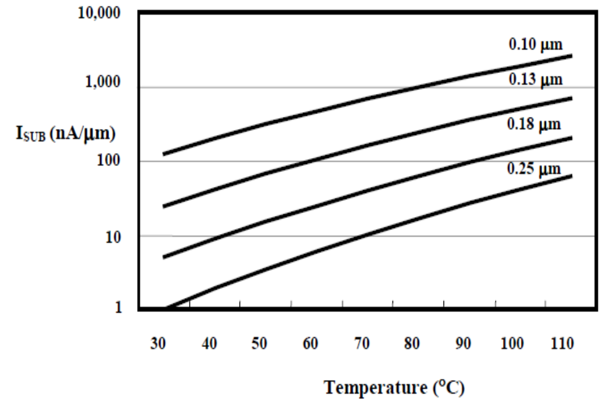

Fig 2: I (Sub threshold) (VGS=0) trend as a function of temperature. Courtesy of Vivek De, Intel

2. TEMPERATURE DEPENDENT MODELS (BSIMV3)

2.1 Model for temperature dependence of mobility

There are several empirical formulations to describe the mobility as function of process parameter and bias conditions. In BSIMv3 the temperature dependence of mobility is described by a second order polynomial that has parameters U_a,U_b,U_c and these parameters are linear function of temperature [15, 16, 17]. For mobMod =1, the mobility model, including temperature effects, is given as follows :

$$\mu_{eff} = \frac{\mu_{0mmmmk}\ (T/T_{NOM})^{ute}}{1+(U_a(T)+U_c(T)V_{bseff})\left(\frac{V_{gsteff}+2V_T}{T_{OX}}\right)+U_b\ (T)(\frac{V_{gsteff}+2V_T}{T_{OX}})^2}$$

Where

$U_a(T)=U_A+U_{A1}(T/T_{NOM}-1)$

$U_b(T)=U_B+U_{B1}(T/T_{NOM}-1)$

$U_c(T)=U_C+U_{C1}(T/T_{NOM}-1)$

Where parameter μ_0 ,U_A, U_{A1} ,U_B,U_{B1},U_C,U_{C1} and U_{TE} could be extracted from the measured I-V data and T is the temperature in Kelvin. T_{NOM} is the nominal temperature. At this temperature the model parameter μ_0 , U_A,U_{A1} ,U_B and U_C are extracted.

B. Modeling of temperature dependence of the threshold voltage

Temperature model for threshold voltage (V_T) used in BSIM 3 is as follows [15, 16, 17].

$$V_T(T) = V_T(T_{NOM}, L, V_{ds}) + \left(K_{T1} + \frac{K_{T1L}}{L} + K_{T2}V_{bs}\right)(\frac{T}{T_{NOM}} - 1)$$

where V_T (T_{NOM}, L ,V_{ds}) is value of threshold voltage at T_{NOM}.The value of K_{T1}, K_{T1L}, and K_{T2} parameters is obtained room the experimental data. To improve the fitting a minor term K_{T1L}/L is introduced.

3. EXPERIMENTAL RESULT

The analysis is done using Synopsys tool HSPICE (180nm TSMC) for the circuits LECTOR NAND Gate and Conventional NAND Gate for a temperature range of 25 to 105°C.The analysis is done for the sub-threshold conduction region.Table1 is showing the propagation delay values in picoseconds for different temperatures . It could be clearly seen

from the Table 1 and the Fig 3 that the propagation delay of these CMOS circuits decreases as the temperature increases.

Table 1: Propagation delay for different temperatures obtained using HSPICE

Propagation Delay (picoseconds) Variation with Temperature					
CMOS circuit Type	Temperature (^{0}C)				
	25	45	65	85	105
Convention al NAND gate	15.81	15.0 2	14.1 2	13.26	12.85
LECTOR NAND gate	23.25	22.2 0	20.0 3	18.11	17.99

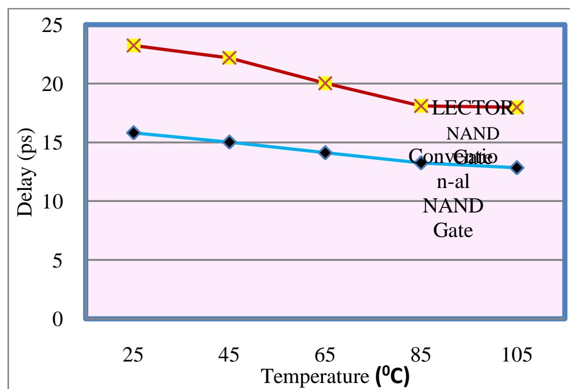

Fig 3: Variation of propagation delay of LECTOR NAND gate and Conventional NAND GATE with temperature.

4. CONCLUSION

The key finding of the analysis is that ,with increasing temperature Propagation delay LECTOR based CMOS NAND gate and Conventional NAND gate decreases approximately linearly. From the Results it is observed that the reduction in delay for conventional NAND gate is 18.72% while it is 22.62% in case of LECTOR NAND gate. Even though the delay of LECTOR circuit is more than that of conventional circuit but the reduction % of delay is more in LECTOR circuit in comparison to the conventional circuit

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