Impact of Width Variation of Global Inductive VLSI Interconnect Line

Diwakar Singh Gargi Khanna Rajeevan Chandel

Department of Electronics and Communication, National Institute of Technology, Hamirpur, Hamirpur (H.P)-177005, India

ABSTRACT
In this paper the impact of width variation is being addressed on transition time, power dissipation and crosstalk noise in coupled inductive lines for different switching patterns. The finding of simulation reveals that there is first decrease in transition delay and then it increases afterwards. It is also observed that power increases slowly with width increasing and also observed the crosstalk noise at the victim line for the increase in width.

Keywords
Power Dissipation, Inductive VLSI Interconnect Line, Signal Skew.

1. INTRODUCTION
The distribution of clock and other signals is the main function of interconnect of the wiring systems and also provide power/ground to and among the various systems on the chip. Among wiring systems global interconnect play major role on the chip. Due to aggressive scaling of device dimensions into the nanometer regime has led to a considerable reduction in gate delays. However, due to less aggressive interconnect scaling, wire delays have not reduced in proportion to gate delays. Hence, wire delays and especially the global interconnect delay, now contribute significantly to the total circuit delay. These advances have given rise to a number of serious concerns and associated challenges especially into the sub-100 nm regime which were not significant in the past. Maintaining tolerable signal integrity and accurate timing characteristics is a key factor for the proper operation of high performance digital integrated circuits. While the performance of CMOS devices has improved dramatically, aggressive scaling of interconnect dimensions has resulted in a number of critical issues which degrade chip performance significantly. Therefore, optimization and efficient design of interconnect networks is the most important task for VLSI circuit designers [1], [2]. The current trends of chip designing requires higher aspect ratio and smaller spacing between signals lines, which results in coupling capacitance to become larger than line to ground capacitance. Furthermore, it is not possible to neglect the on-chip self inductance and mutual inductance because of faster signal rise/fall time (signal slew), higher operating frequency and usage of wider and low resistive wires especially in global interconnects [3]-[5]. Also the signal transition time and switching patterns of signal lines affect the coupling behavior [6]. Due to presence of these inductive effects, the new generation VLSI designers have been forced to model interconnects as distributed transmission

lines [7]-[8]. Power and parameters are important factors in designing interconnect. Clock distribution networks can dissipate a large portion of the total power dissipated within a synchronous IC, ranging from 25% to as high as 70% [7]-[9]. On-chip interconnect now dominates the circuit delay and power dissipation characteristics of high performance ICs. Interconnect design has, therefore, become an important issue in the IC design process.

The reduction in delay and power can be obtained with the optimization of the interconnect width [10]. In previous research it is focused that matching condition at driver and load end plays important role in reducing transition time delay through interconnect [7]-[16]. The load at the far end of interconnect is modeled by an equivalent parasitic capacitance of the following gate. The work reports that delay uncertainty and clock skew of signal lines change significantly in the presence of on-chip inductance. In this paper, we present the variations of transition time delay and power dissipation with respect to the interconnect width. Further, the investigation about the effect of jitter and skew been done on the crosstalk.

Following this introduction, section II describes the simulation set up and extracted parameters for the simulations. Transition time for signal at the far end of an RLC interconnect is given in section III. Section IV and V give the impacts of width variation of interconnect line on power dissipation and cross talk noise in a victim line respectively. Finally, section VI concludes the paper with a brief overview of this work.

2. MODEL PARAMETERS EXTRACTION AND SIMULATION SETUP
In this work, we consider a two-line bus structure. Each line is driven by an inverter and the far end is connected to the passive load (capacitance). We consider each of 5mm as the length of global interconnects line falls within the range. The whole simulation environment is created based on 70 nm technology node. Table 1 gives interconnect parameters as given by PTM for this technology node. Here, T, $W_{\min}$, $S_{\min}$, and T_{ins} are wire thickness, minimum wire width, spacing and insulator thickness respectively. Using the parameters in Table I and PTM parameters, we have extracted resistance, line inductance, mutual inductance, ground and coupling capacitance. The inverter is driving the RLC transmission line which is terminated by a passive load (capacitance) as shown in Figure 1. Representation of an interconnect line is shown physically in Fig. 1(a), while, by its equivalent RLC model in Fig. 1(b). It is assumed that leakage conductance 'G' equals 0,
which is true for most insulating materials such as SiO_2, sapphire etc. R_l, L_l, and C_l, are the total resistance, inductance,
and capacitance of the line, respectively. The line parameters R_l L_l, and C_l, are given by $R_l=Rl$, $L_l=Ll$ and $C_l=Cl$ respectively, where R, L and C are the resistance, inductance, and capacitance per unit length of interconnect and l is the length of the line. The leakage conductance of the line G is neglected since at current operating frequencies the capacitive impedance dominates the parallel semiconductor conductance. R_{tr} is the equivalent output

resistance of the gate driving interconnects. C_L is the load capacitance which is considered by [7-14].

Table I
Interconnect Parameters Used For Simulations And Analysis

W(µm)	S(µm)	H(µm)	ILD Thickness(µm)	ε_r
0.45	0.45	1.2	0.2	2.2

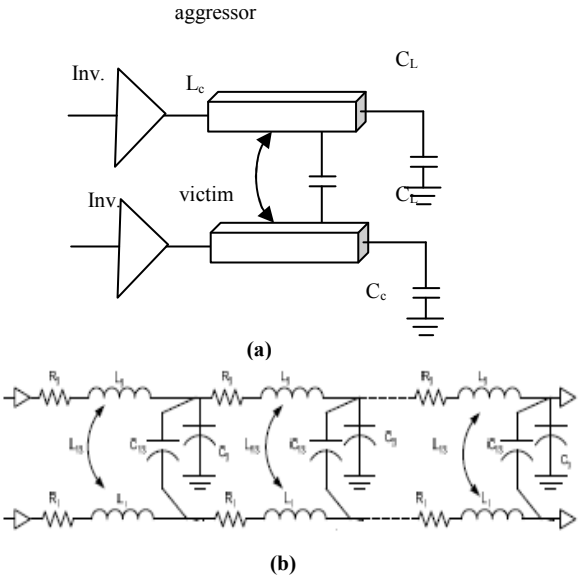

Fig. 1. Two line bus structure used for analyzing the effect of width variation

3. IMPACT OF WIDTH VARIATION ON TRANSITION TIME

Transition time is the time required by signal at the end of interconnects to vary from 10% to 90% of its final value (V_{dd}). For line widths at which the line inductance dominates the line resistance, the matching condition plays an important role in determining signal characteristics. For an inductive environment, the matching condition at the driver and the load ends affects both the Power and Speed characteristics. At small interconnect widths, the characteristic line Impedance Z_{lossy} is large as compared to the equivalent output Resistance R_{tr} of the transistor. Thus, the line is overdriven (the underdamped condition). Z_{lossy} decreases with increasing line width. The line remains underdamped until Z_{lossy} equals R_{tr}. A further increase in the line width under drives the line as Z_{lossy} becomes less than R_{tr}. Therefore, as the line width is increased, the line driving condition changes from overdriven to matched to underdriven. The transition time is minimum for the matched condition. A further increase in the width under drives the line. At these widths, the capacitance begins to dominate the line impedance and thus the transition time increases with increase in width. A 70nm technology CMOS inverter (W_n=5.25µm, W_p=13.125µm) driving a 5-mm-long interconnect line is chosen to demonstrate the signal behavior. Sixty distributed impedance elements are used to model the interconnect line. The input is a ramp signal with a 5 psec transition time. Simulation results for transition time are shown in Fig. 2 for line width varying from 0.1µm to 4µm at C_L of 100, 200, 400, 700 and 1000fF for similar switching pattern at both the inputs. Also we have extended our analysis for opposite switching pattern which is provided in Fig. 3 for line width varying from 0.1µm to 4µm at C_L of 100, 200, 400, 700 and 1000fF.

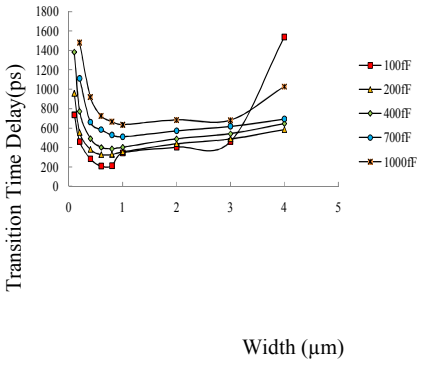

Fig. 2. Transition time delay for passive load of 100, 200, 400,700, and 1000fF capacitance with respect to Interconnect width (with similar switching)

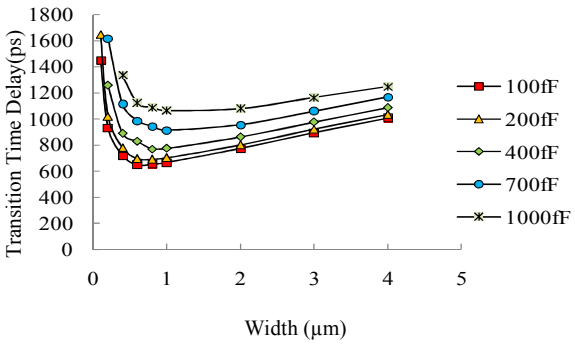

Fig. 3. Transition time delay for passive load of 100, 200, 400,700, and 1000fF capacitance with respect to Interconnect width (with opposite switching)

4. POWER DISSIPATION

Dynamic Power Dissipation (P_d) is given by the relation

$$P_d = fV_{dd}^2 C_{Lt} \quad (1)$$

where, f is the operating frequency, C_{Lt} is the total capacitance driven, and V_{dd} is the supply voltage. The total capacitance C_{Lt} comprises of distributed line capacitance C_t, and load capacitance C_L. The dynamic power dissipated in the distributed transmission line capacitance and load capacitance represents a large portion of the total transient power dissipated. Power dissipation continues to grow, as the width of interconnect is increased due to increased line capacitance. Simulation results in Fig. 4 confirms this theory for wide range of interconnect width at different values of C_L. Reduced transition time for matched condition does not affect overall power dissipation of the circuit.

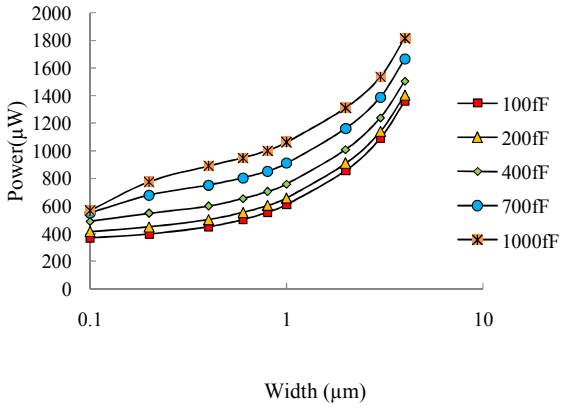

Fig. 4. Power Dissipation for passive load of 300, 400, 500 and 1000 fF with respect to Interconnect width (with similar switching)

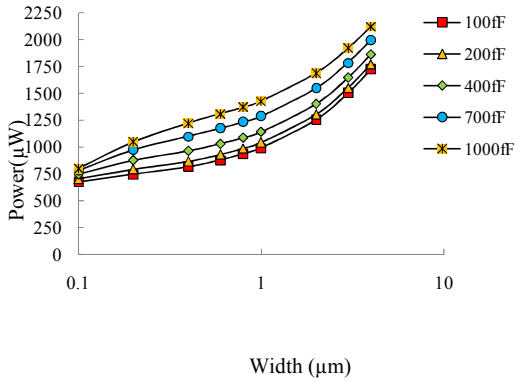

Fig. 5. Power Dissipation for passive load of 300, 400, 500 and 1000 fF with respect to Interconnect width (with opposite switching)

5. IMPACT OF SIGNAL SKEW ON CROSSTALK NOISE

Noises injected on to a victim line from multiple neighboring aggressors due to capacitive and inductive coupling have different implications depending on the modes of switching activities of neighboring lines with respect to the victim line. In this section, we investigate the impact of width variation on the cross-talk voltage caused by both capacitive and inductive coupling. For better comparison, we define overshoot voltage in terms of percentage overshoot as in Eq. (2). Here, V_{dd} and V_{out} are the supply voltage and output voltage (at the input of receiver connected at the end of the victim line) respectively. Again keeping signal slew time at 5ps, we vary the width of the interconnect line for different sets of passive load and measure maximum overshoot voltage at the receiver input for different switching patterns. The simulation results are shown graphically in Figure 6 and Figure 7.

$$\%Overshoot = \frac{V_{out} - V_{dd}}{V_{dd}} \quad (2)$$

For neighboring lines switching in same direction of victim line, maximum voltage overshoot increases slowly with the increase in width of interconnect line as can be observed in Fig. 6. However, Fig. 7 shows that maximum overshoot first rise significantly and then become constant afterwards in case of opposite switching of the victim line.

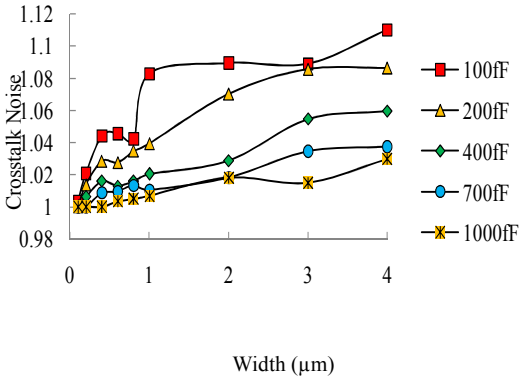

Fig. 6. Power Dissipation for passive load of 300, 400, 500 and 1000 fF with respect to Interconnect width (with similar switching)

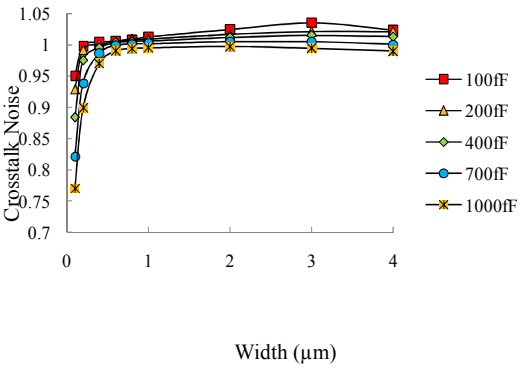

Fig. 7. Power Dissipation for passive load of 300, 400, 500 and 1000 fF with respect to Interconnect width (with similar switching)

In this circuit configuration (opposite switching), we observe large amount of spike voltage during the input transition of victim line with respect to aggressor lines. These spikes arise due to strong capacitive coupling behavior of oppositely switching lines. In contrast, almost no spike voltage is seen during similar switching (first case) because of the minimum capacitive coupling.

6. CONCLUSION

In this paper, we analyze the impacts of width variation on transition time delay, power dissipation and cross talk noise in *RLC* interconnects for different switching combinations based on simulation results. It is observed that transition time delay first decreases with width variation and then it is again start increasing with increase in width. Also we observe that power dissipation increases with the increase in width of the interconnect line in either of the switching condition. Also we observed that crosstalk noise increases with increase in the width of the interconnect line. Optimized width should be used for the global interconnect line for improved performance.

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