Optimum Body Biasing Technique in Domino Logic Gate Design for Low Power Applications

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ABSTRACT
Domino CMOS logic circuit family finds a wide variety of applications in microprocessors, digital signal processors, and dynamic memory due to their high speed and low device count. These dynamic circuits are often favored in high performance designs because of the speed advantage offered over static CMOS logic circuits. In this paper, AND gates with different body biasing are compared taking power consumption and delay as parameters. The designs are tested in 32nm technology. The domino AND gate design with least power consumption, delay and power delay product is proposed.

Index Terms: CMOS, Subthreshold regoin, Domino logic, Dynamic power, Substrate Biasing.

1. INTRODUCTION
The complexity of the devices is increasing with advancement of the technology. The increasing number of transistors and interconnect length is increasing the power consumed in high performance microprocessors. The power consumption has increased to levels that impose a fundamental limitation to increasing performance and functionality [1]-[2]. Domino logic circuit techniques are extensively applied in high performance microprocessors due to the superior speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits [3]. If the current trend in increasing power continues, high performance microprocessor will soon consume thousands of watts. The power density of a high performance microprocessor will exceed the power density levels encountered in typical rocket nozzles within the next decade [4]. Domino logic circuits, however, are highly sensitive to noise as compared to static gates. As on-chip noise becomes more severe with technology scaling and increasing operating frequencies, error free operation of domino logic circuits has become a major challenge [1]-[6].

The application of aggressive circuit design techniques which only focus on enhancing circuit speed without considering power is no longer an acceptable approach in most high complexity digital systems. Dynamic switching power, the dominant component of the total power consumed in current CMOS technologies, is quadratically reduced by lowering the supply voltage. Lowering the supply voltage, however, degrades circuit speed due to reduced transistor currents.

Threshold voltages are scaled to reduce the degradation in speed caused by supply voltage scaling while maintaining the dynamic power consumption within acceptable levels [1] – [4]. At reduced threshold voltages, however, sub-threshold leakage currents increase exponentially. Energy efficient circuit techniques aimed at lowering leakage currents are, therefore, highly desirable. Domino logic circuit techniques are extensively applied in high performance microprocessors due to the superior speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits. However, deep sub micrometer (DSM) domino logic circuits utilizing low power supply and threshold voltages have decreased noise margins. As on-chip noise becomes more severe with technology scaling and increasing operating frequencies, error free operation of domino logic circuits has become a major challenge.

The latest advances in mobile battery-powered devices such as the Personal Digital Assistants (PDA) and mobile phones have set new goals in digital VLSI design. The mobile devices require high speed and low power consumption and thus power-delay product plays important role in the designing of VLSI circuits. The operation of low frequency circuits in the sub-threshold region stands out as the optimal method of power reduction [7]. Sub-threshold current of a MOSFET transistor occurs when the gate-to-source voltage (V_{GS}) of a transistor is lower than its threshold voltage (V_{TH}). When V_{GS} is larger than V_{TH}, majority carriers are repelled from the gate area of the transistor and a minority carrier channel is created. This is known as *strong-inversion*, as more minority carriers are present in the channel than majority carriers. When V_{GS} is lower than V_{TH}, there are less minority carriers in the channel, but their presence comprises a current and the state is known as *weak-inversion*. In standard CMOS design, this current is a sub-threshold parasitic leakage, but if the supply voltage (V_{DD}) is lowered below V_{TH}, the circuit can be operated using the sub-threshold current with ultra-low power consumption. Over the past decade, considerable research is devoted to the development of energy-efficient VLSI circuit and systems for portable systems [8] – [10].

Comparison of body bias methods using delay, power and PDP indicates that separately biasing the pre-charge and evaluation tree transistor bodies permits high-speed and energy-efficient ultra-low voltage domino circuits to be realized. Minimum energy in the subthreshold region then depends not only on supply voltage but also on the substrate bias voltage [11].

In this paper domino AND gates with different substrate biasing techniques are compared. Power consumption, delay are used as parameters at different frequencies, supply voltages and temperatures in subthreshold region. The rest of the paper is organized as follows: In Section II various Circuit techniques in domino logic circuits for power reduction and

delay reduction are proposed. In Section III simulation and implementation results are presented. Finally, conclusions are presented in Section V.

2. CIRCUIT TECHNIQUES

Dynamic domino logic circuits are widely used in modern VLSI circuits. These dynamic circuits are often favored in high performance designs because of the speed advantage offered over static CMOS logic. The main drawbacks of dynamic logic are a lack of design automation, a decreased tolerance to noise and increased power Consumption. This work discusses several domino circuits design techniques to reduce the power Consumption of domino logic while simultaneously improving noise immunity. Domino logic gates are frequently employed in high performance circuits for high speed and area efficiency. As supply voltage is reduced, delay increases, unless threshold voltage V_T is also decreased. Substrate biasing provides an effective circuit-level technique for varying threshold voltage, as can be seen in (1) below.

$$V_T = V_{T0} + \gamma(\sqrt{|V_{SB} - 2\emptyset_F|} - \sqrt{|2\emptyset_F|})$$

Here V_{TO} is the zero-bias threshold voltage, γ the body-effect coefficient, V_{SB} the source-to-bulk voltage, Φ_F the quasi-Fermi potential.
For different biasing schemes, the output inverter is zero body biased figure 1.

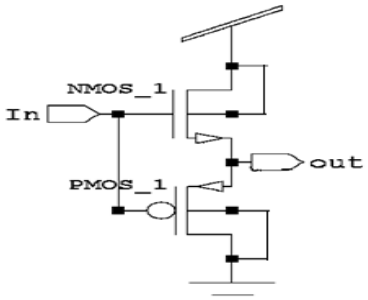

Fig. 1 Conventional body-biasing inverter

Different biasing schemes are shown below:-
In order to enhance the performance of the circuit, various body biasing techniques are used. The substrate of the MOS transistors is connected in six different ways. Six body biasing schemes for the evaluation networks are shown in figure 2.
1. The substrate of NMOS is connected to clock and the substrate of PMOS is connected to supply voltage V_{DD} (SB1) (fig. 2(a)).
2. The substrate of NMOS and PMOS is connected to clock (SB2) (fig. 2(b)).
3. The substrate of NMOS is connected to supply voltage V_{DD} and the substrate of PMOS is connected to clock (SB3) (fig. 2(c)).
4. The substrate of NMOS is connected to supply voltage V_{DD} and the substrate of PMOS is connected to Ground (SB4) (fig. 2(d)).
5. The substrate of NMOS and PMOS both connected to supply voltage V_{DD} (SB5) (fig. 2(e)).
6. The substrate of NMOS is connected to its source terminal and the substrate of PMOS is connected to clock (SB6) (fig. 2(f)).

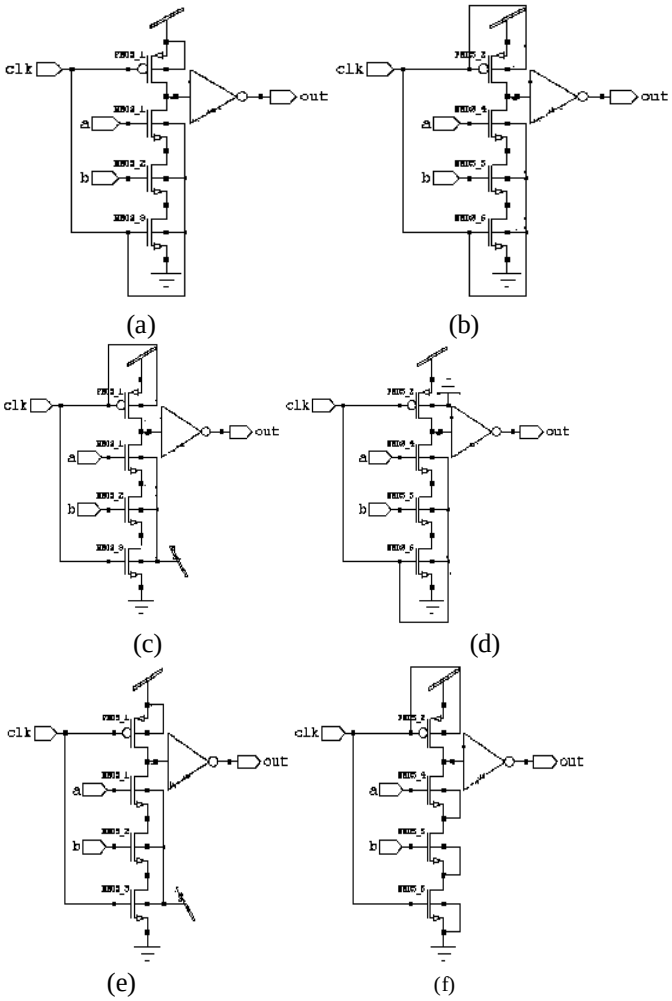

Fig. 2.(a) SB1, (b)SB2, (c)SB3, (d)SB4, (e)SB5, (f)SB6

3. SIMULATION AND IMPLEMENTATION RESULTS

The design is simulated using tanner-EDA tool in 32nm, technology and Power, Delay and Power Delay Product (PDP) are taken as parameters. Designs are tested in different biasing conditions when different voltage, operating frequency, and temperature are taken.

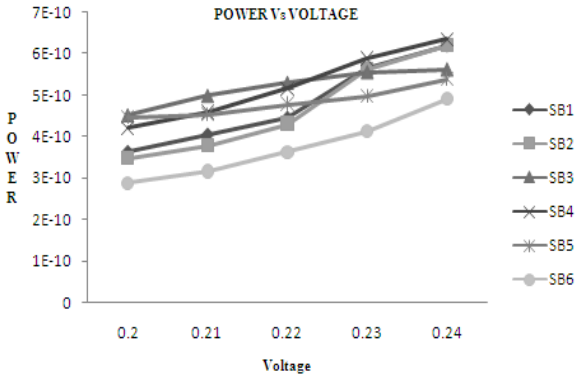

Figure.3 Power Dissipation at various voltages in 32 nm technology

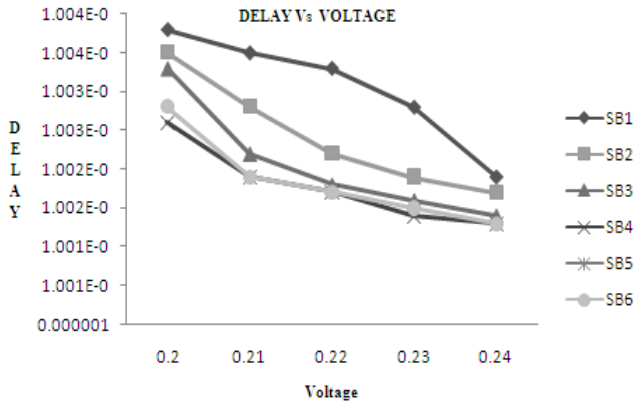

Figure.4 Delay at various voltages in 32 nm technology

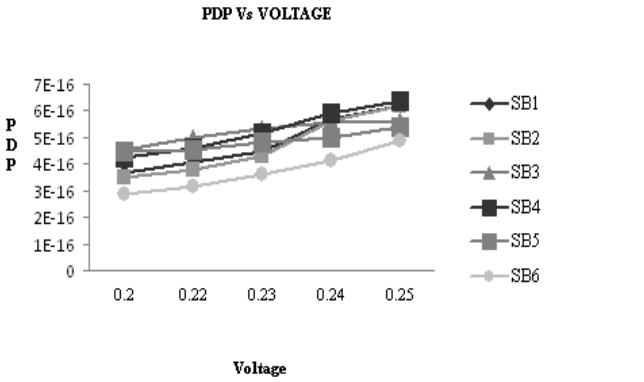

Figure.5 Power-Delay Product at various voltages in 32 nm technology

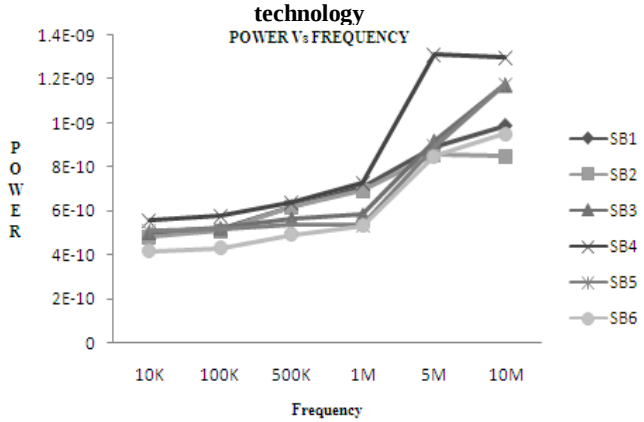

Figure.6 Power Dissipation Vs frequency in 32 nm technology

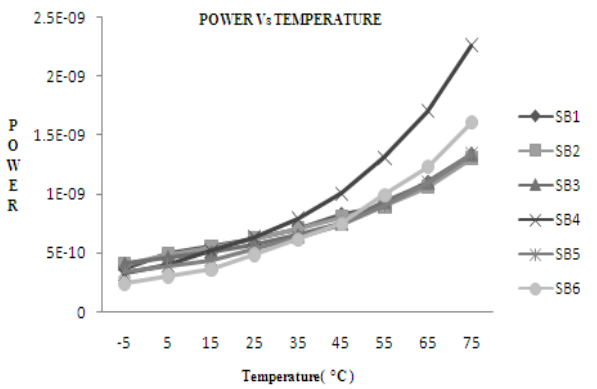

Figure.7 Power Dissipation Vs temperature in 32 nm technology

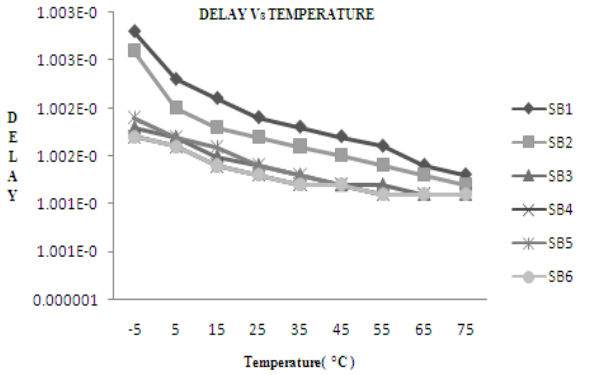

Figure.8 Delay Vs temperature in 32 nm technology

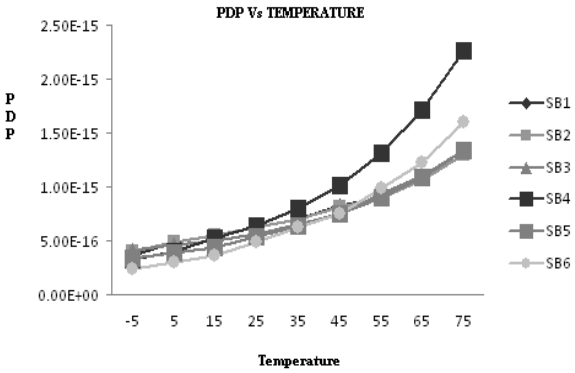

Figure.9 Power-Delay Product Vs temperature in 32 nm technology

Supply voltage, frequency and temperature are taken as parameters. The standard temperature value of 25°C, input signal frequency of 500 kHz, and supply voltage of 0.22 V in 32 nm technology is used. Power consumption, delay are measured keeping one parameter variable with two other parameters constant, e.g. , power consumption is calculated at various frequencies keeping the supply voltage at 0.24 V and temperature at 25°C.

The power dissipation depends upon the supply voltage. As the supply voltage increases, the power consumption also increases. It is clear from the figure 3, that the supply voltage is varied from 0.20 – 0.24 V such that the circuit operates in subthreshold region. The power consumption is measured in various body biased designs and found that the SB6 design

shows the least power consumption. Delay also depends upon the supply voltage. The SB6 biasing and SB4 biasing of the gate shows the comparable delay (fig. 4) but overall power delay product of the SB6 biased gate is least among all the biasing schemes (fig. 5).

Power consumption also depends upon the applied signal frequency. From the fig. 6, the power consumption at various frequencies in SB6 biasing is least in low to medium frequency region up to 5 MHz but more than SB2 biasing above 5 MHz frequency.

Power dissipation in the chip increases the temperature, which in turn degrades the performance of the chip. Thus the performance of the design to be tested at various temperatures is also an important simulation step. The power consumption by the SB6 design is less up to 45^{o}C (fig. 7). Delay introduced by the SB6 design is always less at various temperatures among all the designs (fig. 8). Hence the power delay product is least up to 45^{o}C among all the designs (fig. 9).

4. CONCLUSION

Domino logic circuit techniques are extensively applied in high-performance microprocessors due to the superior speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits. The domino logic based gate designs using various biasing schemes are presented and simulation results reveal that the AND gate design, in which the substrate of NMOS transistors are connected to its source terminal and the substrate of PMOS transistor is connected to clock shows the best power delay product among the other five designs presented. The design proposed is optimum and better applicable for portable applications operating at medium frequency range.

5. REFERENCES:

[1] Alvandpour, P. Larsson-Edefors, and C. Svensson, "A Leakage Tolerant Multi-Phase Keeper for Wide Domino Circuits", Proceedings of the IEEE International Conference on Electronics, Circuits and Systems, pp. 209-212, September 1999.

[2] S. Borkar, "Obeying moore's law beyond 0.18 micron", in Proc. IEEE Int. ASIC/SOC Conf., Sept. 2000, pp. 26–31.

[3] V. Kursun and E. G. Friedman, "Low Swing Dual Threshold Voltage Domino Logic", Proceedings of the ACM/SIGDA Great Lakes Symposium on VLSI, April 2002.

[4] M. T. Bohr, "Nanotechnology goals and Challenges for electronic applications", IEEE Trans.Nanotechnol., vol. 1, pp. 56–62, Mar. 2002.

[5] R. Ronen et al., "Coming challenges in microarchitecture and architecture", Proc. IEEE, vol. 89, pp. 325–339, Mar. 2001.

[6] M. W. Allam, M. H. Anis, and M. I. Elmasry, "High-Speed Dynamic Logic Styles for Scaled-Down CMOS and MTCMOS Technologies", Proceedings of the IEEE International Symposium on Low Power Electronics and Design, pp. 155- 160, July 2000.

[7] Wang, B. H. Calhoun and A. Chandrakasan, "Sub-threshold design for ultra low-power systems". Springer publishers, 2005.

[8] Narendra S., Tschanz J., Hofsheier J., Bloechel B., Vangal, S., Hoskote Y., Tang S., Somasekhar D., Keshavarzi A., Erraguntla V., Dermer G., Borkar N., Borkar S., De V., "Ultra-low voltage circuits and processor in 180nm to 90nm technologies with a swapped-body biasing technique", International Solid-State Circuits Conference, ISSCC, vol., no., pp. 156-518 Vol.1, 15-19 Feb. 2004.

[9] T. Sharma, K. G. Sharma, B. P. Singh, N. Arora, "Efficient Interconnect Design with Novel Repeater Insertion for Low Power Applications," World Scientific and Engineering Academy and Society (WSEAS) Transactions on Circuits and Systems, Vol. 9, N0.3, pp. 153-162, March 2010.

[10] K.G.Sharma, Tripti Sharma, Prof.B.P.Singh, Manisha Sharma and Neha Arora, "Optimized Design of SET D Flip-Flop for Portable Applications", International Journal of Recent Trends in Engineering and Technology, vol. 4, no. 3, Nov. 2010.

[11] Fu and P. Ampadu, "Techniques for Robust Energy Efficient Subthreshold Domino CMOS Circuits", ISCAS, pp. 1247-50, 2006.