BER Analysis for Different Number of Inserted Flip-Flop and Latches

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ABSTRACT
In this paper a detailed analysis for how the number of flip-flops and latches inserted are effecting BER and repeater size with wire pipelining is performed. Since number of flip-flops, latches and repeater sizes cannot be scaled down beyond a certain limit due to the solidity requirement, which is determined by maximum allowable bit error rate.

Keywords:
Bit Error rate (BER), Timing Margin (TM), D-flip flop, Wire Pipelining.

1. INTRODUCTION

Building a sequential machine requires memory elements which read a value, save it for some time and then write that stored value somewhere else even if the element's input value has subsequently changed. A Boolean logic gate can compute values, but its output value will change shortly after its input changes. Each alternative circuit used as a memory element has its own advantages and disadvantages. A generic memory element has as internal memory and some circuitry to control access to the internal memory. Access to the internal memory is controlled by the *clock* input. The memory element reads its *data* input value when instructed by the *clock* and stores that value in its memory. For interconnect delays beyond the capabilities of repeater insertion, several alternative approaches can be adopted to meet certain timing constraints [1][3][5][6]. But all these approaches have their own drawbacks. Insertion of sequential elements in interconnects lines – a concept that is become known as *interconnect pipelining* − is one feasible solution for modern nanometer technologies. The idea is to divide a wire, whose delay is longer than one clock cycle, into several segments by inserting sequential elements to store signal values that require multiple clock cycles to travel through a particular global wire.

2. BER ANALYSIS FOR FLIP-FLOP BASED WIRE PIPELINING

The Solidity of wire pipelining scheme is strongly dependent on many factors including repeater sizing, process, parameter variations and clock signal variation. Some of the factors cannot be controlled, such as the clock signal variation and the wire delay uncertainty. The BER can be decreased by changing the number of flip-flops inserted and the repeater sizes [2][4]. The impact of these factors on the BER of flip-flop based wire pipelining using statistical timing analysis to calculate the BER of a flip-flop inserted global wire is given.

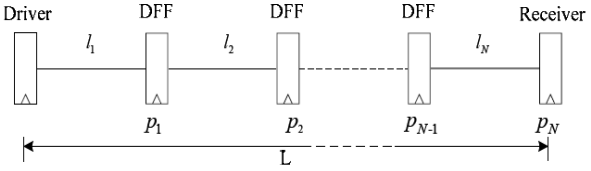

Fig. 1. Dff pipelined interconnect stage

A. *BER calculation for FF based wire pipelining*

For an interconnect wire of Length *L*, whose driver and the receiver are all registers as shown in Figure 1, if the wire length and the target clock frequency are known, the analytical models to determine the minimum number, central positions and width of feasible regions of inserted flip-flops for wire pipelining can be expressed by equation (1), (2) and (3) respectively, which are proposed by [8], assumed that the clock signal is ideal and stable. Here, *LF*, *LL*, *LM* stand for the maximum wire length of the first wire segment, last wire segment and the middle segments after optimal number of repeater insertion. *Lmax,0* is the maximum wire length without interconnect pipelining and *n* is the number of flip-flop inserted. The width of the feasible region for each (1), (2) and (3) respectively, which are proposed by [8], assumed that the clock signal is ideal and stable. Here, *LF*, *LL*, *LM* stand for the maximum wire length of the first wire segment, last wire segment and the middle segments after optimal number of repeater insertion.

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$$N_f = \begin{cases} 0 & if \;\; L \le L_{\max,o} \\ 1 & if \;\; L_{\max} < L \le L_l + L_f \\ \left[\left(L - L_f - L_l\right)/L_m\right] + 1 & otherwise \end{cases} \qquad (1)$$

$$P_I = L_F + (i-1)\,L_M - (i-1/2)\,W_{FR} \qquad (2)$$

$$W_{FR} = (L + L_l + (n-1)L_M - L)/n \qquad (3)$$

Now, we perform our calculation based on 0.13μ*m* technology parameters. Here the wire length is changed from 5*mm* to 25*mm*, and the clock frequency is fixed at 2.0GHz. The propagation delay of the inserted flip-flop is .79ns and the setup time is 112ps. Other parameters are shown in table 1. Here *c* is wire capacitance per unit length, *r* is wire resistance per unit length, *R* is wire resistance, *C* is

flip-flop/latch input capacitance (input capacitance of receiver).

TABLE I
PARAMETER VALUES USED IN THE ANALYSIS

Tech. Node(nm)	**130**
WIDTH	335
THICKNESS	670
R Ω-μm	0.098
Ca (fF/mm)	207
Cb(fF/) μm	0.0570
Cc(fF/) μm	0.226

First, through using the equations given by [8], we can calculate the maximum wire length *LL*, *LF*, *LM* and *Lmax,0*. For different wire length, the number and positions of inserted flip-flops are calculated using (1) and (2). Then, we calculate the BER at the presence of clock and parameter variation. We assume that all the parameters are following the normal distribution $N(\mu, \delta)$, and the standard deviation of clock jitter, wire delay, propagation delay and the setup-time of the inserted flip-flops are 3% of their nominal values. The Bit Error Rate (BER) for the wire pipelining scheme can be calculated by (4) [3].

$$BER = 1 - \prod_{i=1}^{N+1} q_i \qquad (4)$$

Where, *qi* is the possibility that data can be transferred correctly from *i*-th stage to the next stage and can be calculated using equation (6) [3].

$$q = \frac{1}{2} + erf\left(-\frac{\mu_\delta}{\sigma_\delta}\right) \qquad (5)$$

$$erf(x) = \frac{1}{\sqrt{2\pi}} \int_0^x \exp\left(-\frac{t^2}{2}\right) dt \qquad (6)$$

and,

$$\mu_\delta = T_{prop} + T_{setup} - T_{clk} \qquad (7)$$

$$\sigma_\delta^{\,2} = \sigma_{Tprop}^{\,2} + \sigma_{itwire}^{\,2} + \sigma_{Tsetup}^{\,2} + \sigma_{Tclk}^{\,2} \qquad (8)$$

Tprop and *Tsetup* is the propagation delay and the setup time of the inserted flip-flops, *Twire* is the wire delay for that wire segment and *Tclk* is the clock period. σ stands for the standard deviation of corresponding parameter. The calculated results are shown by Figure 2. It can be observed that the BER is unusually high if the wires length is in certain ranges, which clearly indicates the devastating impacts of the clock and parameter variations on wire pipelining.

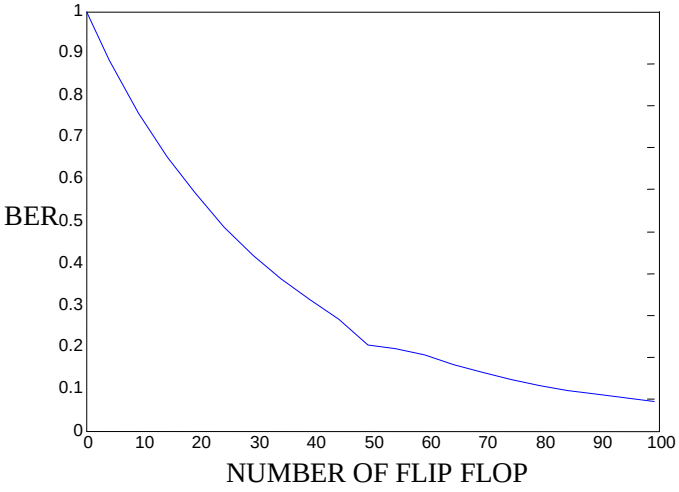

Fig.2. BER V/S Number of Flip-Flops

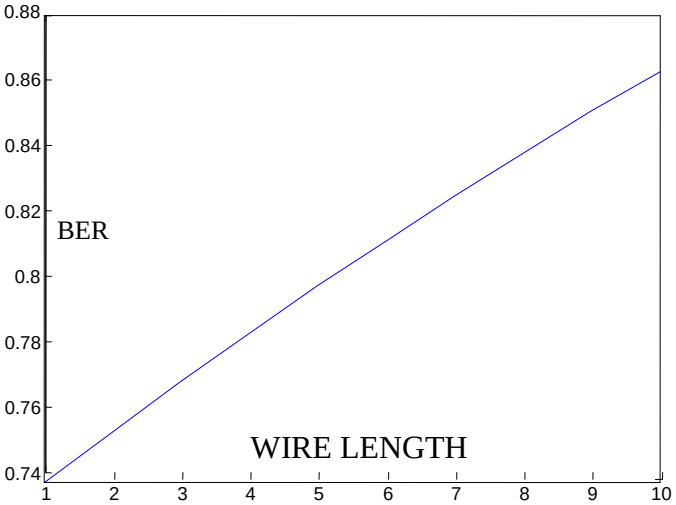

Fig.3. BER V/S Wire Length

Demonstrate the reason for this phenomenon, we introduce a parameter – "*timing margin*" for wire pipelining scheme. This parameter determines how much extra time can be safely consumed by clock or parameter variations. So, this parameter is just an indication of the solidity a wire pipelining scheme. The timing margin *TM* for a flip-flop based wire pipelining scheme can be calculated using the following equation:

$$T_M = (N+1)(T_{clk} - T_{prop} - T_{setup}) - D_{t\,wire} \qquad (9)$$

Where, $D_{t\,wire}$ is the total wire delay. Figure 2 shows the average timing margin (*TM* /*N*) of the wire pipelining scheme using the minimum number of flip-flops. From the figure, we can see that the average timing margin changes periodically and the trend of BER is the same as the trend of average timing margin. At certain wire length, the timing margin of the wire pipelining scheme is zero and BER will reach the maximum. Therefore, the reason for the high BER at certain wire length is that the timing margin is too low. From the above observation, we can see that the way to lower the BER for flip-flop based wire pipelining is just to increase the timing

margin. And, according to equation (9), increasing the number of flip-flop inserted will increase the timing margin. So, we can lower the BER of a wire pipelining simply through increasing the number of inserted flip-flops. Furthermore, the location of each inserted flip-flop will also affect the BER of whole wire pipelining scheme. So, before we analyse the relationship between the BER and the number of flip-flops inserted, we will take a look at the relationship between the position of each inserted flip-flop and the BER. From the above observation, we can easily draw a conclusion: in order to get the lowest BER, the best position for each inserted flip-flop is:

$$pi=iL/(N+1),(i=1,2,....,N) \qquad (10)$$

Now, we will take a look at the relationship between BER and the number of flip-flops inserted. Figure (1) gives out the BER for different number of inserted flip-flops for a wire of 20*mm* in length. Each flip-flop is located at their best position according to (10). From the analysis of the trend of this function we can find that when the number of flip-flops inserted is small, the BER will decrease rapidly as *N* increases. After that, the decrease rate will slow down and gradually reaches the lowest BER. Then, the BER will slowly increase. We can also see that the lowest BER will be reached if we insert nearly 100 flip-flops along this wire, which is impossible in practice. If we want to implement a flip-flop based wire pipelining scheme at a given BER requirement *TE*, the given BER requirement must be larger than the lowest BER. Only under that condition, we can find the solution of the following inequality:

$$BER = 1 - \prod_{i=1}^{N+1} q_i \le T_E \qquad (11)$$

Now, the problem becomes finding the minimum number of inserted flip-flops so that it can satisfy the given BER requirement.

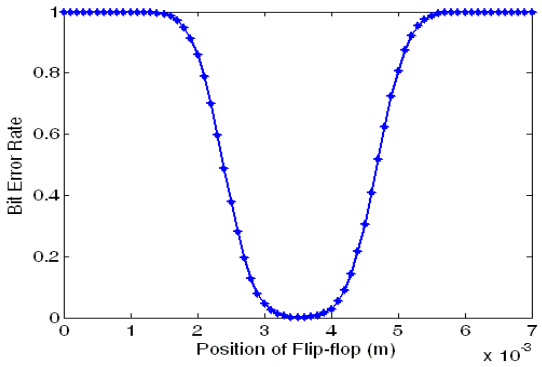

Fig 4. BER V/S Position of Inserted Flip-Flops

3. BER ANALYSIS FOR LATCH BASED WIRE PIPELINING

The analysis method of latch based wire pipelining is different from flip-flop based wire pipelining. A detailed comparison of flip-flop and latch based wire pipelining is given by [7] and [10]. To analyse the BER of latch based wire pipelining, we used the algorithm proposed by [9] to implement the wire pipelining scheme. Then we use the method given by [3] to acquire the BER of this wire pipelining scheme. Here, we also use 0.13μ*m* technology data, the propagation delay of the latch is 94ps, and the setup time is 116ps. The clock frequency is 2GHz and the wire-length is varied from 1cm to 2.5cm. In the implementation, all the latches are placed at the centre of its feasible region. The clock and other parameter variations are the same as those that we have used for flip-flop based wire pipelining.

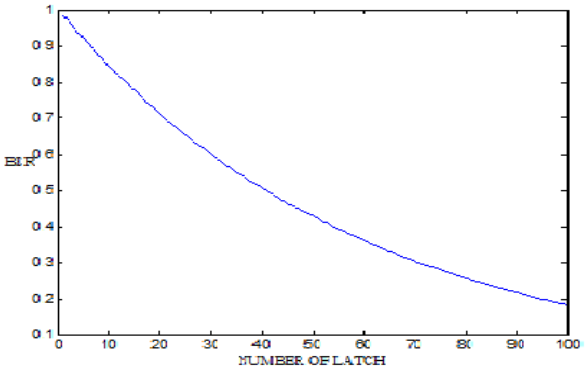

Fig.5. BER V/S Number Of Latches

Figure (4) gives out the BER for latch based wire pipelining for different wire lengths. Compare this figure (1) with Figure (4), we can see that the BER for latch based wire pipelining is lower than that of flip-flop based counterpart in most cases.

But, we can also see that for some wire lengths, the BER is also unusually high. The reason for the high BER can also be explained by the average timing margin of the wire pipelining. The definition of the timing margin of latch based wire pipelining is given by equation (12) [10].

$$T_M = (N+1)T_{clk} - D_{t\,wire} - N_{T_{data}} - T_{prop} - T_{setup} \qquad (12)$$

From the figure (6), we can see that both average timing margin and the remaining average timing margin are zero at certain wire lengths, and the BER will reach the maximum at those wire lengths. Now, the problem is to find a method to increase the average timing margin, which can be done through increasing the number of latches inserted. Because in a latch based wire pipelining, a latch can be designed as a reference latch or non-reference latch, the function of BER for latch based wire pipelining is not a continuous function. Therefore, it is hard or even impossible to derive an expression of the BER for latch based wire pipelining. But, if we are given the BER requirement, we can still find ways to solve this problem. The same as flip-flop based wire pipelining, the position of each inserted latch will also affect the whole wire pipelining scheme.

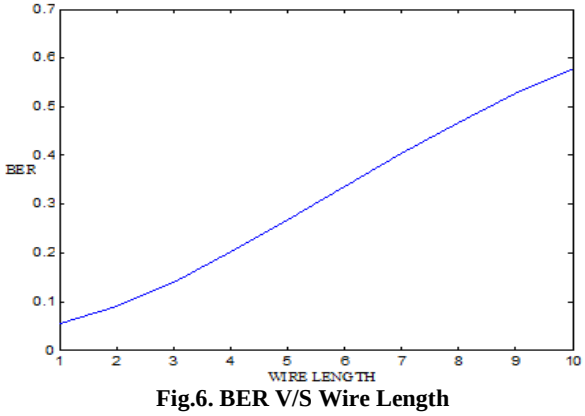

Fig.6. BER V/S Wire Length

So, we also take a look at the relationship between the position of each inserted latch and the BER. Figure (7) gives out the calculation result, the best position of the inserted latch is p1=6.6mm. When we consider a wire of 10mm in length and two latches are needed. From these observations, we know that it is hard to get an expression for the best position of each inserted latch. So, a possible method to find the best position of each inserted latch is just through trying.

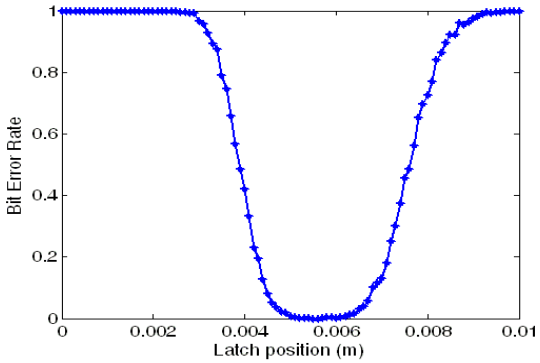

Fig.7. BER V/S Position of Inserted Latch

4. CONCLUSION

In this paper, we performed an in depth analysis of the BER for flip-flop and latch based wire pipelining, and demonstrated the higher BER of using the minimum number of sequential elements. And observe that the minimum number of inserted latches always smaller than the optimal number of latches from BER point of view. Then we analysed the reason for the phenomenon and proposed methods to lower the BER. Finally, a comparison of the two kinds of wire pipelining approaches from the BER point of view is given. Our ongoing attempt is to take other circuit level issues into consideration and analyses their impacts on the wire pipelining schemes.

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