

# **Power Reduction Technique in LFSR using Modified Control Logic for VLSI Circuit**

**Praveen J**

Alva's Institute of Engineering and Technology  
Dept of Electronics and Communication Engg  
Moodbidri, South Canara - 57425

**M N Shanmukhaswamy**

JCE Institute of Technology  
Dept of Electronics and Communication Engg  
Mysore -570006

## **ABSTRACT**

A linear feedback shift register (LFSR) is proposed technique which targets to reduce the power consumption within BIST itself. It reduces the power consumption during testing of a Circuit Under Test (CUT) at two stages. At first stage, Control Logic (CL) makes the clocks of the switching units of the register inactive for a time period when output from them is going to be same as previous one and thus reducing unnecessary switching of the flip-flops. And at second stage, the LFSR reorders the test vectors by interchanging the bit with its next and closest neighbor bit. It keeps fault coverage capacity of the vectors unchanged but reduces the Total Hamming Distance (THD) so that there is reduction in power while shifting operation.

## **General Terms**

Fault coverage, LFSR technique, switching Activity, Humming Distance

## **Keywords**

Built-In Self-Test, VLSI Testing, low-power test vector pattern generation.

## **1. INTRODUCTION**

Dissipation is a challenging problem in today's System-on-Chips (SoC) Design and Test. In general, power dissipation of a system in test mode is more than that in normal mode. This is because a significant correlation exists between the consecutive tests vectors applied during the circuit's normal mode of operation, whereas this may not be necessarily true for applied test vectors in test mode of operation. Low correlation between test vectors increases switching activity and eventually leads to power dissipation in the circuit. Built-In Self Test (BIST) is the most suitable approach for low power testing as it provides a larger scope for low power techniques to be used. BIST uses an LFSR as test pattern generator (TPG). The LFSR generates all possible test vectors with the proper use of tap sequence. Furthermore the pseudorandom behavior of the LFSR reduces the correlation among test vectors which means that it can achieve high fault coverage in a relatively short run of test vectors. However, this lack of correlation among test vectors substantially increases the Hamming distance among the vectors which leads to increased switching activity in the CUT. This often causes more power dissipation in test mode of operation. It is therefore required to find an optimum linear feedback shift register which, in-itself is power efficient and the test vectors generated as well, are power efficient i.e., they cause least switching activity when scanned in into a scan chain of CUT, without compromising the fault coverage.

## **2. PROLOGUE**

Many low power testing techniques have been proposed. However, there are two broad categories namely External Testing and BIST.

The External Testing techniques include the methodologies based on Automatic Test Pattern Generator (ATPG), Vector Reordering and architecture whereas the BIST include techniques based on LFSR, Test Scheduling, Circuit Partitioning and Reseeding.

However, the vector ordering can be used in BIST environment as well. In ordering techniques, the THD i.e. the sum of the hamming distances is minimized by modifying the order in which test vectors of a given test sequence are shifted into the CUT. The Travelling Salesman Algorithm (TSA) has been quite useful for ordering the test vectors. The test vector ordering has been useful in minimizing the hamming distance among test vectors and thereby reducing in average and peak power.

Reordering of test vectors does not affect the fault coverage as overall the same set of test vectors are applied, just their order is modified. The paper discussed about two methods used for reordering of test vectors in order to reduce the dynamic power dissipation during testing of combinational circuits. Two search methods, 2-opt heuristic and a genetic algorithm based approach has applied and results obtained for combinational circuits. These techniques can be applied during external testing or deterministic BIST as well.

## **3. MOTIVATION**

Motivation for the proposed work arises from two observations. First is that the literature available focuses upon ordering the test vectors after obtaining the test vector sequences from the LFSR. And other is LFSR can itself be power efficient if modified for the purpose.

The aim of the work is to design an LFSR which in itself is power efficient and the test vectors generated from it are also power efficient.

## **4. PROPOSED METHODOLOGY**

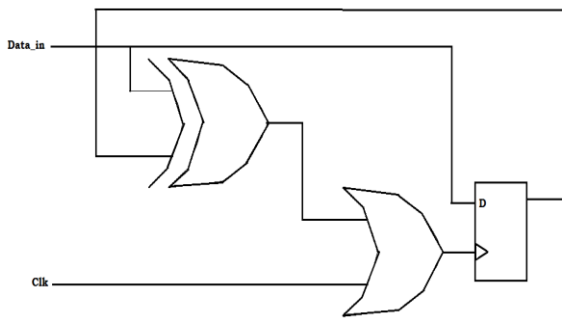
In the proposed approach, an LFSR has been designed such that it reorders the test vectors to minimize the switching activity and consumes little power as compared to conventional LFSR. The switching units (flip-flops) of the LFSR toggle unnecessarily in the process of generating  $2^n$  sequence when same bits are repeated for a particular set of test sequences. Therefore the non performing flip-flops are disabled for a particular time period.

The flip-flops are disabled by asserting the clock signal to state '0'. The behavior of the switching unit is projected in the Table 1

**Table 1. Truth Table for the modified clock**

Data_in	Data_out	Clock	Modified Clock
1	0	1	1
0	1	1	1
1	1	1	0
0	0	1	0

The truth table logic can be realized by the use of an XOR and XNOR gate as shown in the fig.1



**Fig 1: Switching unit of LFSR with Modified Clock**

The CL logic shown in figure 1 can be used with last flip-flop of LFSR cell without modifying its tap sequence and thus without changing its behavior. Thus the clock signal is modified in order to reduce power consumption. Let the hamming distance test vector  $V_i$  and  $V_{i+1}$  be  $D(V_i, V_{i+1})$  which is the total number of changes between the vectors  $V_i$  and  $V_{i+1}$ . Then the Total Hamming Distance (THD) can be calculated from the Equation (1)

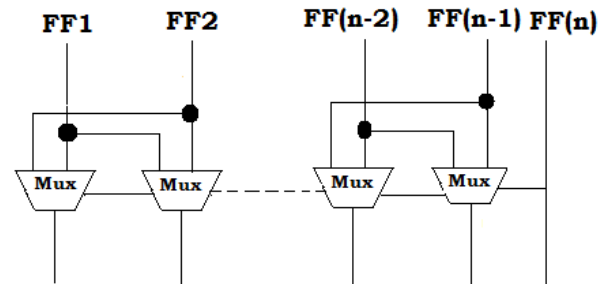
$$THD = \sum_{i=1}^{i=n+1} D(V_i, V_{i+1})$$

In the figure 2, a case of odd  $n$  is considered. When  $n$  is even the interchanging is performed up to third and fourth last FF outputs. Embedding the Bit Interchanging Module with the modified clock LFSR makes the design more power efficient as shown in Figure 3.

The THD is the measure of changes occurring among the test vectors. These changes determine the amount of switching activity in a CUT. The THD can be minimized if test vectors are shifted in a proper order. The LFSR with control logic is used along with a reordering algorithm based on bit interchanging method in. In an  $n$ -bit LFSR with bits 1, 2, 3, 4... $q$ ,  $q+1$ ,  $n$ , if the bit  $n$  (the selection bit) has a value '0' (or '1') the interchanging is performed between bit 1 & bit 2, between bit 3 & bit 4 and so on. If bit  $n$  has a value of 1 (or 0) then no interchanging is performed. The process ultimately generates a new order of test vectors. Let us illustrate the point with an example. We have a set of test vectors generated from a maximal length 3-bit LFSR. Applying the bit interchanging methodology a new order of the same test vectors is obtained. The resultant reduction in the hamming distance is depicted in the table below

**Table 2. Total Hamming Distance Reduction for 3-Bit LFSR**

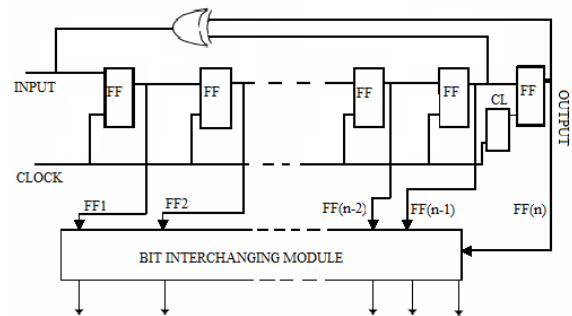
Test Vector	Test Vector from Conventional LFSR	Reordered Test Vector
V1	011	101
V2	001	001
V3	100	100
V4	010	010
V5	101	011
V6	110	110
V7	111	111
THD	10	9
New order of test vector		
V5 - V2 - V3 - V4 - V1 - V6 - V7		



**Fig 2: Architecture of bit interchanging module**

## 5. PROPOSED ARCHITECTURE

Based on the suggested bit interchanging methodology, the modified LFSR can be designed using the conventional LFSR and a group of two-input multiplexers where bit  $n$  is considered as the selection line of the multiplexers. The architecture for interchanging the bits as per the proposed methodology is presented in figure 2.



**Fig 3: Proposed general Modified TPG Architecture**

**Table 3. Experimental results for different test generation methods**

Circuits	LFSR			LFSR+CL			LP-TPG		
	LP(nw)	DP(nw)	TP(nw)	LP(nw)	DP(nw)	TP(nw)	LP(nw)	DP(nw)	TP(nw)
<b>Full adder</b>	33.57	84839.83	84873.40	34.98	81996.29	82031.27	42.88	80525.82	80525.69
<b>Full Subtractor</b>	30.61	80831.25	80861.87	32.01	80645.20	80677.22	39.90	77485.33	77525.24
<b>Binary to Gray</b>	30.11	23593.44	23593.48	31.17	1586.90	71618.15	33.58	75523.65	75557.23
<b>Gray to binary</b>	29.75	90634.91	90664.67	33.60	76898.88	76932.491	33.60	72830.44	72861.62

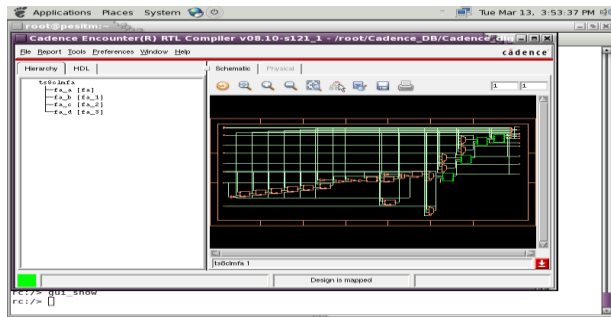
## 6. EXPERIMENTAL RESULTS

### Power Analysis and Simulation Setup

The results of the proposed method-1 shows that initially by adding only one CL, we can see that Total power reduced by 15.14 % to compare to conventional LFSR for Gray to Binary Bench Mark circuit, if along with this method Bit Interchange circuit is added than 19.63 % of Total power is reduced.

## 7. SIMULATION RESULTS

The overview of LP-TPG circuit output achieved from obtained from one of the power tool called cadence.



## 8. CONCLUSION

This paper presented a new low-power LFSR to reduce the average and peak power of a circuit during the test mode. The techniques available so far have focused upon reducing the switching activity from the test patterns generated from the generator. Embedding the switching activity minimizing techniques with a power efficient test pattern generators will be a good step ahead. Therefore a modification is proposed in the conventional LFSR by embedding it with control logic module and bit interchanging module. This culminates into a novel architecture of the test pattern generator (TPG).

The modified TPG architecture is capable of not only disabling the switching units for a particular time frame but also reorders the test vectors so as to reduce the transition activity. The benefit of the proposed TPG is that it can be used with any other low power technique to have further

reduction in power. The proposition is an attempt to invoke research on the test pattern generator itself. The techniques available so far have focused upon reducing the switching activity from the test patterns generated from the generator. Embedding the switching activity minimizing techniques with a power efficient test pattern generators will be a good step ahead. Therefore a modification is proposed in the conventional LFSR by embedding it with control logic module and bit interchanging module. This culminates into a novel architecture of the test pattern generator (TPG).

## 9. FUTURE WORK

Power dissipation in BIST can also be test pattern reordering with the purpose of reducing the amount of power dissipated during circuit testing. By reordering test patterns one is able to find test sequences for which power dissipation is minimized.

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## **AUTHOR'S PROFILE**

**Dr. M. N. Shanmukha Swamy** completed his B.E. degree in Electronics and Communication Mysore University in the year 1978, M.Tech in Industrial Electronics from the same university in the year 1987 and obtained his Ph.D in the field of Composite materials from Indian Institute of Science, Bangalore in 1997. He is presently working as Professor in the Department of Electronics and communication, Sri. Jayachamarajendra college of Engineering, Mysore, Karnataka, India. He is guiding several research scholars and has published many books & papers both in National & International conferences & journals. His research area includes Wireless Sensor Networks, Biometrics, VLSI and composite materials for application in electronics.

**Prof. Praveen J.** completed his B.E degree in Electrical and Electronics from Kuvempu university in the year 1999, M.Tech in VLSI design and Embedded system From Visvesvaraya Technological University in the year 2004 and currently pursuing his Ph.D Degree in Electronics from Mysore University, Karnataka 2010. He is presently working as an Associate Professor & Head of the Department in the Department of Electronics and communication at Alva's Institute of Engineering & Technology, Moodbidri, South Canara, Karnataka, India. His areas of interest are VLSI Design and Testing. He has published two papers in the International Journals and Conferences in his field of expertise. He has delivered invited lectures and organized a few in-house workshops and certificate programmes.