

Low Power 10-Bit Digital-to-Analog Converter in 0.35 μ m Technology

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ABSTRACT

In this paper the design of a low power 10-bit segmented current steering DAC for instrumentation applications is presented. The static performance of segmented DAC depends upon the matching of current sources. The layout and switching scheme of current sources of the DAC is proposed to reduce the mismatch between the current sources for better accuracy and glitch while switching respectively. The prototype is fabricated in 0.35 μ m two-poly three-metal CMOS technology and measurement results show maximum DNL of +0.45/-0.326 LSB and integral non-linearity INL of +1.085/-0.7836 LSB for 3.3v supply voltage. The total power consumption of the DAC is 3.39mW and core area of the DAC is 0.52mm².

General Terms

Instrumentation, Sensor Calibration

Keywords

DAC, INL, DNL, current steering, segmented architecture.

1. INTRODUCTION

Digital to analog converters (DACs) with medium resolution and medium speed are commonly used in instrumentation applications as programmable voltage and current sources, calibration of sensors for digital offset correction, gain adjustment, temperature compensation and in portable instrumentation applications for controlling various parameters of analog parts using digital signals [1]-[3]. The performance of a DAC is specified through static parameters like differential non-linearity (DNL), integral non-linearity (INL); dynamic parameters like settling time, glitch energy and SFDR; transient parameters like settling time. However, good accuracy, low power consumption, small die area and reasonable conversion time are the main specification requirement of DAC for these applications. Among the most popular architectures of DACs that are suitable for these applications are current steering and resistor ladders or strings based [4]-[6]. These architectures are very well suited for implementation in standard CMOS processes and provide a good compromise between occupied area and power consumed.

Current steering DACs are favored for medium to high resolution bits and their ability to drive resistive load without the need of an output buffer. The current steering DAC can be implemented with binary-coded [7], interpolated [8] and segmented architectures. Static performance of the current steering DAC is dependent on the matching of the current cells and segmentation. A segmented architecture provides a good compromise between logic complexity and the overall layout area. Fig. 1 shows the typical block diagram of the segmented current steering DAC architecture. It consists of

current source array, biasing circuit for current sources, decoders, latches and switch drivers. In binary coded current array, for every increase in digital input, the current in the output is increased in the multiple of 2. The advantage of binary-weighted array is its simplicity as no decoding logic is required and hence area occupied is less. The major drawback is with the mid-code bit transition (0111 \rightarrow 1000), as all the switches are switching simultaneously which results in a glitch at the output. Such a mid-code glitch contains nonlinear

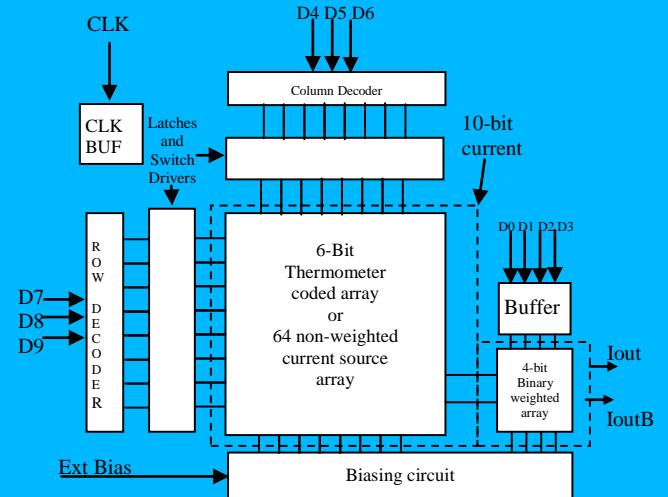


Fig. 1. Typical current steering digital-to-analog converter architecture

signal components, even for small output signals and will manifest itself as spurs in the frequency domain. In thermometer-coded array, each unit current source is connected to a switch controlled by the signal coming from the binary-to-thermometer decoder, latches and switch drivers. When the digital input increases by one bit, one more current source is added to the output. Assuming positive-only current sources, the analog output is always increasing as the digital input increases. Hence, monotonicity is guaranteed using this architecture. The segmentation ratios of the current sources also optimize digital area and analog area. In the proposed architecture the 10-bit current source array is segmented into 4-bit binary coded and 6-bit thermometer coded array, which make up array of 4 LSB bits [D0-D3] and 6 MSB bits [D5-D9] to optimize the performance and area of the DAC [6].

In this paper, a 6 MSB and 4LSB segmented current steering design is presented for low power, medium rate (5MSPS), 10-bit resolution implemented in 0.35 μ m two-poly three-metal AMS technology. Also, a layout strategy and accordingly the switching of the current sources are proposed. Section II describes the unit current cell, biasing of the current cell.

Section III provides proposed layout and switching scheme of the currents cells of DAC architecture and Section IV describes the testing and measurement performed on five prototypes.

2. UNIT CURRENT CELL

The structure of unit current cell is shown in Fig. 2b. M1, M2 are differential switches to control the current at the output nodes out1 and out1b respectively. Out1 and Out1b are loaded with external resistor (R_{ext}) of 2k Ω to produce an output voltage. M5 is the unit current source. To increase the output impedance, M5 is cascoded with transistor M4 that reduces the variation at the drain of M5 when the input in1, in1b makes transition from low to high and vice-versa.

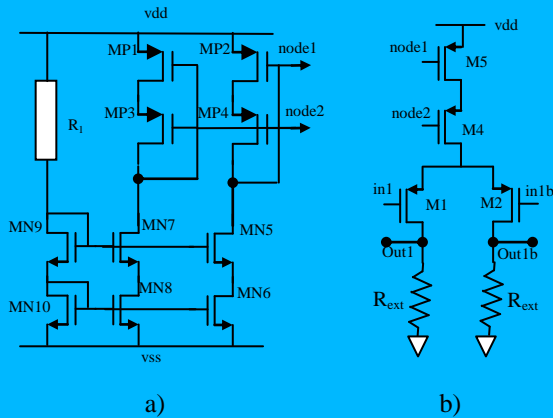


Fig. 2. a) Biasing circuit for the unit current source and b) Unit current cell.

The cascoded current source in the unit current cell are biased using a cascoded current mirror MP1-MP4 and MN5-MN10 transistors as shown in Fig. 2a. An external current source or resistor (R_1) is used as the reference current and this current is mirrored through NMOS cascoded current mirror (MN5-MN10) to each branch of the cascoded PMOS current sources. The digital logic that is used to latch and drive the switch is shown in Fig. 3. The crossing point of the rising/falling waveforms of in1 and in1b to the gates of the switches M1, M2 (in Fig. 2b) is important in reducing the glitch caused if both switches are momentarily turned off. The circuit proposed in [9] is used here that ensures symmetric switching and thus greatly reduces distortion in the output spectrum.

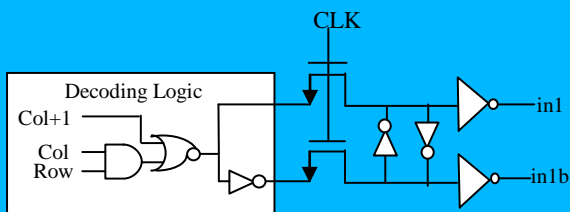


Fig. 3. Latch and Switch driver

3. PROPOSED DAC LAYOUT ARCHITECTURE

Fig. 4 shows the proposed layout of DAC. Quadrants {I, II, III, IV} form the unary plane and quadrant V is the binary weighted plane. Each box in the quadrants contains cascoded current source (M4, M5) that are matched within the cell and also at cell level in the layout. Switch matrix contains switch transistors (M1-M4) for each current cell of the thermometer

coded array and are selected using row decoder and column decoder for the corresponding digital input code applied.

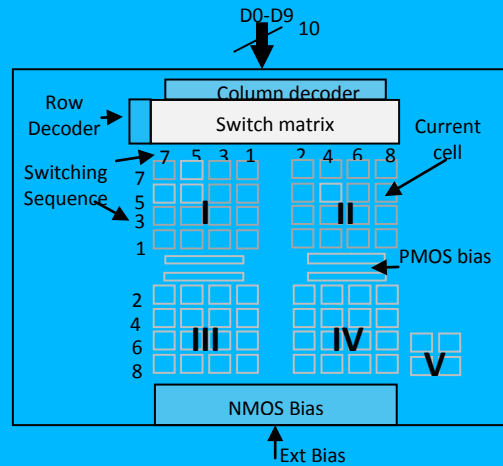


Fig. 4. Layout and Switching sequence of DAC

The local bias and global bias are realized using common-centroid layout to reduce the effects of gradients. Also, the local bias is separated into four quadrants. Although breaking up the biasing of the main matrix into four quadrants is helpful in reducing the current gradients within each quadrant, still they could affect the INL behavior. To solve this problem, the order of the columns and rows were shuffled, as shown in the Fig. 4. Dummy transistors are placed within the cell to make sure that each current cell experiences the same environment.

4. MEASUREMENT RESULTS

The 10-bit DAC has been implemented in two-poly three-metal CMOS technology. The die photograph is shown in Fig. 5. The core area of the chip is 0.52mm².

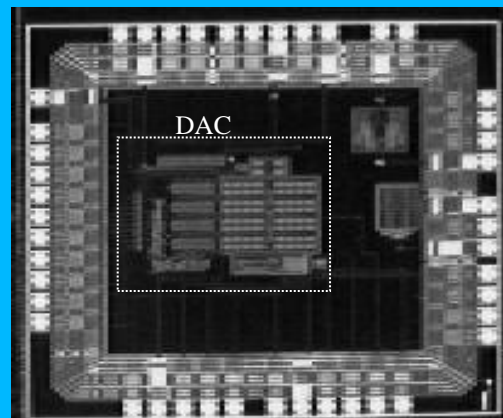


Fig. 5. Die photograph of the DAC

4.1. STATIC MEASUREMENTS

Fig. 6 shows the PCB for the testing of DAC. Lab-view program is used to generate digital input code from 0 to 1023, which is interfaced with PCI card. The analog output voltage of the DAC is read in Agilent multi-meter. The displayed data on multi-meter is read through lab-view program. The lab-view stores the analog output voltage in a text file. The clock for the DAC under test is given from function generator (Tektronix AFG3022B). Fig. 7 shows static measurement results of the DAC and Table 1 show the DNL and INL measurements done across 5 prototype chips. The process

variation across the die and mismatch of the current sources within the DAC causes DNL and INL variation for different prototypes. However, the proposed layout scheme keeps the values of DNL and INL within $\pm 0.5\text{LSB}$ and $\pm 1.1\text{LSB}$ respectively across different prototypes without any calibration to the DAC.

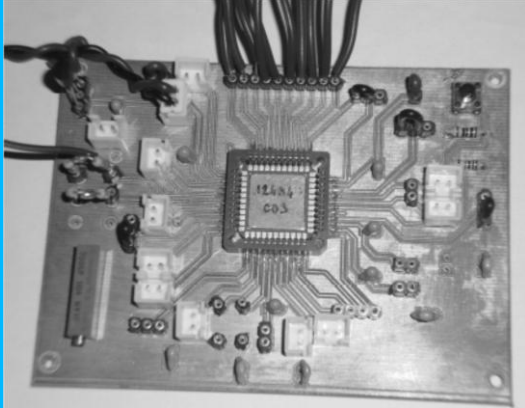
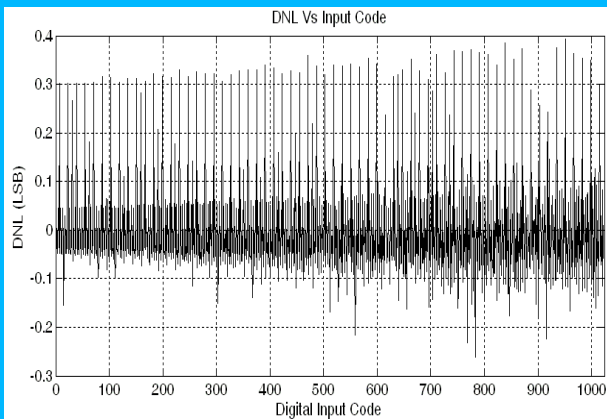
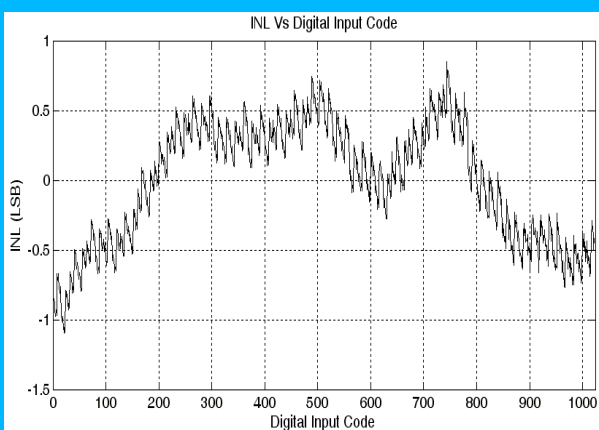


Fig. 6. PCB setup for testing of DAC



a)



b)

Fig. 7. Static measurement for a) DNL of 0.39355/-0.26155 and b) INL of 0.84224/-1.0997 with resistive load of 2K

Table 1: DNL/ INL Measurements for five prototype chips

Chips	DNL (Max/min)	INL (Max/min)
1	0.39355/-0.26155	0.84224/-1.0997
2	0.4149/-0.4072	0.7836/-1.1022
3	0.45/-0.326	1.085/-0.7836
4	0.4122/-0.242	0.9656/-0.756
5	0.3344/-0.3963	0.706/-0.976

4.2. TRANSIENT MEASUREMENTS

The transient performance of the DAC is important for instrumentation applications such as calibration of ADCs, sensors that decides how fast the system gets calibrated. However, rise/fall time of the DAC depends upon the output load capacitance. The worst-case settling time is measured when the digital input code is changed from 0 to 1023 and 1023 to 0 when the load capacitance is 10pF and clock frequency is 5MHz as shown in Fig. 8. In this case the observed rise time is below 100ns.

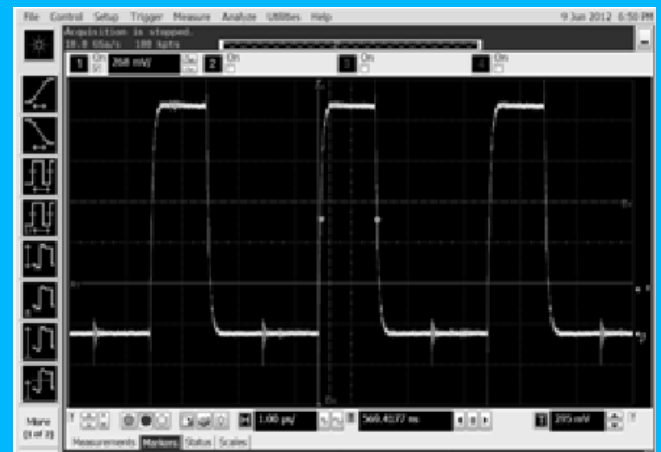


Fig. 8. Transient response of the DAC with capacitive load of 10pF shows rise time and fall of 100ns (approx.)

5. CONCLUSION

The design and measurements of a 10-bit, low-power, small-area current steering CMOS DAC that is implemented in 0.35um two-poly three-metal CMOS technology is presented. The circuit core occupies an area of 0.52mm^2 . With the proposed layout and switching scheme the DNL and INL obtained are $+0.45/-0.326$ LSB and $+1.085/-0.7836$ LSB respectively with a power consumption of 3.39mW that are well-suitable for instrumentation applications.

6. ACKNOWLEDGEMENT

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7. REFERENCES

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