Aerial Monotonic based Layer Assignment on 3D Global Routing

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ABSTRACT

The complexity and routability of layout depends on the number of layers, which can be used for the completion of interconnections. The global routing can be solved by graph based techniques. Efficient 3D routing methods are efficient to minimize the via overflows and total number of vias. The minimization methods rip-up and reassignment for a integer programming based layer assignment. Benchmark process is used to achieves performance of routability and minimum wire length.

General Terms

Algorithms, Design.

Keywords

Global Routing, Integer Programming

1 INTRODUCTION

As VLSI design complexity continues increasing and semiconductor manufacturing advances to the nanometer scale, interconnection delay begins to dominate the circuit delay. Placement and routing stages mainly determine interconnection delay, where placement determines the lower bound of total wirelength and routing realizes physical wires to determine final wirelength. In recent years , there has been an increasing amount of literature concerning routing issues for nanometer designs, including global routing for nanometer designs, variable-rule routing [5] [7] [8] , double-via-aware routing [2] , lithography-friendly routing [4], and density driven routing, etc.

Conventional routing flow is composed of global routing and detailed routing. Global router identifies a global path for every net to constraint the path searching conducted by detailed router within the global path. Path search space is substantially reduced and path searching time is thus massively dropped. Meanwhile, global routing result can offer a good estimation of routing congestion and routed wirelength. 2-D global routing determine the global path for each net, while 3-D global routing additionally determines the used layer of every routing path. Mostly, 3-D global routing is accomplished by 2-D global routing as well as layer assignment. The ideal approach for interconnection optimization is to undertake a simultaneous placement and global routing[12] or take interconnection delay into account in early stage. The necessity for fast and efficient global routing algorithms for cooperating with placers and tackling modern designs with high congestion and complexity is increasing. The most popular global routing approach is iterative rip up and reroute based. The approach first breaks each multi-pin net into a set of two-pin nets. Then the two pin nets are routed sequentially based on a predetermined order. The routing solution is iteratively refined by rip-up and reroute until reaching acceptable quality. For the ISPD07 and ISPD08 global routing contest benchmarks, it successfully generates 8 out of 16 congestion free solutions in very short runtime. The rest of this paper is organized as follows. Section II presents background. Section III gives an overview of the router. Section IV presents the 3-D global routing technique. Section V describes the layer assignment algorithm. Section VI draws conclusions.

2 BACKGROUND

Global routing is usually formulated as a graph problem and addressed with a suite of graph algorithms.

2.1 Global Routing: Problem Formulation

The problem of global routing can be characterized as follows: there is a grid-graph G specifying a set of vertices V and a set of edges E. As shown in Figure 1, each vertex v_i 2 V corresponds to a particular rectangular region (or cell) of the chip, and each edge e_{ij} 2 E corresponds to a boundary between adjacent vertices (with a maximum allowable resource m_{ij}). There is also a set of nets N, where each net n_i 2 N is composed of a set P_i of pins (with each pin corresponding to a vertex v_i). A solution is a mapping of nets to routes, in which each route connects all the pins of a net using the edges of the graph G. When evaluating a routing solution (or, for that matter, a routing engine), one is typically concerned with three metrics. Overflow refers to the total amount of demand that exceeds capacity over all edges. As it directly corresponds to the routability of the design, overflow is minimized (ideally zero). Wirelength is the combined length of segments needed to route all nets, and should also be minimized. In three-dimensional routing, this calculation can also include vias, special wires used to connect segments between adjacent layers of metal. Finally, one may be concerned with the runtime needed to construct the solution. This is especially true in cases where global routing is repeatedly used to guide a placement algorithm. Global routing is a textbook example of a multi-objective optimization problem, in which the relative importance of the individual criterion depends heavily on the greater context and application. As is illustrated in figure 1, the whole routing region is partitioned into a number of global bins. Each global bin is represented by one node and each common boundary is represented by one edge in the grid graph. The edge is called global edge with the capacity of c_e. The overflow is defined as how much is usage u_e over the c_e. If u_e is smaller than c_e, $o_e = 0$, otherwise $o_e = u_e - c_e$.

2.2 Global Routing: Basic Algorithms

Numerous algorithms for global routing are discussed in a comprehensive survey on the topic [19]. However, best performing routers draw upon only on a subset of these techniques.

Krushkals algorithm has been widely employed in path searching of various routing problems and promises to identify a feasible path for a routing problem that has a feasible solution. However krushkal algorithm costs large runtime for the routing of large modern designs. Hence initial routing generally applies another fast routing algorithm, such as pattern routing or monotonic routing.

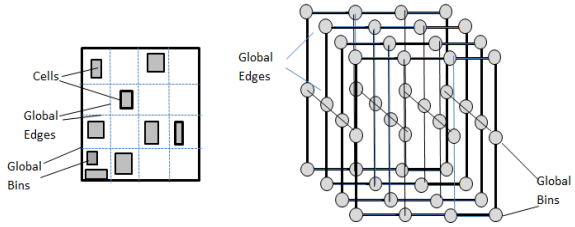

Figure 1: The bin decomposition and grid graph of the global routing problem formulation. (a) Global bin decomposition (b) Corresponding grid graph

The most commonly used patterns are L-shaped or Z shaped patterns. Pattern routing used in multi-net routing offers extremely fast routing speed at the cost of worse routing quality than maze routing. Monotonic routing is another very fast routing technique and produces a path without detour as well. 3D aerial-monotonic routing path in aerial view, it is monotonic In lateral view, it can detour Escaping-point routing path Allowing detour easy to avoid congested regions It is composed of 2 monotonic routing paths.

2.3 Global Routing Benchmarks

In both ISPD2007 and ISPD2008 global routing contests, 3-dimensional benchmarks include the costs on vias for performance evaluation to encourage the global routers to consider the via effect. There are two categories of 3D techniques. The first category tries to solve the 3D problem directly on the 3D routing grids, The second category employs layer projection to transform the 3D routing problem into a 2D one. After solving the 2D problem, the 2D solutions are mapped to 3D ones by layer assignment. Almost all recent global routers. Although theoretically the direct 3D technique should produce better solutions, in practice it is less successful in both solution quality and runtime than 2D routing with layer assignment. Router can generates solutions successfully on these benchmarks

ISPD 07	ISPD 08
adaptec1 3d	bigblue1 3d
adaptec2 3d	bigblue2 3d
adaptec3 3d	bigblue3 3d
adaptec4 3d	bigblue4 3d
adaptec5 3d	newblue4 3d
newblue1 3d	newblue5 3d
newblue2 3d	newblue6 3d
newblue3 3d	newblue7 3d

3 OVERVIEW OF ROUTER

A designed framework to perform 3D global routing effectively and efficiently. This study tries to minimize overflow and wirelength in 3D global routing via simulated evolution based rip-up and rerouting using aerial monotonic routing.finally, the number of vias is minimized in the layer assignment for 3Dglobal routing.

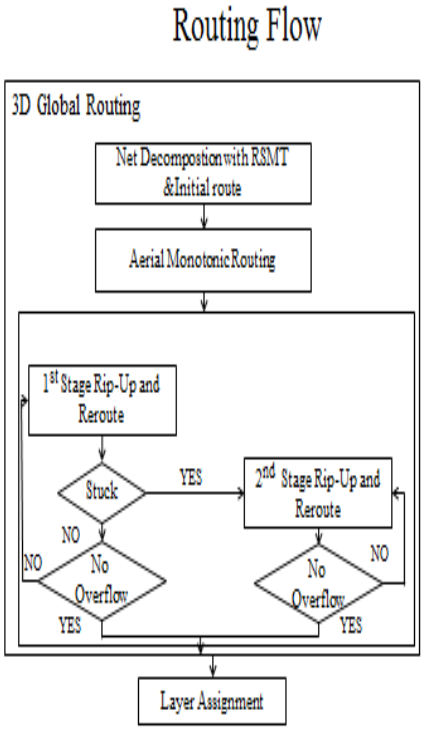

Figure 2: Design flow of the router

4 3-D GLOBAL ROUTING

3D global routing is more flexible . Solves the 3D global routing problem Minimizes wire length and via simultaneously Routes can go up and down The AMR algorithm iteratively performs the two phase operations of the pile update and pile propagation. The AMR and EPR algorithms are used to finds an optimal 3D aerial monotonic routing path. 3D aerial monotonic routing path, that does not contain any detour from an aerial view, but it contains detours from a lateral view. Escaping point routing path, when a net is in a very congested region, it is desired to finds a path with u turns or detour to escape from the net bounding box for congestion optimization. Solves the 3-D Global Routing Problem directly Does not apply layer assignment and directly works on 3-D Steiner routes Minimizes wirelength and via cost simultaneously, and cost in general Does not decompose into multi-terminal nets Tends to route as many nets as possible without overflow Quickly gets rid of the dummy variables by assigning large penalty factor . The formulation can thus handle the 3D GR problem to include both wirelength and via cost as the cost of a route.

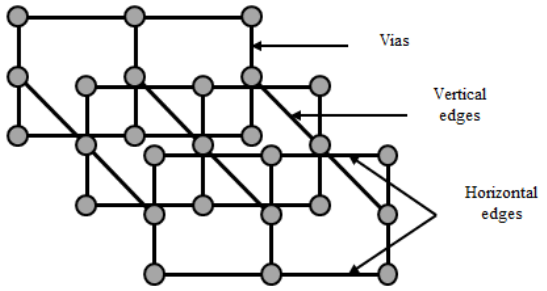

Figure 3: 3-D Global routing

4.1 Global Routing Cost Functions

Every global routing method depends on the evaluation metric employed to measure the goodness of the technique. There are two traditional primary objectives in the automated global routing problem: minimizing chip area and achieving routable designs. For the standard-cell layout style, since the total chip area is approximately equal to the area of the modules plus the area occupied by the interconnect, minimizing the wire-length is approximately equivalent to minimizing the chip area. Congestion minimization is another important objective of global routing. Each connection may have multiple possible paths, and by selecting an appropriate set, the routing demand in any given area can be reduced such that all the nets can be routed without exceeding the track capacity of each routing channel. As the routing layers have been increased to more than two, the number of vias or vias plays a vital role in the routability and timing of the nets. Minimizing the number of vias tends to reduce the number of metal contacts in the routing, therefore, improving the performance of the circuit.

5 LAYER ASSIGNMENT

In layer assignment work, net decomposition offers more accurate assignment order; besides a layer assignment algorithm with layer shifting technique is proposed to further reduce congestion by pushing away early assigned nets to increase the flexibility of later assigned nets. Two-pin net assignment Consider the usage assignment of one single two-pin net, the usage ready to be assigned within the bounding box. Without loss of generality, here we discuss the assignment for vertical edges. The same criteria will be applied for horizontal edges.

The layer assignment has the following improvements:[1]

1) refined net ordering by net decomposition;
2) via minimization of a net by integer programming based layer assignment with layer shifting and rip-up and reassignment.

5.1 Integer Programming Formulation

In a mathematical description of the global routing problem, we are given a grid-graph G = (V,E) describing the network topology, a set of (multi-terminal) nets given by N = {T1, T2, . . . , TN}, (with Ti ⊂ V), and edge capacities ue and weights ce ∀e ∈ E. Denote by T (Ti) the collection of all Steiner trees (routes) connecting the terminals in Ti, and let the parameter ate = 1 if Steiner tree t contains edge e ∈ E, ate = 0 otherwise. Define the binary decision variable x_{it} that is equal to 1 if and only if net Ti is routed with route t ∈ T (Ti). An integer program for the global routing problem can be written as,

$$\min \sum_{i=1}^{N} \sum_{t \in \Gamma(T_i)} c_{it} x_{it}$$

$$\begin{cases} \sum_{t \in \Gamma(T_i)} x_{it} = 1 & \forall i = 1, \cdots, N \\ \sum_{i=1}^{N} \sum_{t \in \Gamma(T_i)} a_{te} x_{it} \le u_e & \forall e \in E \\ x_{it} = \{0,1\} & \forall i = 1, \cdots, N, \ \forall t \in \Gamma(T_i) \end{cases} \quad (1)$$

The formulation (ILP-GR) has a number of appealing properties. The exact properties of the route, such as topology and metal layer can be incorporated into the "cost" of a route. The objective is to minimize this cost. The formulation can thus handle the 3D GR problem to include both wire length and via cost as the cost of a route. It then avoids a traditional layer-assignment phase which can be a source of sub-optimality. A pin assignment algorithm used to provides better routing results.

5.2 Column Generation

The first step in an IP-based approach to global routing is to solve the linear-programming (LP) relaxation of (ILP-GR), a relaxation obtained by replacing the binary requirement on the variable $x_{it} \in \{0, 1\}$ with a non-negativity restriction $0 \le x_{it} \le 1$. The linear program is solved by a column-generation (CG) procedure

$$\max \sum_{i \in N} \lambda_i + \sum_{e \in E} \pi_e u_e$$

$$\begin{cases} \lambda_i + \sum_{e \in t} \pi_e \le c_{it} & \forall i \in N, \forall t \in S(T_i) \\ \pi_e \le 0 & \forall e \in E \\ \lambda_i : free & \forall i \in N \end{cases} \quad (2)$$

By linear programming duality, if the solution satisfies all the dual constraints (2), then (ˆx, ˆs) is an optimal solution to the LP relaxation of (ILP-GR).

Table 1.ISPD07 BENCHMARKS

Name	#Nets	Grids	#Pins	# r. nets
adaptec1 3d	219794	324x324	824734	177k
adaptec2 3d	260159	424x424	911964	208k
adaptec3 3d	466295	774x779	1657913	368k
adaptec4 3d	515304	774x779	1706575	401k
adaptec5 3d	867411	465x468	2857283	581k
newblue1 3d	331663	399x399	1060921	271k
newblue2 3d	463213	557x463	1517918	374k
newblue3 3d	551667	973x1256	1612116	442k

6 CONCLUSION

This work proposes a high-performance of 3-D global router. This study also presents two routing methods for 3-D global routing aerial monotonic routing and simulated evolution-based rip-up and rerouting using a cost function. It also presents a integer programming-based layer assignment by using a layer shifting algorithm followed by layer rip-up and reassigning to further reduce the number of vias. Benchmark process is used to achieves performance of routability and minimum wire length. In future work detailed routing can be used to places actual wires within regions indicated by the global router and minimize the interconnect length and minimize the critical path delay.

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