

Hierarchical Electro-Optical Hybrid Arithmetic Circuits and Systems

Ekkurthi.Sreenivasa Rao
Professor of E.C.E,
Vasavi College of Engineering,
Hyderabad

M.Satyam
Professor of E.C.E (Retd.),
IIIT, Hyderabad

K.Lal Kishore
Professor of E.C.E (Retd.),
J.N.T.University, Hyderabad

ABSTRACT

Logic gates and arithmetic circuits are the basic building blocks for developing large and complex systems like Arithmetic Logic Unit (ALU) of a digital computer system. Most of the research groups have reported logic gates and combinational circuits, which responds to only one stimulus namely either electrical or optical signals. This paper reports a novel approach called hybrid approach in realizing electro-optical combinational logic circuits and systems. An electro-optical hybrid logic circuit is defined as a circuit which accepts electrical and/or optical signals and produces both electrical and optical signals. First, hybrid logic function to perform the EX-OR operation is discussed and its functionality has been demonstrated. Later, the hybrid EX-OR gate is used as a basic building block in realizing higher level hybrid combinational arithmetic circuits like hybrid half adder and full adder. These hybrid logic circuits are of great importance, where electrical and optical systems have to coexist namely, computing, communication, instrumentation and control systems. One direct application of these hybrid combinational circuits is in developing hybrid arithmetic unit in a computer system where information can be processed either electrical or/and optical means and have the advantages of both the systems.

Index Terms — Hybrid Circuits, Hybrid Logic Gates, Hybrid Opto-Electronics, Optical Computing, Optical Logic Gates.

1. INTRODUCTION

There are several conventional logic families evolved in electrical domain due to the special requirements of application areas. Electrical logic circuits are extensively used because of their propagation characteristics and availability of versatile devices and systems. It is found in the literature that optical logic devices and circuits [1-11] are becoming more and more popular because of their immunity from electromagnetic interference, speed of operation, reduced cross talk and higher isolation. The coexistence of electrical and optical systems are quite common and well known in modern communication, computing and signal processing because of the advantages of one system over the other. Thus, treating these two disciplines as one domain seems to be appropriate as the gap between these two systems is coming down and it is quite likely that future systems have lot of common features. If these two systems are combined together, one has to think of hybrid logic circuits which can take either electrical and/or optical signals and produces both electrical and optical signals. Therefore, an attempt has been made by authors of this paper, to combine these two physical systems and the new area is named as electro-optical hybrid logic circuits [12]. These hybrid logic circuits are of great importance, where electrical and optical systems have to coexist in the areas like communication,

computing, modern devices and systems. Computer aided circuit simulation tool is very useful to study and verify circuits/systems design and to predict the behavior that is some times difficult to obtain with laboratory prototype measurements. Therefore, OrCAD CAPTURE circuit simulation tool has been used to carry out the research work. In hierarchical design procedure, basic and smaller circuit blocks called hierarchical circuit blocks are created first. Later, by instantiating these smaller hierarchical circuit blocks, larger and complex circuit blocks are implemented. Hybrid EX-OR gate is the basic building block for realizing hybrid combinational arithmetic circuits like half adder, full adder etc.. Therefore, in the first instance, realization of hybrid EX-OR gate using hierarchical design procedure with OrCAD CAPTURE circuit simulation tool is discussed, and thereafter higher level hierarchical hybrid combinational circuits like hybrid half adder and full adder are discussed.

2. HYBRID EX-OR GATE

The authors of this paper have reported hybrid logic circuits [13-14] to perform logic functions like inverter, NAND, NOR, AND, OR and hybrid sequential logic functions like RS flip flop [15-16]. The functionality of these hybrid logic functions have been demonstrated by carrying out experimental work. Realization of hybrid logic gates and sequential logic functions has clearly demonstrated that these hybrid logic circuits are cascadable and large and complex hybrid logic circuits and systems can be realized. In continuation of this though process, an attempt has been made to realize the hybrid EX-OR gate. The block diagram of hybrid EX-OR gate is shown in Fig 1.

The hybrid EX-OR gate is realized using hybrid inverter, AND and OR logic gates as basic hierarchical building blocks. In this block diagram, $E_i/E_{i1}/E_{i2}$ are the electrical input terminals and $I_i/I_{i1}/I_{i2}$ are the optical input terminals of hybrid logic gates. Similarly, E_o is the electrical output and I_o is the optical output terminals of the hybrid logic gates. The inputs to the hybrid EX-OR gate are electrical or/and optical signals and produces both electrical and optical signals as the output. In this block diagram, V_{i1} and V_{i2} are electrical inputs, I_{i1} and I_{i2} are optical inputs to the hybrid EX-OR gate. $V_{i1} \oplus V_{i2}$ is the electrical output and $I_{i1} \oplus I_{i2}$ is the optical output of the hybrid EX-OR gate. The main objective of this paper is to demonstrate the functionality of basic hybrid arithmetic circuits and to show how larger and complex arithmetic circuits and systems can be build using hierarchical design procedure with OrCAD CAPTURE circuit simulation tool. Simulation of hybrid EX-OR gate is discussed in the following, using hierarchical design procedure with OrCAD CAPTURE circuit simulation tool.

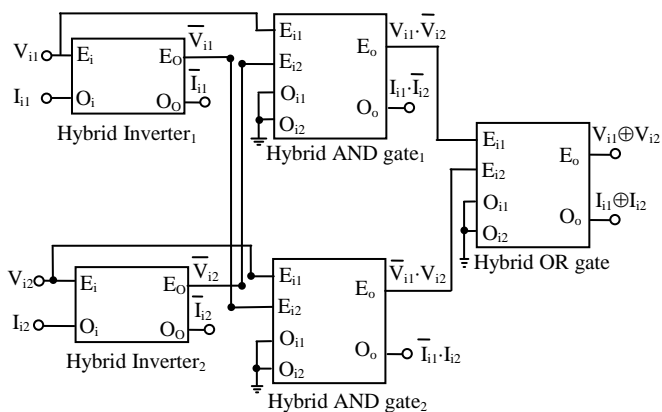


Fig 1: Block diagram of hybrid EX-OR gate.

To realize the electro-optical hybrid arithmetic circuit blocks, Light Emitting Diode (LED) which can give optical output and phototransistor which can respond to electrical/optical signals are used. Since alignment of light source and photo detectors are involved in realizing hybrid arithmetic circuits, it is proposed to use optocouplers as they are available with perfectly aligned Light Emitting Diode (LED) and the phototransistor in a single IC package. Hence, optocouplers (4N32) have been used for implementing and verifying the functionality of hybrid arithmetic circuits. As there is no access to measure the light output power of LED in the optocoupler, an LED model available in the library of OrCAD CAPTURE circuit simulation tool has been used to calculate the light output power based on the current flowing through the LED. To verify the hybrid EX-OR logic function, simulation is carried out using bias point analysis procedure for different combinations of electrical or/and optical logic values. The simulation results are given in Table 1.

Table 1. Simulation results of hybrid EX-OR gate.

Electrical inputs (V)		Electrical output (V)	Optical output (mW)
V ₁₁	V ₁₂		
0	0	0	0
0	5	4.8	9.6
5	0	4.8	9.6
5	5	0	0
Optical inputs (mW)		Electrical output (V)	Optical output (mW)
I ₁₁	I ₁₂		
0	0	0	0
0	10	4.8	9.6
10	0	4.8	9.6
10	10	0	0
Hybrid inputs		Electrical output (V)	Optical output (mW)
I ₁₁ (mW)	V ₁₂ (V)		
0	0	0	0
0	5	4.8	9.6
10	0	4.8	9.6
10	5	0	0

From the Table 1, it may be noted that when both the inputs to the EX-OR gate are same logic level values, the EX-OR gate produces both electrical LOW and optical LOW as outputs. If

the inputs are different logic level values, the EX-OR gate produces both electrical HIGH and optical HIGH logic level values as outputs. Thus, the hybrid EX-OR logic function is demonstrated. Hybrid EX-OR gate is implemented using 2 hybrid inverters, 2 hybrid AND gates and 1 hybrid OR gate. Using the hybrid EX-OR gate as the basic hierarchical building block, hybrid half adder has been implemented and discussed in the following section.

3. HYBRID HALF ADDER

Hybrid half adder is a combinational arithmetic circuit which is used to perform addition of two single bits and produces a SUM and a CARRY. Block diagram of hybrid half adder is shown in Fig 2. The hybrid half adder is realized by using hybrid EX-OR gate and hybrid AND gate. The hybrid EX-OR gate is created as hierarchical circuit block and then used along with the hybrid AND gate to obtain the hybrid half adder.

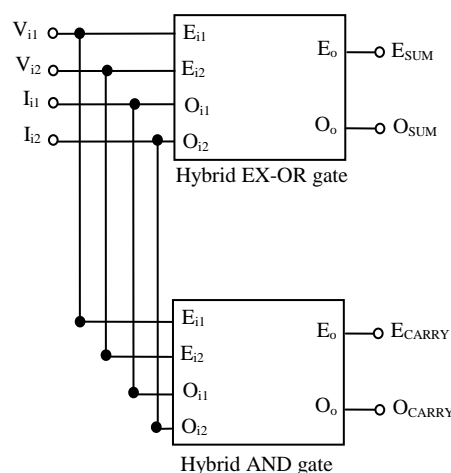


Fig 2: Block diagram of hybrid half adder.

In the hybrid half adder block diagram, E₁₁/E₁₂ are the electrical input terminals and I₁₁/I₁₂ are the optical input terminals. Similarly, E_{SUM} and E_{CARRY} are the electrical output and O_{SUM} and O_{CARRY} are the optical output terminals of the hybrid half adder. In this block diagram, V₁₁ and V₁₂ are electrical inputs and I₁₁ and I₁₂ are optical inputs. The Boolean expressions for the electrical SUM and CARRY outputs of the hybrid half adder are given by,

$$E_{SUM} = V_{11} \oplus V_{12} \quad (1)$$

$$E_{CARRY} = V_{11} \cdot V_{12} \quad (2)$$

Similarly, the Boolean expressions for the optical SUM and CARRY outputs of the hybrid half adder are given by,

$$O_{SUM} = I_{11} \oplus I_{12} \quad (3)$$

$$O_{CARRY} = I_{11} \cdot I_{12} \quad (4)$$

To verify the functionality of hybrid half adder, bias point analysis is carried out using OrCAD CAPTURE simulation tool. The output response for different electrical or/and optical logic combination values is given in Table 2.

From the simulation results given in Table 2, it may be seen that for the given input logic values, the output SUM and CARRY logic level values of the hybrid half adder satisfy the

functionality of hybrid half adder. Thus, the functionality of hybrid half adder is verified. Using the hybrid half adder as the basic hierarchical building block, hybrid full adder has been implemented and discussed in the following section.

Table 2. Simulation results of hybrid half adder.

Electrical inputs (V)		Electrical output (V)		Optical output (mW)	
V _{i1}	V _{i2}	E _{SUM}	E _{CARRY}	O _{SUM}	O _{CARRY}
0	0	0	0	0	0
0	5	4.8	0	9.6	0
5	0	4.8	0	9.6	0
5	5	0	4.8	0	9.6
Optical inputs (mW)		Electrical output (V)		Optical output (mW)	
I _{i1}	I _{i2}	E _{SUM}	E _{CARRY}	O _{SUM}	O _{CARRY}
0	0	0	0	0	0
0	5	4.8	0	9.6	0
5	0	4.8	0	9.6	0
5	5	0	4.8	0	9.6
Hybrid inputs (V)		Electrical output (V)		Optical output (mW)	
V _{i1} (V)	I _{i2} (mW)	E _{SUM}	E _{CARRY}	O _{SUM}	O _{CARRY}
0	0	0	0	0	0
0	10	4.8	0	9.6	0
5	0	4.8	0	9.6	0
5	10	0	4.8	0	9.6

4. HYBRID FULL ADDER

Hybrid full adder is an arithmetic combinational logic circuit which is used to perform the addition of two single bits taking previous carry into account and produces SUM and CARRY outputs. The hybrid full adder is realized by using two hybrid half adders and hybrid OR gate. The hybrid half adder is created as hierarchical circuit block and is used along with the hybrid OR gate to obtain the hybrid full adder.

The block diagram of hybrid full adder which is realized by making use of two hybrid half adders is shown in Fig 3. In the hybrid full adder block diagram, E_{i1}/E_{i2}/E_{i3} are the electrical input terminals and I_{i1}/I_{i2}/I_{i3} are the optical input terminals. Similarly, E_{SUM} and E_{CARRY} are the electrical output and O_{SUM} and O_{CARRY} are the optical output terminals of the hybrid full adder. In this block diagram, V_{i1}, V_{i2} and V_{i3} are electrical inputs and I_{i1}, I_{i2} and I_{i3} are optical inputs. Two inputs (electrical or/and optical) are added in the first hybrid half adder. The E_{SUM1} and E_{CARRY1} produced in the first half adder are given by the following Boolean expressions,

$$E_{SUM1} = V_{i1} \oplus V_{i2} \quad (5)$$

$$E_{CARRY1} = V_{i1} \cdot V_{i2} \quad (6)$$

Similarly, the O_{SUM1} and O_{CARRY1} produced in the first half adder are given by the following Boolean expressions,

$$O_{SUM1} = I_{i1} \oplus I_{i2} \quad (7)$$

$$O_{CARRY1} = I_{i1} \cdot I_{i2} \quad (8)$$

The SUM produced in the first hybrid half adder will be given as one of the input to the second hybrid half adder along with the previous CARRY bit generated. The Boolean expressions for the E_{SUM} and E_{CARRY} outputs of the hybrid full adder is given by,

$$E_{SUM} = E_{SUM1} \oplus V_{i3} = V_{i1} \oplus V_{i2} \oplus V_{i3} \quad (9)$$

$$E_{CARRY} = V_{i1} \cdot V_{i2} + V_{i2} \cdot V_{i3} + V_{i3} \cdot V_{i1} \quad (10)$$

Similarly, the Boolean expressions for the O_{SUM} and O_{CARRY} outputs of the hybrid full adder is given by,

$$O_{SUM} = O_{SUM1} \oplus I_{i3} = I_{i1} \oplus I_{i2} \oplus I_{i3} \quad (11)$$

$$O_{CARRY} = I_{i1} \cdot I_{i2} + I_{i2} \cdot I_{i3} + I_{i3} \cdot I_{i1} \quad (12)$$

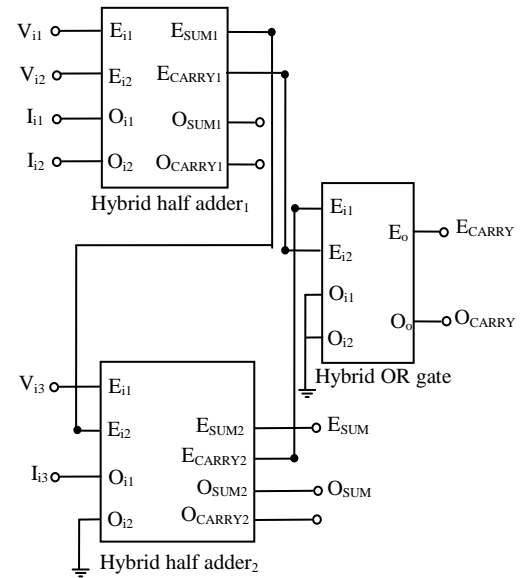


Fig 3: Block diagram of hybrid full adder.

To verify the functionality of hybrid full adder, bias point analysis is carried out using OrCAD CAPTURE simulation tool. The output response for different electrical or/and optical input logic combination values is given in Table 3. From the Table.3, it may be observed that the SUM output of the hybrid full adder becomes logic HIGH, when the number of electrical or/and optical input logic HIGH values are odd number; and CARRY becomes logic HIGH, when two or more electrical or/and optical inputs are logic HIGH values. As shown in the Table 3, the full adder functionality is verified with all electrical input combinations and later with all optical input combinations. At the end, the functionality of hybrid full adder is verified with different combinations of both electrical and optical inputs. From the simulation results given in Table 3, it may be seen that for all the input logic values, the output SUM and CARRY values of the hybrid full adder are within the tolerable logic values. Thus, the functionality of hybrid full adder is verified. The main objective of this research paper is intended to verify the functionality of basic hybrid arithmetic circuits and it is clearly demonstrated that using hierarchical design procedure, it is possible to build higher level complex arithmetic circuits and systems.

Table 3. Simulation results of hybrid full adder.

Electrical inputs (V)			Electrical output (V)		Optical output (mW)	
V _{i1}	V _{i2}	V _{i3}	E _{SUM}	E _{CARRY}	O _{SUM}	O _{CARRY}
0	0	0	0	0	0	0
0	0	5	4.8	0	9.6	0
0	5	0	4.8	0	9.6	0
0	5	5	0	4.8	0	9.6
5	0	0	4.8	0	9.6	0
5	0	5	0	4.8	0	9.6
5	5	0	0	4.8	0	9.6
5	5	5	4.8	4.8	9.6	9.6
Optical inputs (mW)			Electrical output (V)		Optical output (mW)	
I _{i1}	I _{i2}	I _{i3}	E _{SUM}	E _{CARRY}	O _{SUM}	O _{CARRY}
0	0	0	0	0	0	0
0	0	10	4.8	0	9.6	0
0	10	0	4.8	0	9.6	0
0	10	10	0	4.8	0	9.6
10	0	0	4.8	0	9.6	0
10	0	10	0	4.8	0	9.6
10	10	0	0	4.8	0	9.6
10	10	10	4.8	4.8	9.6	9.6
Hybrid inputs			Electrical output (V)		Optical output (mW)	
I _{i1} (mW)	V _{i2} (V)	I _{i3} (mW)	E _{SUM}	E _{CARRY}	O _{SUM}	O _{CARRY}
0	0	0	0	0	0	0
0	0	10	4.8	0	9.6	0
0	5	0	4.8	0	9.6	0
0	5	10	0	4.8	0	9.6
10	0	0	4.8	0	9.6	0
10	0	10	0	4.8	0	9.6
10	5	0	0	4.8	0	9.6
10	5	10	4.8	4.8	9.6	9.6

5. CONCLUSION

This research paper reports a novel approach called hybrid approach for realization of combinational arithmetic circuits which can take electrical and/or optical signals and produces both electrical and optical signals. These hybrid combinational circuits have been realized using hierarchical design procedure with OrCAD Capture circuit simulation tool. The operation of these hybrid arithmetic circuits has been explained through simple theory and their functionality has been demonstrated using simulation. These basic hybrid arithmetic circuit blocks can be used further in building large and complex hierarchical hybrid circuits and systems, as the input and output logic values are almost the same or within the tolerable logic levels. It is felt that this effort would pave the way for developing new branch of electro-optical hybrid circuits and systems which will involve both electrical and optical signals and have advantages of both the systems.

6. REFERENCES

- [1] Beyette.F.R, Jun. Feld, S.A, An. X, Geib.K.M, Hafich. M.J, Robinson. G.Y, and Wilmsen. C.W, "Integrated optical inverter using light amplifying optical switch (LAOS)", *Electron.Lett*, 27(3), pp 497-498, 1991.
- [2] X. An et al., "Optical latch and AND gate based on an InGaAs/InP LOAS", *Proceedings of the photonic switching Conf.*, Mar 6-8, Salt Lake City, UT, 1991.
- [3] F.R. Beyette, Jr., K.M. Geib, S.A. Feld, X. An, M.J. Hafich, G.Y. Robinson, and C.W. Wilmsen, "Integrated optical NOR gate", *IEEE photonics Technology letters*, 4, pp 4, 1992.
- [4] X. An, K.M. Geib, M.J. Hafich, L.M. Woods, S.A. Feld, F.R. Beyette, Jr., G.Y. Robinson, and C.W. Wilmsen, "Integrated optical NAND gate", *Electronic letters*, 28, pp 16, 1992.
- [5] T. Chino et al., "Novel Integrated optoelectronic RS flip flop based on optically coupled inverters," *Elec. Letters*, 28, pp7, 1992.
- [6] K. Matsuda et al., "Dynamic set and reset optoelectronic latching device", *IEEE Photon. Tech. Lett.*, 4, pp 483-485, 1992.
- [7] X. An et al., "Highly compact integrated optical set-reset memory pixels for optical processing arrays", *IEEE photonics Tech. Lett.* 5, pp 5, 1993.
- [8] Avireni Srinivasulu, "Modified Optical OR and AND gates", *Journal of Semiconductor Physics, Quantum electronics & Optoelectronics*, vol.5, no.4, 2002.
- [9] P.K.Roy, Dr.N.Roy, "Optical NAND", *Journal of the institution of engineers (India)*, vol.82, 2002.
- [10] Avireni Srinivasulu and Sivadasan Kottayi, "Optical EX-OR GATE", *Journal of Microwaves & Optoelectronic*, vol.3, no1, 2003.
- [11] Haifeng Zhou, Wanjun Wang, Jianyi Yang, Minghua Wang, Xiaoqing Jiang, " Electro-optical logic application of multimode interference coupler by multivalued controlling", *Journal of Applied Optics*; 50(15), pp 2299-2304, 2011.
- [12] M.K.Ravishankar and M.Satyam "Optically/Electrically (Symmetrically) Triggerable Bistable Multivibrator", *IEEE Transactions on circuits and systems-1. Fundamental theory and applications*, vol.43,no.7, July 1996.
- [13] Ekkurthi.Sreenivasa Rao, M. Satyam, K. LalKishore, "Electro-Optical Hybrid NOR Gate", *Proceedings of NUConE-2007, Nirma University, Ahmedabad*, pp 133-135,2007.
- [14] Ekkurthi.Sreenivasa Rao, M. Satyam, K. LalKishore, "Universal Electro-optical hybrid logic gates" *Semiconductor Physics, Quantum Electronics & Optoelectronics*, 11(1), pp 96-100, 2008.
- [15] Ekkurthi Sreenivasa Rao, M. Satyam, K. LalKishore, "Cascadable electro-optical hybrid RS flip flop" *Proceedings of International conference on Engineering, Technology and Management (ICETM-2012), RG CET, Pondicherry*, pp 254-258, 2012.
- [16] Ekkurthi Sreenivasa Rao, M. Satyam, K. LalKishore, "Realization of cascadable electro-optical hybrid RS flip flop using hybrid NAND gates" *International Journal of Advances in Engineering Science and Technology (IAEST)*, 02(3), pp 219-225, 2012.