Standby Leakage Power Reduction Techniques in Deep Sub-Micron CMOS VLSI Circuits

Sangeeta Parshionikar
P.G..Student and Assistant Professor
Fr. Conceicao Rodrigues College of Engg.
Mumbai University

Deepak V. Bhoir, Ph.D
Head of the Electronics Department
Fr. Conceicao Rodrigues College of Engg.
Mumbai University

ABSTRACT

The use of Very Large Scale Integration (VLSI) technologies in high performance computing, wireless communication and consumer electronics has been growing at a very fast rate. Every generation of VLSI technology reduces feature size of transistor and leads to more powerful and compact wireless devices. The challenge of the advanced VLSI technology is the increase in the leakage power consumption. In deep sub–micron technology, standby leakage power dissipation has emerged as major design considerations. Leakage control is very important, especially for low power applications and handheld devices such as cellular phones and PDAs.

In this paper two techniques such as transistor stacking and sleepy transmission gate for reducing leakage power are proposed. In these techniques, the resistance of the path from Vdd to ground is increased, so that significant reduction in static power is achieved with small increase in delay. This work analyses the leakage power and delay of three basic digital circuits inverter, NAND and NOR gates and the same can extended to any complex digital implementation. The circuits are simulated with MOSFET models of level 54 in 90 nm, 45nm and 32nm process technology.

General Terms

Low-power VLSI design, Leakage power consumption

Keywords

Leakage power, static power, sleep transistor, threshold voltage, stacking. Process Technology

1. INTRODUCTION

Development of low-power VLSI design is essential for current and future wireless devices. The advances in technology enable us to achieve higher density and performance at the same time results in increase in power consumption. In past day‟s technology the magnitude of leakage current was low and usually neglected. In current trends, the supply voltage is being scaled down to reduce dynamic power. The threshold voltages also follow the same scaling trend in order to satisfy the high speed requirements. This decrease of threshold voltages brings an exponential increase in sub-threshold currents [1]. Sub-threshold leakage is the weak inversion current between source and drain of MOS transistor observed when the gate voltage is less than the threshold voltage. Since the leakage current of the transistors determines the static power of a CMOS circuit, the increase in sub-threshold current increases the leakage power consumption of the circuit. Thus the total power consumption of the circuit is increased.

Consequently, power dissipation is becoming recognized as a top priority issue for VLSI circuit design. Leakage power makes up to 50% of the total power consumption in today‟s high performance microprocessors [3]. Therefore leakage power reduction becomes the key to a low power design. Leakage power dissipation is the power dissipated by the circuit when it is in sleep mode or standby mode. Leakage power is given by equation 1 and the propagation delay (Tpd) of a circuit is given by equation 2.

$$Pleak = Ileak * V_{dd} \quad (1)$$

$$Tpd \propto V_{dd} / (V_{dd}-V_{th})^2 \quad (2)$$

Where Ileak is the leakage current that flows in a transistor when it is in off state, V_{dd} is the supply voltage, Vth is the threshold voltage of the transistor. This power dominates dynamic power especially in deep submicron circuits and also in circuits that remains in idle mode for a long time such as cell phones. In all such applications, it is important to prolong the battery life as much as possible and now with growing trend towards portable computing and wireless communication, power dissipation has become one of most critical factor in continued development of micro-electronic technology. Therefore the focus is on the reduction of leakage power dissipation.

The rest of the paper is organized as follows, a review of the related work is presented, in Section 2. In Section 3, the proposed work on a leakage reduction for combinational CMOS logic gates is presented, which is followed by the simulation results and conclusions in Sections 4 and 5, respectively.

2. RELATED WORK

High leakage current in deep-submicron technology is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. This section reviews different approaches for leakage current reduction techniques. All these techniques are effective in reducing leakage power and ultimately all come down to a fundamental set of concepts: dissipation is reduced by lowering supply voltage, voltage swing, physical capacitance, switching activity or by introduction of a high resistance path between VDD and ground.

In self-adjustable voltage level circuit, the output voltage of the circuit is applied to any load circuit [3]. During the active mode

(when SL=0), this circuit supplies maximum supply voltage to the load circuit so that the load circuit can operate quickly. During the standby mode, it provides slightly lower supply voltage to the load circuit through the weakly ON transistors. When drain to source voltage is decreased, the drain induced barrier-lowering (DIBL) effect is decreased and this in turn increases the threshold voltage V_{th} of NMOS transistors. Consequently the sub threshold leakage current of the OFF MOSFETs decreases, so leakage power is minimized, while data are retained.

A technique for leakage power control is Power gating [4], which turns off the devices by cutting off their supply voltage. This technique uses additional transistors (sleep), which are inserted in series between the power supply and pull-up network (PMOS) and/or between pull-down (NMOS) network and ground to reduce the standby leakage currents. The sleep transistors are turned on when circuit are in active mode and turned off when circuits are in standby mode. The input vector method makes use of dependence of leakage current on the input vector to gate [5]. Additional control logic is used to put the circuit in a low-leakage standby state when it is idle and restored to its original state when reactivated. Upon reactivation, the circuit no longer retains the original state information before going into low-leakage standby state. Thus, to retain original state information, it requires special latches thereby increasing the area of circuit by about five times in worst cases. The multi-threshold voltage CMOS (MTCMOS) [7] technique is also a kind of power gating technique which uses high threshold transistors as a sleep transistors and low threshold voltage transistors are used to implement the logic. In dual threshold voltage CMOS technique, transistor of different threshold voltages are used. Low threshold voltage transistors are used for the gates on the critical path to maintain the performance, while high threshold voltage transistors are used for the gates on the non-critical path for reduction of the leakage current.

3. PROPOSED LEAKAGE REDUCTION TECHNIQUES

3.1 Transistor Stacking

The leakage current flowing through a stack of series connected transistors reduces when more than one transistor of the stack is turned OFF. This effect is known as the "Stacking Effect". Sub threshold leakage is exponentially related to the threshold voltage of the device and the threshold voltage changes due to body effect. From these two facts, the sub threshold leakage in the device can reduced by stacking two or more transistors serially. This is because each transistor in the stack induces a slight reverse bias between the gate and source of the transistor right below it, and this increases the threshold voltage of the bottom transistor making it more resistant to leakage [1]. Therefore in Fig. 3.1, transistor T2 leaks less current than transistor T1 and T3 leaks less than T2. Hence the total leakage current through the transistors T1, T2 and T3 is decreased as it flows from Vdd to Gnd. So Ileak1 is less than Ileak2.

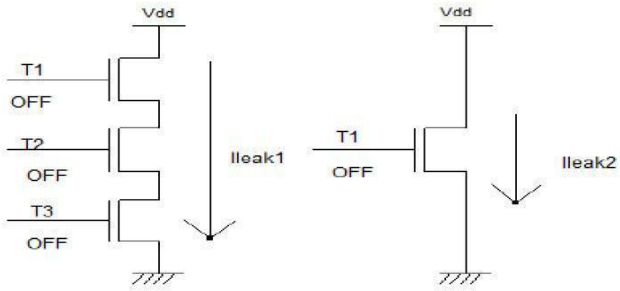

Figure 3.1: Transistor Stacking Effect

3.2 Sleepy transmission gate technique

The idea behind this technique is to reduce leakage power by inserting high resistance between the supply and ground by means of CMOS switch. In comparison with single sleep transistor (PMOS or NMOS) connected between PUN (Pull up network) and PDN (Pull down network), which pass degraded output; the transmission gate is capable of passing logic 1 and 0 well. In addition to that, output logic state is not lost when the circuit enters from active mode to sleep mode and vice-versa [2]. The sleep circuit consists of two complementary MOS transistors S1 (PMOS) and S2 (NMOS). The sleep transistors S1 and S2 are connected in parallel to form transmission gate configuration between PUN and PDN as shown in figure.

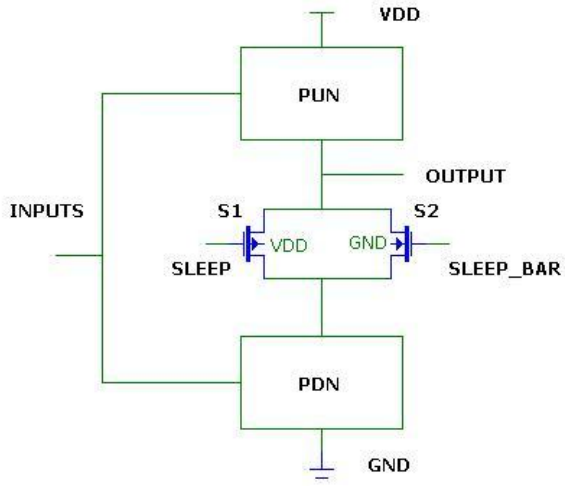

Figure 3.2: Block diagram of Sleepy Transmission gate transistor

The sleep transistors S1 and S2 are high threshold voltage devices and the logic gate transistors are standard threshold voltage devices. This is to provide a well-balanced trade-off between high speed and leakage loss. The CMOS circuit output can be drawn either between PUN and sleep circuit or between sleep circuit and PDN. During the normal (active) mode of operation, „sleep=0" and „sleep_bar=1". This makes the transistors S1 and S2 to turn ON and acts as a transmission gate. Even though the ON resistance of transmission gate is not as high as it"s OFF state resistance, it increases the resistance of VDD to ground path, controlling the flow of leakage currents, resulting in leakage power reduction in active mode. In standby mode of operation, sleep=1" and sleep_bar = 0" makes the transistors S1 and S2 to turn OFF forcing a high-impedance condition between PUN and PDN nodes. Thus, the introduction of sleepy-transmission gate increases the resistance of the path

from VDD to ground during standby mode of operation resulting in reduction of leakage current.

4. SIMULATION AND RESULT

The transistor stacking and sleepy transmission gate techniques were implemented and tested on set of combinational circuits. Inverter, NAND and NOR circuits are implemented and net lists are simulated using Synopsys HSPICE. The implementation of inverter using both the techniques are shown in figure 4.2 and figure 4.3 respectively. Conventional CMOS Inverter is shown in figure 4.1. NAND and NOR circuits are implemented in same way using both the techniques. All circuits were simulated at a temperature of 25°C. Their leakage power was measured in the standby mode of operation. The Berkeley Predictive Technology Models (BPTM) contained process parameters and values for both standard threshold voltage and high threshold voltage devices [12]. The net lists of combinational logic gates are modified with respect to the Berkeley Predictive Technology Models. The modified net lists are also simulated using Synopsys HSPICE for power measurements.

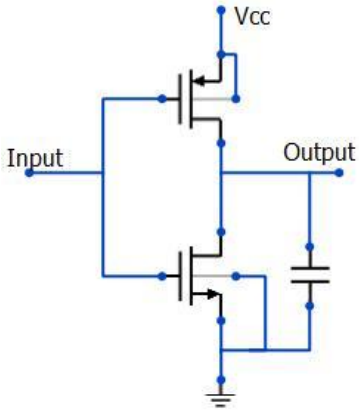

Figure 4.1: Conventional CMOS Transistor

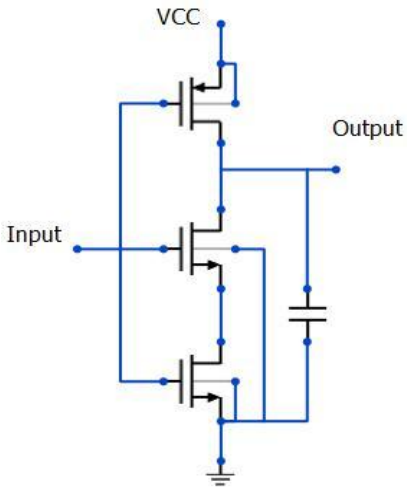

Figure 4.2: Stacked NMOS Transistor Inverter

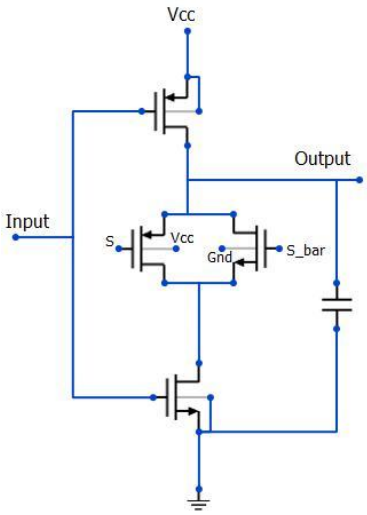

Figure 4.3: Sleepy Transmission Gate Inverter

The proposed methods provide exact logic levels and leakage savings as the process technology shrinks. The leakage power measurements are made for the CMOS inverter, NAND and NOR using 90nm, 45nm and 32nm process technology. Tables I, table II and table III show the simulation results of each circuit for three different process technologies. From the table I, II and III, it is clear that the Sleepy transmission gate technique yield more percentage reduction in standby power compared to the stacking technique.

Table I. Standby Leakage power (W) for Inverter circuit

Process Technology	Base case	Transistor Stacking	Sleepy transmission gate
90n	10.820 9E-12	1.10802E-12	0.997 E-12
45n	56.2534E-09	4.6662E-09	0.2901E-09
32n	29.7287E-06	12.4747E-09	1.52E-09

Table II. Standby Leakage power (W) for NAND circuit

Process Technology	Base case	Transistor Stacking	Sleepy transmission gate
90n	1.11E-12	0.69E-12	0.588E-12
45n	4.66E-09	1.19E-09	0.2415E-09
32n	13.03E-06	5.918E-06	1.519E-09

Table III. Standby Leakage power (W) for NOR circuit

Process Technology	Base case	Transistor Stacking	Sleepy transmission gate
90n	4.0199E-12	1.339E-12	1.12E-12
45n	1.0638EE-06	5.446E-09	0.325E-09
32n	25.974E-06	12.67E-06	0.549E-09

The proposed techniques achieve significant reduction in standby leakage power with increase in propagation delay. Minimal additional circuitry is used to modify the original logic design to force the combinational logic into a low-leakage state during both active and idle mode of operations. Since the power and delay are inter related, increase in propagation delay is minimum. The same is shown in figure 4.5 for NAND gate.

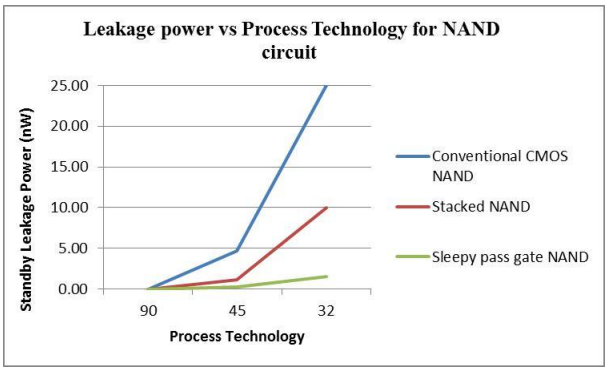

Figure 4.4: Total Leakage Power vs. Process Technology

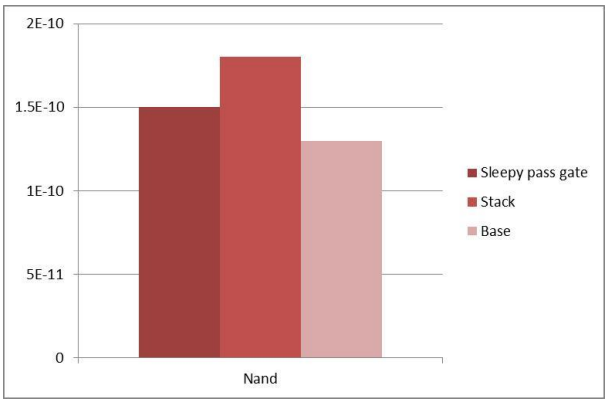

Figure 4.5: Propagation delay for NAND gate

5. CONCLUSION

Scaling down of the supply voltage and threshold voltage along with CMOS technology feature size for achieving high performance has largely contributed to the increase in standby leakage power dissipation. In this paper, for reducing leakage power two efficient techniques such as transistor stacking and sleepy transmission gate are proposed. Three digital circuits Inverter, NAND and NOR are implemented with leakage reduction techniques. The leakage power of all the designs decrease when reduction techniques are applied. The percentage reduction of leakage power is more with the Sleepy transmission gate technique (200X) compared to the Stacking technique. The design of NOR with Sleepy transmission gate gives the minimum leakage power of 5.49nW. The drawback of the Sleepy transmission gate technique is that it requires a controller to automatically generate sleep signals to put the circuit in standby mode and also to activate it when necessary.

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