Digital PWM Control of Synchronous Converter

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ABSTRACT
The proposed system is to utilize the renewable resources by digital PWM control of synchronous converter. Usually PWM pulse is being generated through a digital system such as microcontroller or Digital signal controller. In stand – alone application these controllers increases the cost but XILINX FPGA based PWM generation reduces the cost. XILINX FPGA is invented by XILINX which is being considered as an efficient device for rapid prototyping and also to perform concurrent operations. In this paper two PWM signals was generated to control the switch duty cycles in Bi-directional DC-DC Converter or synchronous converter. In addition to that under various operating modes the proposed circuit is verified by MATLAB / SIMULINK.

Keywords
Bi-directional dc-dc converter, pulse width modulation; Field programmable gate array, XILINX, duty cycle.

1. INTRODUCTION
Interest in utility interactive PV systems has increased for the past few years and more number of central-station photovoltaic systems were installed. It is anticipated that as PV system cost decreases, the residential systems will be installed in increased number. The DC – DC converter performs three functions: implementation of MPPT algorithm, Buck Converter & Battery Charger and Boost Converter.This paper focuses on PWM control of DC – DC converter output voltage depends on the Duty Cycle. XILINX FPGA is employed for complex electronic circuits. Xilinx web pack software 9.2i generates PWM by diagarams and VHDL programs.. The final design is converted in configuration data file and loaded into SPRTAN – 3E board.

2. PROGRAMMABLE LOGIC DEVICES (PLD)

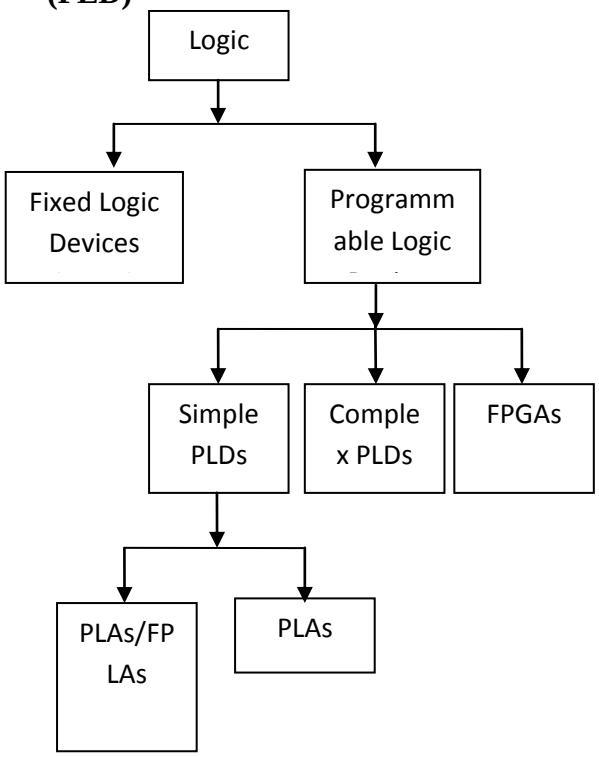

Fig:2 Programmable logic devices

2.1 Field Programmable Gate Arrays (FPGAS)
Field programmable gate arrays (FPGAs) are so-called since structural very much like the now-obsolete "Gate Array" form of (ASIC). Inside the ring of I/O blocks lies a rectangular array of logic blocks and connecting logic blocks to logic blocks and I/O blocks to Logic Blocks is the programmable interconnect wiring.

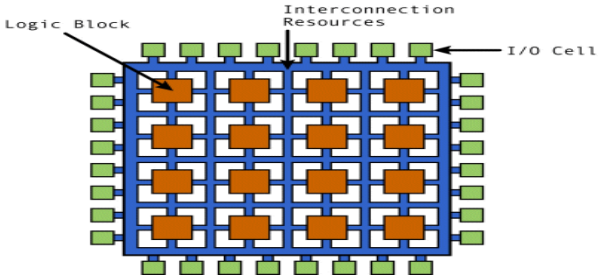

Figure 2.1 FPGA Architecture

2.2 Architecture of FPGA

In FPGAthere will be clock circuit to drive the clock signals to each logic block. ALUs, and the other logic resourcesare also available. The three elements of an FPGA are static Random access memory , anti-fuses and Flash EPOM.

2.3 Configurable logic blocks (CLBS)

These CLBs contain enough logic to create a small state machine as illustrated in figure 2.4. The block contains Random access memory for creation of arbitrary combinational logic functions also known as lookup tables(LUTs)..

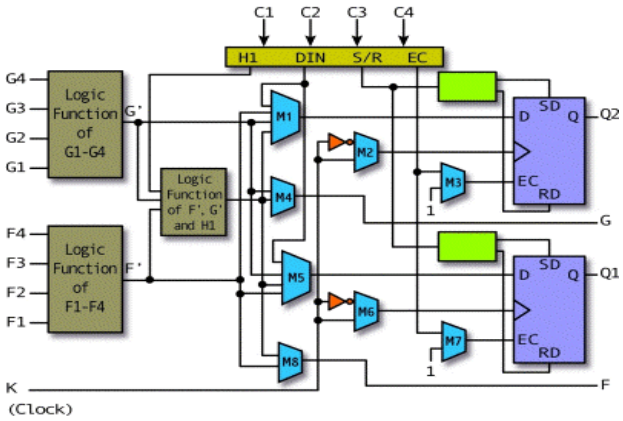

Figure 2.3Configurable Logic Blocks – Xilinx FPGA

The logic blocks within an FPGA can be as small and simple as the macro-cells in a PLD (called fine-grained architecture). But the logic blocks in an FPGA are generally nothing more than a couple of logic gates or a LUT and a flip-flop.

3. SYNCHRONOUS CONVERTER

3.1 Mportance of Dc-Dc Converters For Pv Applications

The choice of dc-dc converter must be taken into account considering the different aspects deriving from the need to supply the load with the greatest efficiency, minimizing volume, weight and cost. From the possibility of implementing control with good dynamic performance and from the reduction of filtering costs, which govern the choice of switching frequency range Different circuit technologies for switching power supply are available.The most suitable switching frequencies are found for the different topologies and applications. The findings provide pointers to the optimum solutions in the case where optimization of efficiency and/or minimization of weight and space occupied by the dc-dc converter are the key points of issue.

3.2 Proposed circuit topology of synchronous converter

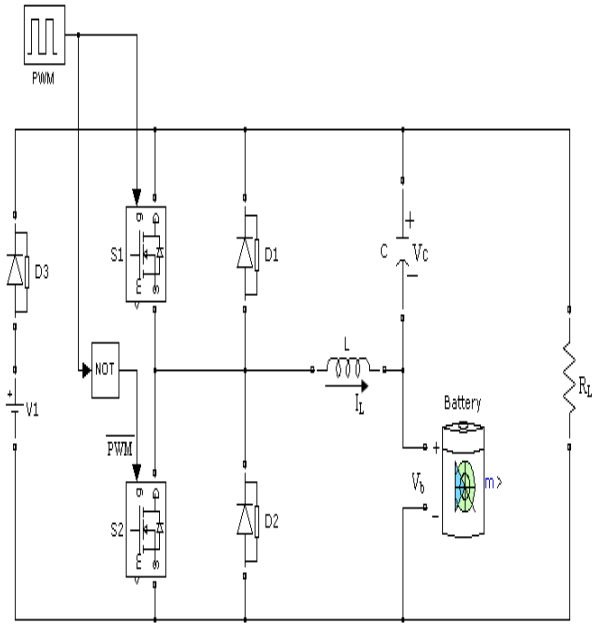

Figure 3.2 Bi-directional DC – DC Converter

If the supply voltage is not enough to supply the load, the power system operates as a boost converter, transferring energy from the battery to the load. In this case, while the switch S2 is turned ON, the inductor L stores energy from the battery as shown in Figure 3.4 & 3.5 When the switch S2 is turned OFF, the energy stoRed in the inductor is fed back to the Load .

4. FPGA BASED PWM GENERATION

4.1 Generation of duty cycle

The duty cycle k can be generated by comparing a dc reference signal V_r, with a saw tooth carrier signal V_{cr}. This is shown in fig---, where V_r is the peak value of V_r and vcr is the peak value of V_{cr}, the reference signal.Where M is called the modulation index. By varying the carrier signal vcr from 0 to vcr, the duty cycle k can be varied from 0 to 1.

4.2 Algorithm to generated the gating signal is as follows

1. Generate a saw tooth waveform of period T as the reference signal V_r and a dc carrier signal V_{cr}.

2. Compare these signals by a comparator to generate the difference $V_c - V_{cr}$ and then a hard limiter to obtain a square – wave gate pulse of width kT, which must be applied to the switching device through an isolating circuit. Any variation to V_{cr} varies linearly with the duty cycle k

5. PWM SIGNAL GENERATION AND SIMULATION RESULT

5.1 Sample Rate Calculation

Xillinx Spartan – 3E kit clock frequency is 50MHz. So, Time is T=1/FT=1/50MHz=0.02µs.This nanosecond time is not measurable. So, clock frequency will be divided to our requirements.

Design Frequency=50 KHz and Max. Count is FFF. This frequency and maximum count will be fixed and sampling time was varied.

Case(i) Sample rate=Design Frequency / Max.

Count

= 50KHz/ 4096

=12.2 HZ.

Case(ii) Sample rate=6.25MHz/4096

= 1.525KHz.

5.2 PWM output observer on a DSO

5.2.1 Duty cycle 25%

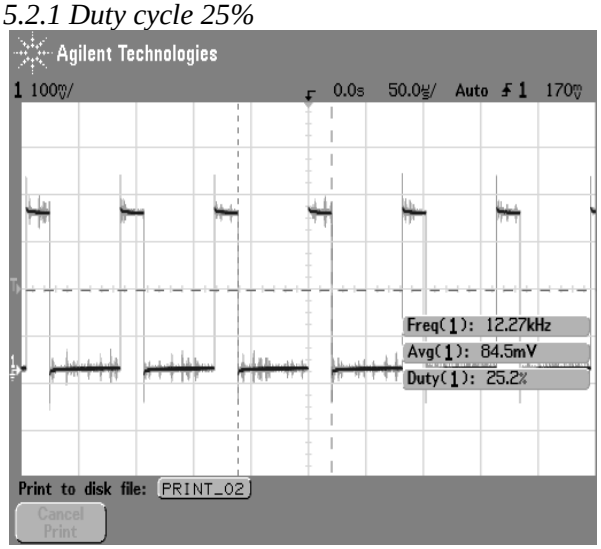

Fig 5.2.1 PWM output observer- 25% duty cycle

5.2.2 Duty cycle 50%

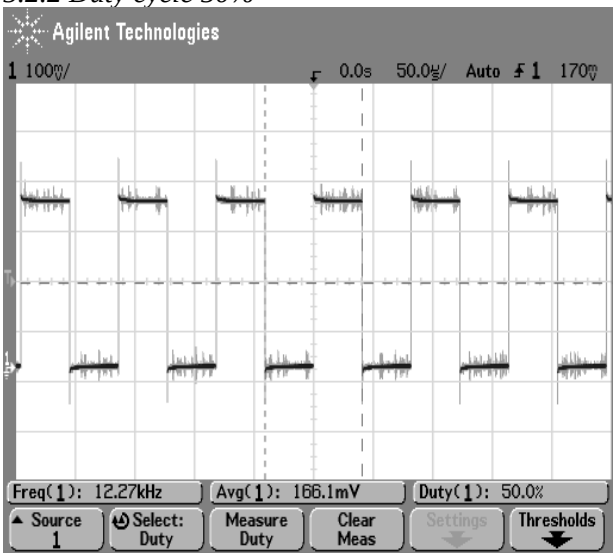

Fig 5.2.2 PWM output observer- 50% duty cycle

5.3 Buck mode (70% of duty cycle)

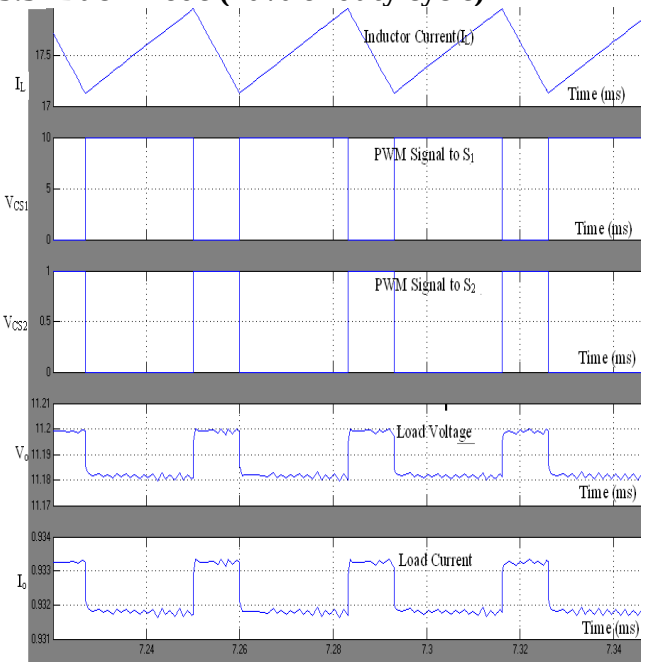

Figure 5.3 Buck Mode Waveforms

5.4 Boost mode (70% of duty cycle)

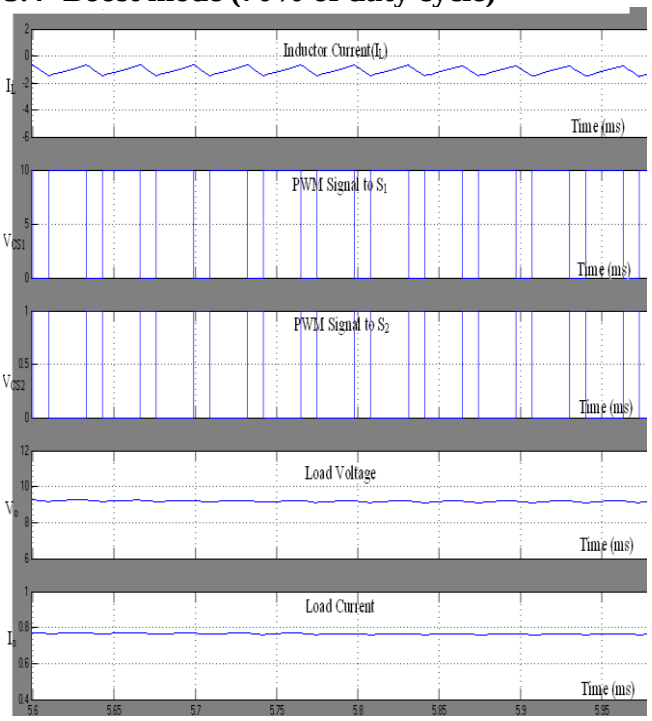

Fig 5.4 Boost Mode Waveforms

6. PROGRAM FOR INDUCTANCE CALCULATION IN BI-DIRECTIONAL CONVERTER

clear

clc

P=1000; %1 kW DC-DC converter

%% can be revised

```
fsw=100000; %switching frequency
Ilim=58; %58A

%set Vin,Vout for buck/boost converter
Vin=100;
Vout=50;
% Vinst=50;
% Voutst=80;
%%

 %For this bi-directional circuit it should always have
Vinst=Vout;
Voutst=Vin;

%the output current for buck/boost mode
Iout=P/Vout;
Ioutst=P/Voutst;
%Buck mode
Vinmin=80; %80V
Vinmax=100; %100V
Voutmin=25;
Voutmax=50;
%Boost mode
Vinminst=25;
Vinmaxst=50;
Voutminst=80;
Voutmaxst=100;

%Calculation of the duty cycles
Dbuck=Vout/Vinmax;
Dboost=1-Vinminst/Voutst;
% Dbuck=0.5;
% Dboost=0.5;

%calculate the inductance value
ripple=0.1;
Lbuck=Dbuck*(Vinmax-Vout)/(2*fsw*ripple*Iout);
Lboost=Dboost*(Vinst)*Vinst/(2*fsw*ripple*Ioutst*Voutst);
%Lbuck=Vout*(Vinmax-Vout)/(2*ripple*Iout*fsw*Vinmax);
%Lboost=(Vinminst^2)*(Voutst-
Vinminst)/(fsw*2*ripple*Ioutst*(Voutst^2));
L=max(Lbuck,Lboost);

%max switch current and max output current for buck/boost
mode
dImax=(Vinmax-Vout)*Dboost/fsw/L; %The maximum
ripple current throught the inductor
Iswmax=Iout+dImax/2;  %The max current going through the
switches
Imaxout=Ilim-dImax/2; %max deliverable current through
inductor by the converter
Rip=dImax/2/Imaxout;

dImaxst=Vinminst*Dboost/fsw/L;
Iswmaxst=dImaxst/2+Ioutst/(1-Dboost);
Imaxoutst=(Ilim-dImax/2)*(1-Dboost);
Ripst=dImaxst/2/Imaxoutst;
%output capacitor selection for buck/boost mode
dVoutripple=0.02*Vout;
Coutmin1=2*ripple*Imaxout/(8*fsw*dVoutripple);
Coutmin2=dImax/(8*fsw*dVoutripple);
Coutmin=max(Coutmin1,Coutmin2);
dVoutripplest=0.02*Voutst;
Coutminst=Imaxoutst*Dboost/(fsw*dVoutripplest);
%results
Lbuck
Lboost
L
Coutmin1
Coutmin2
Coutmin
Coutminst
Rip
Ripst
Lbuck =6.2500e-005
Lboost =9.3750e-005
L =9.3750e-005
Coutmin1 = 1.4000e-005
Coutmin2 =5.0000e-006
Coutmin =1.4000e-005
Coutminst =5.2500e-005
Rip =0.0357
Ripst =0.0714
```

7. CONCLUSION

Hence the above system is simulated using MATLAB/SIMULINK and coding is done for the calculating Inductance of Bi- directional buck boost converter .In this paper , the PWM is generated to switch the duty ratio 70% in synchronous converter and various operating modes are

verified in the converter. And PWM signal generated using XILINX FPGA has proven to be cost effective by varying the duty ratio of synchronous converter to 25% and 50% and the respective waveforms are evaluated using DSO.

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