

Design of a 4-bit 2's Complement Reversible Circuit for Arithmetic Logic Unit Applications

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ABSTRACT

Nowadays reversible circuit designing is the emerging area of research. This design strategy aims towards the formation of digital circuits with ideally zero power dissipation. In this paper we have proposed a new reversible logic module to design a 4-bit binary 2's complement circuit. This complement circuit using reversible logic can be used to design other low loss Arithmetic circuit. Proposed circuits have been simulated using ModelSim and implemented using Xilinx Spartan2 FPGA platform.

General Terms

2's complement calculator.

Keywords

Reversible logic circuit, Reversible gates.

1. INTRODUCTION

Conventionally digital circuits were designed using basic logic gates. These conventional basic logic gates dissipate some energy loss due to the information loss during the operation [1]. Irreversibility of energy is caused because the total number of output signals in the conventional gate is less than the number of total input signals. Reduced number of output signals is the major cause of the lowering of entropy of the overall digital system. The amount of energy loss for one bit of information loss in an irreversible gate was given by R. Landauer in 1961. Later in 1973 C. H. Bennette has shown that this energy loss can be minimized or even removed if the circuit is made up from the reversible logic gates [2].

Reversible circuit designing is gaining wide scope in the area of Quantum computing, Low power CMOS design, Nanotechnology, Optical computing, Signal processing, Advanced computing etc due to its ability to design low loss or approximately lossless digital circuits. Reversible logic concept is based on the formulation of the input states of the digital logic system by knowing its output states at any moment, whereas we can generate the output states from input in a conventional digital system.

Reversible logic approach converts any irreversible digital circuit in reversible circuit by replacing conventional logic gates with new reversible gates. This approach optimizes the circuit on the basis of total number of reversible gates used in the designing. The key issues of reversible circuit designing,

apart from fewer gates are the minimization of garbage output signals generated, quantum cost etc [3-6].

In this paper we have proposed reversible circuits for 2's complement calculator for a 4-bit binary number, which is designed using the combination of various reversible logic

gates. These designs are optimized on the basis of the total number of reversible gates used in the design, total number of garbage outputs and macro statistics etc. Later we have proposed a highly optimized circuit for 2's complement calculator using a single SSMT gate. SSMT gate is introduced in this paper. This gate can be used for the designing of various arithmetic and logical applications, but in this paper its application is limited to 2's complement calculator only.

The paper is organized in nine sections. First section gives the introduction of the proposed 2's complement calculator circuit using the reversible logic concept. Section two gives the brief introduction of the fundamental concepts of reversible logic. Next section introduces the proposed reversible gate i.e. SSMT gate. After that in section four conventional 2's complement calculator for 4-bit binary numbers is discussed. In section five designing of 4-bit 2's complement calculator circuit using reversible gates have been performed. Result and analysis of the proposed designs have been given in section six. Sections seven, eight and nine give the conclusion, acknowledgement and references of the paper respectively.

2. FUNDAMENTALS OF REVERSIBLE LOGIC

Reversible logic is a concept of digital circuit design which was born with the concept of creating digital logic circuits with zero power dissipation. It replaces irreversible logic gates with reversible gates in the conventional digital circuits. Some basic concepts of reversible logic are as follows:

2.1 Reversible Logic Gates:

Reversible gates are denoted as (n, n) digital logic gates, where (n, n) can be elaborated as (Total number of input signals, Total number of output signals). In reversible logic gates both the number of input signals and the number of output signals are equal. In these gates we can generate the input combinations at any instance by knowing the output combinations only. There exists a one to one mapping between the input and output signals i.e. a unique output combination occurs for individual input combinations. Generally reversible gates follow these norms-

[1] Total number of input signals = Total number of output signals.

[2] One to one mapping between input and output variables.

[3] No feedback.

[4] Individual output bits are high for a total of half the number of total input combinations.

Figure 1 below shows the block diagram of a typical (n, n) reversible logic gate.

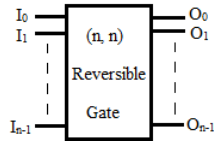


Figure 1: Block diagram of (n, n) Reversible logic gate

Input variables of this (n, n) reversible logic gate are denoted by $(I_0, I_1, \dots, I_{n-1})$ and output variables by $(O_0, O_1, \dots, O_{n-1})$. Till now various researchers have achieved remarkable success in the area of reversible logic. There are various types of reversible logic gates used in the reversible circuits designing [7-13].

2.2 Reversible Circuit Designing:

In reversible circuit designing, conventional irreversible circuits are planned with the help of reversible logic gates (described in section 2.1). Here, the aimed reversible circuit must have following characteristics:

- [a] Minimum number of Total Reversible Gates used in the circuit design.
- [b] Minimum (Ideally zero) Garbage Outputs.
- [c] Minimum (Ideally zero) delay.
- [d] Zero Fan-out.
- [e] No Feedback.

To obtain an ideal circuit is practically very tough [6, 7], so an optimized reversible circuit of an irreversible digital logic circuit has been tried to be attained by the researchers. In this optimized reversible circuit, apart from minimum number of total reversible gates used, minimum possible garbage outputs and delay are being achieved.

3. PROPOSED REVERSIBLE LOGIC GATE

Here we propose a new (4, 4) reversible logic gates, called as SSMT gate. By knowing the status of output conditions at any instance we can formulate the input combinations. SSMT gate has following characteristics:

- [a] Four input signals and four output signals, so equal number of input and output signals.
- [b] One to one mapping between input and output variables.
- [c] Individual output variable is high for a total of 8 combinations i.e. half of the total input combinations.

The block diagram of SSMT gate is shown below in the figure 2.

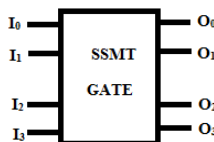


Figure 2: Block diagram of SSMT gate

As shown above in the figure, the four input signals named as I_0, I_1, I_2, I_3 , whereas four output signals as O_0, O_1, O_2, O_3 in the SSMT gate. The output equations are given as:

$$O_0 = I_0$$

$$O_1 = I_1 \cdot (I_0 + \bar{I}_2 \cdot \bar{I}_3) \oplus I_0 \cdot \bar{I}_1 \cdot (I_3 + I_2)$$

$$O_2 = I_2 \cdot \bar{I}_3 \oplus I_2 \cdot \bar{I}_0 \oplus I_0 \cdot \bar{I}_2 \cdot I_3$$

$$O_3 = I_3$$

By using above output signal equations we can derive the truth table of the SSMT gate as shown in the table 1 below.

Table 1: Truth table of SSMT gate

S. No.	Input Combinations				Output Combinations			
	I_0	I_1	I_2	I_3	O_0	O_1	O_2	O_3
1	0	0	0	0	0	0	0	0
2	0	0	0	1	0	0	0	1
3	0	0	1	0	0	0	1	0
4	0	0	1	1	0	0	1	1
5	0	1	0	0	0	1	0	0
6	0	1	0	1	0	1	0	1
7	0	1	1	0	0	1	1	0
8	0	1	1	1	0	1	1	1
9	1	0	0	0	1	0	0	0
10	1	0	0	1	1	1	1	1
11	1	0	1	0	1	1	1	0
12	1	0	1	1	1	1	0	1
13	1	1	0	0	1	1	0	0
14	1	1	0	1	1	0	1	1
15	1	1	1	0	1	0	1	0
16	1	1	1	1	1	0	0	1

We can observe from the above table that there exist unique output combinations for each and every input combination. This SSMT reversible gate can be used to design various digital circuits using reversible logic. But here in this paper the use of the SSMT gate is limited to design a 4-bit binary 2's complement calculator circuit.

4. IRREVERSIBLE 4-BIT BINARY 2'S COMPLEMENT CIRCUIT

There are two ways to represent a negative binary number in the digital systems [14]. These are as follows-

[a] Signed Binary Negative Number

[b] Unsigned Binary Negative Number

In signed binary negative number, the most significant bit (MSB) is used to represent the sign of the number. For negative binary number MSB is set to 1 otherwise 0 for positive binary number.

In the concept of unsigned binary negative number there are two techniques for the representation-

[a] 1's Complement Method

[b] 2's Complement Method

In 1's complement method each and every bit of the binary number is interchanged by its complement bit i.e. 0 by 1 and 1 by 0. In the 2's complement method, binary 1 is added to the 1's complement of the respective binary number. 2's complement method is considered better for arithmetic operations as compared to 1's complement method due to the following reasons-

[1] For subtraction with complements, 2's complement requires only one addition operation, whereas 1's complement requires two addition operations if there is an end carry.

[2] 1's complement has two arithmetic zeros, all 0s and all 1s.

So due to above reasons 2's complement is preferred in the calculations generally. From the table of 2's complement calculator we can convert a 4-bit binary number denoted as (A, B, C, D) we can find the complement given by (P, Q, R, S). After that we calculate the equations for P, Q, R and S using K-map and final equations are as follows-

$$P = A$$

$$Q = B \cdot (A + \bar{C} \cdot \bar{D}) + A \cdot \bar{B} \cdot (D + C)$$

$$R = C \cdot \bar{D} + \bar{A} \cdot C + A \cdot \bar{C} \cdot D$$

$$S = D$$

This K-map simplification can be used to design the circuit for 2's complement for 4-bit binary number in any subtraction application.

5. REVERSIBLE CIRCUIT FOR 2'S COMPLEMENT CALCULATION OF 4-BIT BINARY NUMBERS

In literature, many combinations of reversible gates and approaches are available to design a combinational circuit using reversible logic [15-17]. In the designing of reversible 2's complement calculator circuit we have used combinations of Feynman, Toffoli, Fredkin, URG, TR BVF and SSMT gates. In the present paper we propose three designs for 2's complement calculator to achieve the optimized reversible circuit. These three designs have been simulated using ModelSim. The performance of the circuits is analyzed on the basis of total gates, garbage outputs and macro statistics.

Proposed design approaches have been presented in proceeding subsections.

A. Design 1:

In this design Feynman gate which is a (2, 2) reversible gate and Toffoli, TR and Fredkin gates which are (3,3) reversible gates have been used. Feynman, TR and Fredkin gates are used at input stage and outputs are derived from the same combination of reversible gates i.e. Feynman, TR and Fredkin gates. The block diagram of this design is shown in the figure 3. Here 11 reversible gates have been used in various configurations and number of garbage output signals generated are 13.

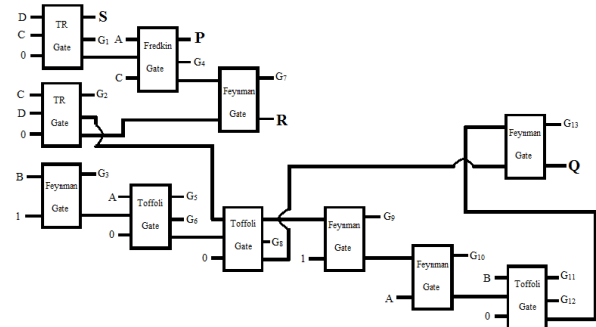


Figure 3: Design 1 of 2's complement calculator of a 4-bit binary number

B. Design 2:

As shown in figure 4, in this design Feynman gate, a (2, 2) reversible gate and a combination of (3, 3) reversible gates i.e. TR, URG, Fredkin and Toffoli gates are used. In this design a (4, 4) reversible gate called BVF gate is also used. In this proposed design TR and URG gates are used at the input stage and the outputs are derived from URG, Feynman and BVF gates. In this design total number of reversible gates used is 10 and garbage outputs generated is 14.

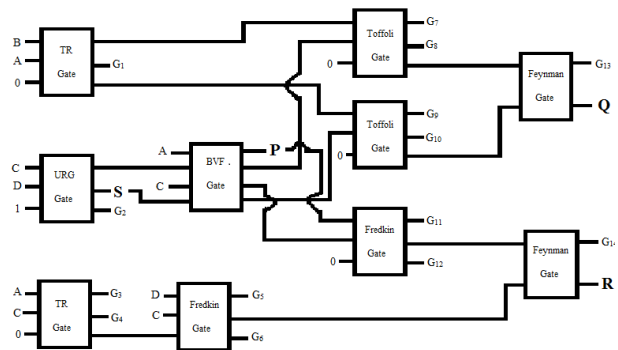


Figure 4: Design 2 of 2's complement calculator of a 4-bit binary number

The 2's complement calculator circuit using reversible logic can be further optimized with respect to configuration and gates so that number of total gates used and garbage outputs can be minimized. So, moving towards the top of the optimization hierarchy, we propose a better design of the same circuit using SSMT gate in terms of various leading parameters.

C. Design 3:

The most optimized circuit for a reversible 4-bit 2's complement calculator circuit is shown in the figure 5 below.

This design uses a single SSMT gate. Four inputs of the SSMT gate is connected to the A, B, C and D bits respectively of the corresponding 4-bit binary number and output to the P, Q, R and S.

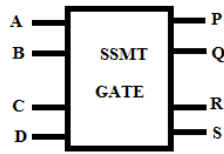


Figure 5: Design 3 of 2's complement calculator of a 4-bit binary number

Here all the four outputs of the SSMT gate are utilized as the 2's complement of the applied 4-bit binary number. There is no garbage output generated in the circuit. Here only one reversible gate is used to design the 2's complement circuit.

6. RESULT & ANALYSIS

The various proposed designs of the reversible 4-bit binary 2's complement calculator circuit have been analysed on the basis of performance parameters as shown in figure 6.

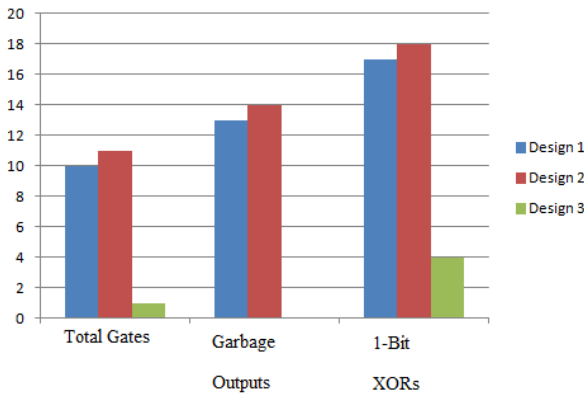


Figure 6: Comparison Chart

The above comparison chart shows the clear variations among all three designs. From above analysis we can conclude that design 3 is the most optimized configuration in terms of number of total reversible gates used, number of garbage outputs generated, 1-bit XORs created and CPU usage as compared to other two designs. This design has been simulated using ModelSim simulator. Structural modelling has been used for programming. Figure 7 shows the simulated waveform for each and every input and output signals of the optimized reversible circuit of 2's complement calculator of 4-bit binary numbers.

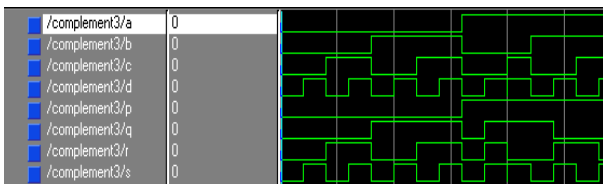


Figure 7: Simulated Waveform

The optimized design is synthesized using Xilinx ISE 6.1i and implemented using Xilinx Spartan 2 FPGA platform.

7. CONCLUSION

Reversible logic is becoming the modern way of digital logic circuit designing. Here in this paper we have attained a highly

optimized four-bit reversible 2's complement calculator circuit by using various combinations of the basic reversible gates and a new reversible gate proposed in the paper. The base of optimization is total reversible gates used and garbage outputs generated. Optimized 2's complement calculator circuit (shown in figure 5) has been designed using a single reversible gate and have zero unused outputs generated. This design can be employed in low power logical design applications.

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