# Implementation of 8-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)

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## ABSTRACT
A SAR ADC is presented in this paper with low power consumption. In this paper an asynchronous SAR logic is used which will reduce its power consumption as MSB bit evaluation and each bit evaluation time is different, due to which it provide high resolution for same power consumption. A dynamic comparator is used. It doesn't consume any static power which will reduce its power consumption. Vcm- based switching technique reduces its power as it maintains the common mode voltage. In this paper different block of a SAR ADC with their schematics and wave-forms is presented. This work is done by using Synopsys Galaxy Custom Designer Tool using 90nm CMOS technology in which power consumption by DAC is 33uW, Comparator consumes 43uW, SAR Logic consumes 55uW with frequency range 100MHz.

## Keywords
SAR, Lower and Upper DAC, Sample and Hold Circuit, Bootstrapped switch.

## 1. INTRODUCTION
In the past few years, advancement in technology scaling, there has been developing enthusiasm for reducing the power consumption of any device. Many devices use a battery for the power. Battery life of any device is fixed and at the end we have to replace the battery and it increases the cost of any device. To solve the problem of replacement of battery solar cells comes into existence. Solar cell produces very low power and low voltage, so ultra-low-voltage sensors come into role. Sensors sense these low power signals. Many sensors are available in market and these sensors are used in various applications like bio-medical devices, communication devices and temperature sensing devices [1][2].

Sensor uses ADC's (analog-to-digital converter) to process the signals. As we know in real world signals are analog in nature and it is very difficult to analyze an analog signal. ADC converts the analog signal into digital signal by providing an interface between analog circuits and digital circuits.

Many ADC's are available in the market like FLASH ADC, Δ-∑ (Delta-Sigma) ADC, DUAL-SLOPE ADC, and SAR (Successive approximation register) ADC. Each ADC is used in different applications according to the requirement of different parameters like power consumption, resolution, accuracy, speed, area, cost etc.

A medium resolution with high accuracy and low power consumption SAR ADC is used as it consumes dynamic power only. Control utilization in SAR ADC is for the most part due to Comparator, DAC (digital-to-analog converter) and control circuitry. A lot of power consumption reduction techniques are developed like split-capacitor reduction technique, data- driven-noise reduction technique, oversampling switching technique and Vcm- based switching techniques.[3] Many architecture is also developed to reduce the power consumption, high speed and low area like FLASH-SAR ADC, Hybrid ADC, and Pipelined ADC etc.

Comparator and DAC consumes more power as comparator IRN (Input-referred Noise) is inversely proportional to power and DAC capacitance increase exponentially with the resolution, it will increase the power consumption. In this work, we are developing a 8-bit SAR ADC. ADC comprises a double-bootstrapped sample, hold circuit, DAC, comparator and SAR logic. In this paper, Vcm- Based switching technique has been used to reduce the power consumption as it maintains the common mode voltage. [3]

This paper is organized in IV sections. Section I gives the thought regarding the introduction of ADC. Section II gives the thought regarding the proposed work which includes the Design- engineering of ADC. Section III portrays the execution of the design and about the various parts of ADC Section IV discusses the work result and section IV summarizes the work in the form of conclusion and future scope.

## 2. PROPOSED WORK
### 2.1 SAR ADC Architecture
The SAR ADC comprises of DAC inherit with bootstrapped-sample and hold circuit, a comparator and a SAR logic. The whole operation of analog to digital conversion will be in three phases. First phase is sampling phase, 2nd phase is comparison phase and third phase is conversion phase. In SAR ADC binary search algorithm is used to perform the analog to digital conversion process. Framework of SAR ADC is shown in Fig.1.The basic principle of SAR ADC is that analog input and is applied to the bootstrapped switch circuit which is inherent in the DAC as it reduces the area and power consumption. For binary search algorithm N-bit shift cells and N-bit TSPC DFF is used in SAR logic block. During the operation the shift-cells are set to mid-scale value. i.e. (b10000…). Here 1 is set at the MSB bit which will force the DAC output equals to $1/2\,V_{ref}$.Now the comparison of input voltage and DAC output voltage has been made. If comparator gives the output as 1 then the MSB bit remain at 1 and for next bit comparison will be made. i.e. $V_{in} > V_{ref}$, comparator gives the output as 1 and MSB bit remain at 1 and for next bit comparison has been made. If$V_{in} < V_{ref}$, the MSB bit is set to 0 and SAR logic moves to next bit down and further comparison has been made. In this comparison, $DAC_n$ and $DAC_p$ has been used as the inputs of the comparator. The decisions were made on the basis of $(V_{ip} - V_{in} > V_{cm})$ or $(V_{ip} - V_{in} < V_{cm})$.The SAR logic will be set according to the comparison made between the mentioned parameters.

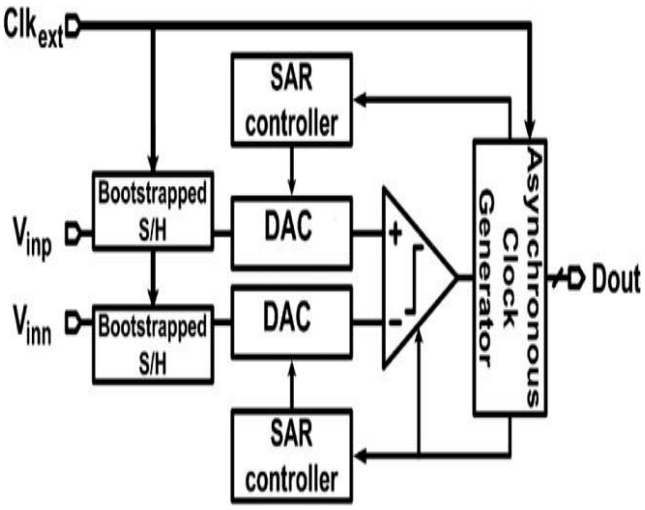


**Fig. 1: SAR Architecture.**

After the whole evaluation process, a complete N-bit digital output will be saved in N-bit TSPC DFF. Here the architecture is for 8-bit ADC which will give a 8-bit digital binary output at the end.

# 3. IMPLEMENTATION

## 3.1. Sample and Hold Circuit Switch

An essential sample- hold circuit comprises of a switch and a capacitor. In this design, the MOSFET is utilized as a switch whose source, drain will go about as as the terminals of the switch and gate will act as a control terminal. In MOSFET, the conductivity between source and drain depends upon the terminal potentials as compared to channel potential. On-resistance of a MOSFET is given by equation (1):

$$R_{ON} \approx \frac{1}{g_{ds}} = \frac{1}{u*Cox\frac{W}{L}(Vgs-Vth)}, V_{gs} \geq V_{th} \qquad (1)$$

Where $R_{ON}$ is the ON resistance, $g_{ds}$ is the conductance, is electron mobility in the channel, $C_{ox}$ is the oxide capacitance, W and L is width and length of transistor individually, $V_{gs}$ is the gate-source voltage and $V_{th}$ is the threshold voltage [4].

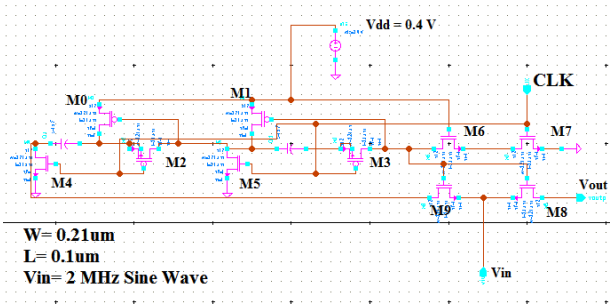


**Fig. 2: Sample and Hold circuit switch.**

Bootstrap concept is used with the sample & hold circuit as it reduces the problem of poor conduction with variation in ON resistance. The principle of bootstrap concept is that a single transistor is used as pass transistor and other transistor are used to generate the $V_g$ for the pass transistor. When clock is low, i.e. clock is 0, the transistor will be in cut-off region and $V_g$ is equals to zero and the capacitors is pre-charged to $V_{dd}$.

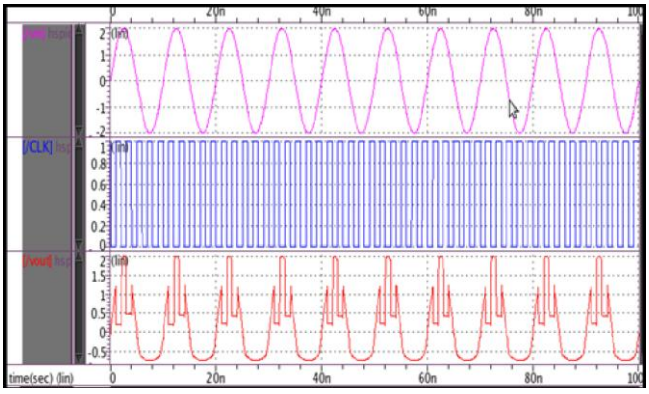


**Fig. 3: Waveform of Sample and hold circuit switch.**

When clock is high M2 and M3 is off and M4, M5, M0, M1, M7 and M8, M9 is ON, as M9 is ON and gate voltage will be $2V_{dd}$. The output of bootstrapped sample-hold circuit and its Waveform is shown in fig. 2 and fig. 3 respectively.

## 3.2. Comparator

Comparator is a 1-bit ADC utilized as a part of the vast majority of the ADC. In the transformation procedure the input signal is sampled and then the signal is encouraged to the terminals of the comparator and the signal will be compared with the other signal given at the other terminal. The basic operation of a dynamic comparator is shown in fig. 4[5].

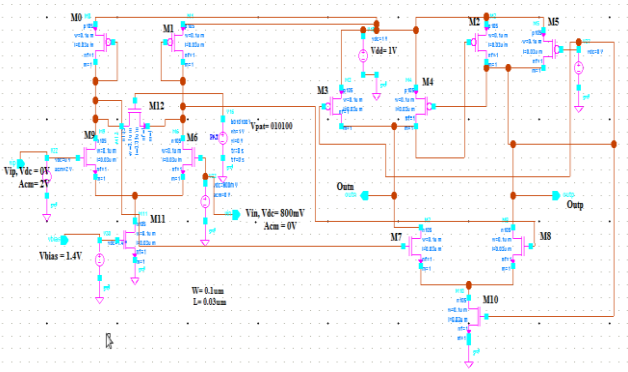


**Fig. 4: Dynamic comparator.**

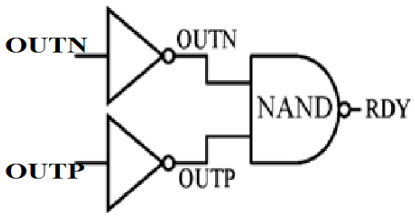


**Fig. 5: Ready signal fed to SAR logic [6]**

When clock signal is low, i.e. during the reset phase, M-tail (M-t) transistor is OFF, it will on the M12 and M7 transistors and pull both outputs $Out_n$ and $Out_p$ to $V_{dd}$. When clock signal is high, i.e. during comparison phase, M-t is ON and M7 and M12 are OFF. $Out_p$ and $Out_n$ will be pre-charged to $V_{dd}$ and it will starts to discharge at different speeds depending upon the values of input voltages $V_{in}$ and $V_{ip}$. If $V_{ip} > V_{in}$, $Out_p$ discharges fast than the $Out_n$, when $Out_p$ falls down the $(V_{dd} - V_{tp})$

before$Out_n$, the M6 will be ON and it starts the latch regeneration which is due to back to back inverter (M6, M8 & M4, M1).

**Fig. 6: Waveform of dynamic comparator.**

Hence $Out_n$ pulls to $V_{dd}$ and $Out_p$ releases to ground. In the event that ($V_{inp} < V_{inn}$), the circuit works the other way around. Ready signal is fed to SAR logic which will give signal to SAR logic for starting of the operation. [6].The output and schematic of comparator is shown in fig. 4 and fig. 6.

## 3.3. DAC

In this architecture, Capacitive DAC is used having binary-weighted values and it inherits the sample and hold circuit within the circuit as shown in fig. 6. No extra sample and hold circuit is required as in resistive DAC. A capacitive DAC is an array of N capacitors having binary weighted values. An extra capacitor is used in the DAC i.e $C_{LSB}$ to make the total capacitance value equals to $2^N C$ and it makes the calculations and manipulations easy.[8] The design of DAC and its waveform is shown in fig. 7 and fig. 8 respectively.

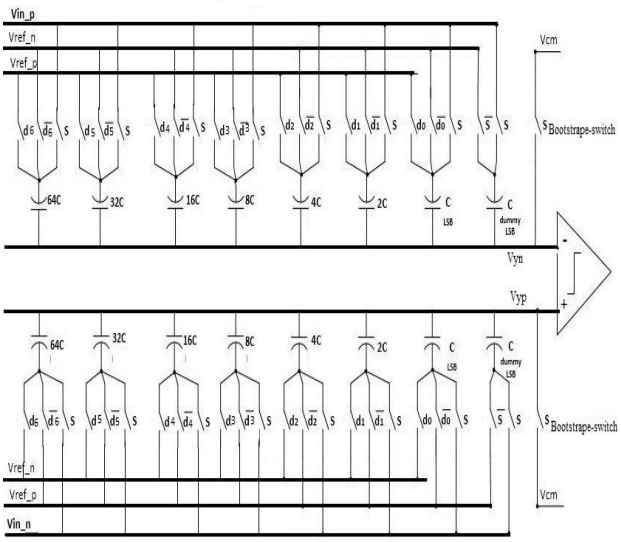


**Fig. 7: Schematic diagram of DAC with sample and hold circuit.**

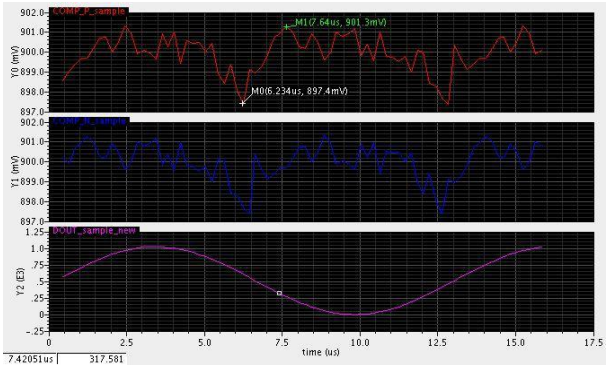

**Fig. 8: Waveform of DAC.**

In SAR ADC, DAC consumes more power as compared to other components used in SAR ADC. Numerous techniques have been proposed to decrease the DAC power consumption. In this work, $V_{cm}$-based switching technique is utilized because it diminishes 75% power consumption. The energy consumption in DAC is during the evaluation of MSB bit. Switch S, the bootstrapped-switch is utilized to sample the analog signal, during the sampling process, bottom plates of the capacitor array is associated with $V_{in}$ and top plates are associated with $V_{cm}$. After sampling the top plate switch S will be open and total charge at the node is $V_y$.Let's take an example for 3-bit calculation.

$$V_{refp} = V_{cm} + V_{ref}/2, V_{refp} = V_{dd}$$

$$V_{refn} = V_{cm} - V_{ref}/2, V_{refn} = 0$$

$$Q_{sp} = (V_{cm} - V_{in}) * C_{Total}$$

$$Q_{sp} = (V_{cm} - V_{in}) * 8C$$

$$Q_{sn} = (V_{cm} - V_{ip}) * C_{Total}$$

$$Q_{sn} = (V_{cm} - V_{ip}) * 8C$$

For MSB evaluation (bit 1): switches are set to (1,0,0)

$$Q_{p100} = (V_{yp} - V_{dd}) * 4C + V_{yp} * 4C$$

$$Q_{n100} = (V_{yn} - V_{dd}) * 4C + V_{yn} * 4C$$

$$V_{yp} = -V_{in} + \frac{1}{2}V_{dd} + V_{cm}$$

$$V_{yn} = -V_{ip} + \frac{1}{2}V_{dd} + V_{cm}$$

If $V_{yn} < V_{yp}$, $(V_{ip} - V_{in})$>0, the comparator output is equal to 1 and d2 is set to 1 and if$V_{yn} > V_{yp}$, $(V_{ip} - V_{in})$ <0, the comparator output is equal to 0 and d2 is set to 0. After this evaluation the bottom plates of MSB capacitor is set to $V_{ref}$ and ground in upper DAC and lower DAC respectively. For bit 2 evaluation the following methods has been followed:

$$Q_{p110} = (V_{yp} - V_{dd}) * 2C + V_{yp} * 6C$$

$$V_{n110} = (V_{yn} - V_{dd}) * 6C + V_{yn} * 2C$$

$$V_{yp} = -V_{in} + \frac{1}{4}V_{dd} + V_{cm}$$

$$V_{yn} = -V_{in} + \frac{3}{4}V_{dd} + V_{cm}$$

If $V_{yn} < V_{yp}$, $(V_{ip} - V_{in}) > \frac{1}{2}V_{dd}$, the comparator output is equal to 1 and d1 is set to 1 and If $V_{yn} > V_{yp}$, $(V_{ip} - V_{in}) < \frac{1}{2}V_{dd}$, the

comparator output is equal to 0 and d1 is set to 0, similarly for bit 3evaluation, it is assumed that bit 3 is evaluated as 0. If $V_{yn} < V_{yp}$, $(V_{ip} - V_{in})$>-$\frac{1}{2}V_{dd}$, the comparator is set to 1 and d1 is set to 1 and if $V_{yn} > V_{yp}$, $(V_{ip} - V_{in})$< -$\frac{1}{2}V_{dd}$, the comparator output is set to 0 and d1 is set 0. The binary search algorithm continues till the LSB is evaluated. When all the bits are evaluated the top plate capacitor array potential is very close to Vcm.

## 3.4. SAR Logic

SAR logic consists of shift-cells known as sequencer used to generate sequential signals and TSPC (True single-phase clock). D-FF known as code register used to generate the comparison results of each bit cycle. SAR ADC follows the 3-step state machine during the evaluation of each bit. It starts by setting a bit in the DAC. After setting the DAC bit comparison is made. After comparison the final value which has to be stored in code-register is finalized. SAR logic is of two types: synchronous SAR logic and Asynchronous SAR logic. In synchronous SAR logic all these three steps are performed for each bit in succession using N clock cycles using over-sampled clock. In asynchronous SAR logic self-synchronization is used to perform these steps.

In Concurrent SAR logic time required to evaluate MSB bit is equal to time required to evaluate each bit approximately. In non-concurrent SAR logic a substantial signal (valid) is produced by the comparator after completion of each comparison. Time of assessment of each bit is different, so total time for the conversion is less as compare to concurrent SAR logic; it makes the increase in sampling rate for same resolution, increases the speed and consumes less power.[9][10]

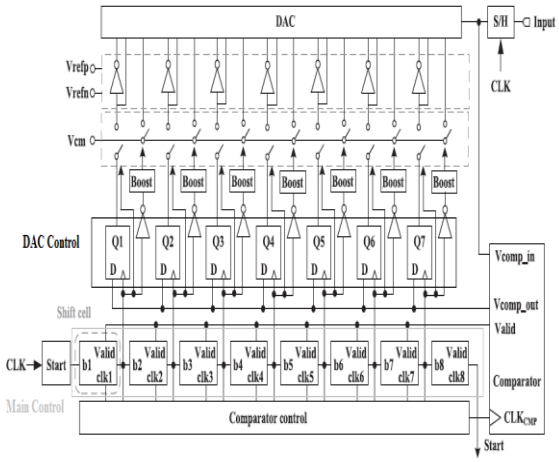


**Fig. 9: SAR logic.**

In this architecture SAR logic made of two parts; main control and DAC control. Main control composes of shift-cells and DAC control composes of TSPC D-FF. Main control controls the timing of all the bit comparison in conversion cycle & DAC control generates the N-bit conversion results. The architecture of SAR logic and full ADC schematic is shown in fig. 9 and fig. 10 respectively.

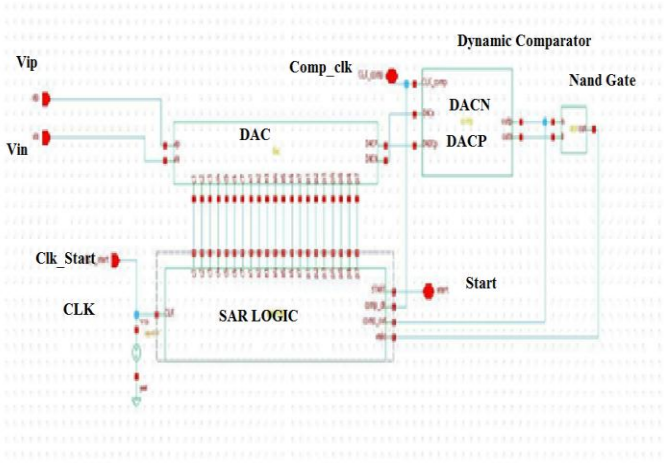


**Fig. 10: Full ADC architecture.**

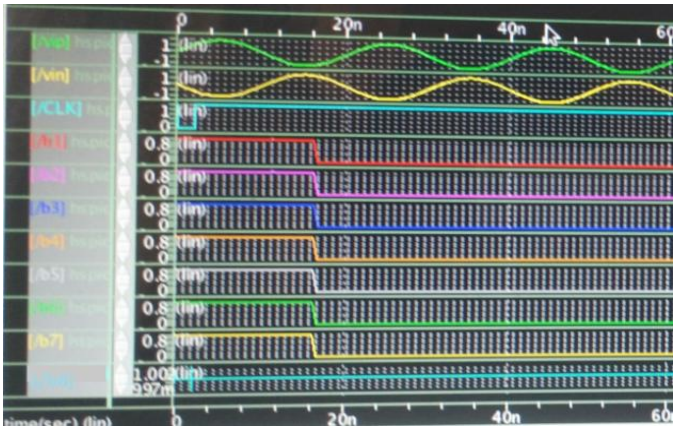

**Fig. 11: Waveform of SAR Logic**

## 4. RESULTS

This Work presents a asynchronous SAR ADC implemented on 90nm CMOS technology using Synopsys Galaxy custom designer tool. As synchronous based SAR ADC have large evaluation time for bits as compare to asynchronous based SAR ADC which is discussed in the fig.12. Power consumption by different blocks is shown in the Table1.

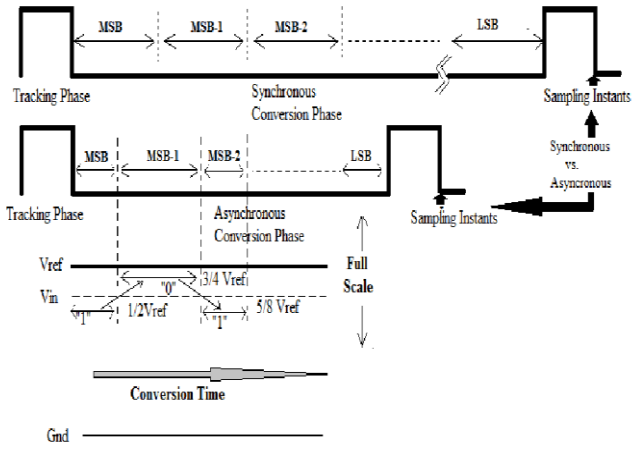


**Fig. 12: Synchronous vs. Asynchronous SAR conversion. [10].**

**Table 1: power consumption by different components**

| Components | Power Consumption |
|---|---|
| DAC | 33uW |
| Dynamic Comparator | 43uW |
| SAR logic | 55uW |

## 5. CONCLUSION & FUTURE SCOPE

The primary focus for this research is on the implementation of a low power 8-bit SAR ADC. To achieve the goals set for the research, various components of SAR ADC has been modified. In this architecture a dynamic comparator is used, if we replace that comparator with double-tail- comparator it may reduce the power consumption

In this research Capacitive DAC, Double bootstrapped sample and hold circuit and Asynchronous SAR control logic contributes in reduction of total power consumption is also reduced.

As the proposed ADC have proven to work efficiently in terms of power consumption, the more effective results are expected to be obtained while incorporating this ADC with other complex systems like sensors and other Bio-Medical applications in the field of low power VLSI design.

## 6. ACKNOWLEDGMENT

This work has been achieved on Synospsys Galaxy custom designer tool in the provision of Electronics Department of Chandigarh University, Gharuan- Mohali (Punjab).

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