Design and Analysis of Faster Multiplier using Vedic Mathematics Technique

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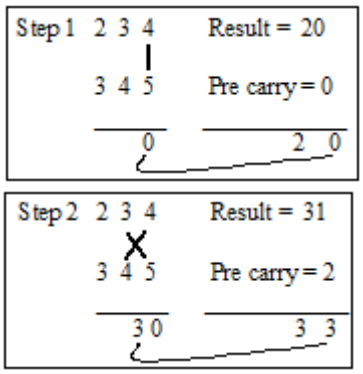
ABSTRACT
In the modern era, as the circuit density is increasing thereby, its complexity is also increasing dramatically. Therefore it effect the processing speed, arithmetic and logical operations of the processor. Hence proposed design of the 8 bits Vedic multiplier which simplify the arithmetical operations compares to conventional multiplier. Moreover, it takes the minimum access time to execute mathematical operation. The proposed multiplier is design by use of Ripple carry adder by using Wallace tree methods. The proposed design is coded in Verilog in Xilinx 14.7 tool and analysis is done using RTL schematics. The proposed design takes less area and access time as compared to conventional multipliers because the number of gates is reduced to perform any operation compared to other multipliers.Moreover, proposed algorithm is simple and faster as compared to other multiplier.

Keywords
Vedic Multiplier, Urdhav Tribhayam, Sutra, Ripple Carry adder

1. INTRODUCTION
Arithmetic is the oldest and most elementary topic of mathematics. The arithmetic is being using day by day from its simple calculation to the advance science and business calculation. If talking about the engineering world, then multiplication based operation is the frequently used functions. Its currently implemented in the field of digital signal processing (DSP) such as convolution operations Fast Fourier Transform, filtering and ALU operations [8]. Since Multiplications dominating functions, so there is a need of high speed and low power multiplier using Vedic Mathematics technique [2].

2. VEDIC MATHEMATICS SUTRA
Vedic mathematics is the mathematical elaboration of the sixteen simple Mathematical formula and thirteen sub-formula taken from Vedas as bought out by Sri Bharti Krishna Tirthaji in the year of 1884-1960. Vedic mathematics is the part of four Vedas in which it is the part of Sthapatya- Veda (book on Civil engineering and Architecture) which is the supplement of the Atharva Veda [3]. It includes the efficient modern mathematical terms including Arithmetic, Trigonometry, geometry, quadratic equations and Calculus. It reduces the complex calculation into the simpler one because it is based on the method of simple working of human mind thereby making them easier. The Algorithm of proposed Vedic multiplier is based on the Vedic multiplications sutras. These sutra is traditionally used for the multiplications of the two number in the decimal number system [7]. In this work same techniques were applied for the binary numbers, to make the proposed design algorithm is simple with hardware system [1]. In this technique the Urdhav Tribhayam method is used for the multiplications Process.

2.1 Urdhav Tribhayam sutra
Urdhav Tribhayam Sutra- This design multiplier is based on the algorithm of Urdhav Tribhayam sutra taken from all the sixteen sutra of ancient times. This technique is used in all cases of multiplications. Its literally means "Vertically and crosswise". It is based on the novel concept in which the concept of partial product has done and after that the concurrent addition of these partial product can done, so by this way the parallelism in the generation of partial product can be obtained by using Urdhav Tribhayam. This algorithm can be generally realized by n x n bits. The proposed multiplier is independent of the clock frequency of the processor. These multiplier enhance the speed of the computation because all the partial product and the addition operation has been done parallely. Thus, for high speed multiplication with their partial sum a special adder is used. The 8x8 bit multiplier is design using structure style of modeling in Verilog Languages. This proposed technique clearly understand the concept of the Urdhav Tribhayam sutra and its processing is done by using the decimal number. Lets considered two decimal number 234 and 345. Multiplications of these two numbers are explained below step by step as shown in figure 1. The first step is the two number shown in line are multiplied, the output is generated. One's place of this generated output has stored as one's place of final result and ten's place of the generated output has taken as pre carry for the next step. In this way the process goes on. Wherever, there is more than one digit to multiply then multiply digits shown with lines and add all those generated products. Output of this summation is again stored in final result with forwarding pre carry to the next steps as it be explained earlier. This way process continues and got the final result of multiplication of two number (234 X 345).



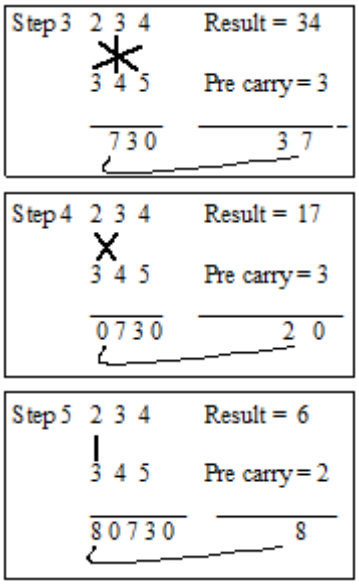


Fig 1: Result of 234 x 345 =8 0 7 3 0.

3. ARCHITECTURE AND IMPLEMENTATION OF THE VEDIC MULTIPLIER

In this section the architecture of the Vedic multiplier design are discuss. For the n x n bits the multiplier is designed which is operated for the binary data. In the design module firstly design the Adder (half adder and full adder) circuit, then 2x2 Vedic multiplier circuit is implemented. This 2 x 2 design Vedic multiplier block can be used in the implementation of 4 x 4 Vedic multiplier architecture. The implementation of 2 x 2, 4 x 4 and 8 x 8 Vedic multiplier architectures explained in detail in this section.

3.1 2x2 Vedic Multiplier Block

In this block the perfect use of the Urdhav Tribhayam technique is used for the implementation of the 2x2 Vedic multiplier. For simple 1 bit binary multiplication the AND gate is used. Considered the 2 inputs value A and B having A_1A_0 and B_1B_0 respectively. Where A_0 and B_0 are the LSB (least significant bits). A_0 and B_0 are multiplied vertically and stored in the LSB of the Product output register. Next step is to multiply LSB of number A with MSB of number B that is (A_0 x B_1) and MSB of number A with LSB of number B that is (A_1 x B_0) as shown in Figure 1. Thus two AND gates are required for this multiplication. These generated product are added that is (A_0 x B_1) + (A_1 x B_0) using half adder (HA0). This summation generates output of 2 bits. LSB of this generated output is stored as second bit of final result and MSB of this generated output is stored as pre carry for next step. Last step is to multiply MSB of A with MSB of B that is (A_1 x B_1). One AND gate is required for this multiplication. This generated product is added with pre carry of previous step. Thus again one more half adder is required for it. This half adder (HA1) generates 2 bits output which is taken as 3rd and 4th bit of final result. A_1 bit wire carry is defined. The result of the multiplication is store in the 4 bit register named as Prod i.e. Prod(3:0).

Prod(0) = A_0 B_0

Prod(1) = A_0 B_1 + A_1 B_0

Prod(2) = A_1 B_1 + carry(prod(1))

Prod(3) = carry(prod(2))

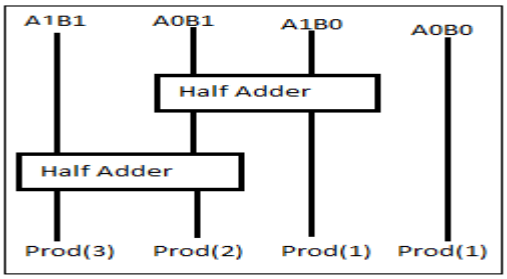


Fig 2: 2x2 bit Vedic Multiplier.

3.2 4x4 Bit Vedic Multiplier Using Ripple Carry Adder

In this section 4 bit multiplier is designed having input A(3:0) and B(3:0). The design is implemented using 2x2 Vedic multiplier. Here the design of the one 4 bit and two 6 bit ripple carry adder for fast addition. In ripple Carry adder the carry out of the each full adder is the carry in of the next most significant full adder. The Same procedure is follow here as 2 x 2 Vedic Multiplication procedure discussed earlier. Initially pre carry is set to zero. In each and every step generated carry is forward to the next step and process is going on. Finally the result generated and it is stored in the output 8 bits register named as Prod (7:0).

3.3 8x8 Bit Vedic Multiplier

In the implementation of the 8 bit Vedic multiplier in same way two inputs A(7:0) and B(7:0) are considered. 8 x 8 Vedic multiplication process will follow same as that of 4 x 4 Vedic multiplier discussed in the previous section. Here the design of the 8 and 12 bit ripple carry adder is explained. Pre carry at first step is set to zero. In every step generated carry is forwarded to next step for addition and process is continues. The result is stored in the 16 bit register Prod (15:0). The 8 x 8 multiplier is designed using 4 x 4 multiplier and one 8 bit Ripple carry Adder and two 12 bit Ripple carry adder. The arrangement of the carry adders is made in different way such that it requires less computation time. The simple architecture design of the Ripple carry Adders are shown in figure 3 having n number of I/Os.

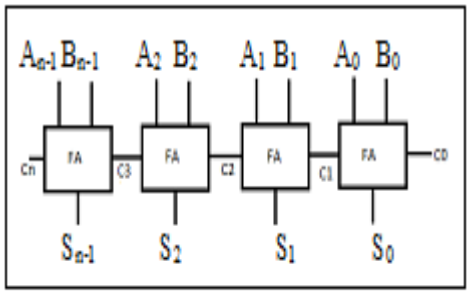


Fig 3: Architecture of Ripple Carry select Adder.

The logic diagram of 8 bits binary number multiplication for Urdhav Tribhayam technique that used in our 8 bit Vedic multiplier are shown in the fig 4.

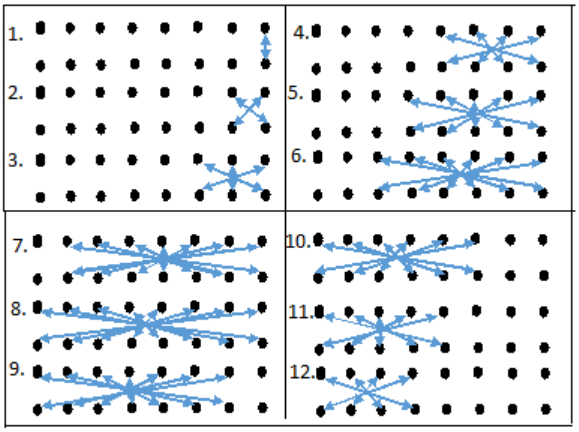


Fig 4: Steps of Urdhav Tribhayam Sutra for 8 bit Multiplication.

3.4 Speed efficient design for Vedic multiplier

The proposed tree structure diagram block diagram of my 8 bit Vedic multiplier as shown in fig. 5 below [8]. According to this architecture design the output is stored in the 16 bit register which is the concatenate of the output obtained from 12 bit ripple carry adder, 4 bit LSB of mult0 value.

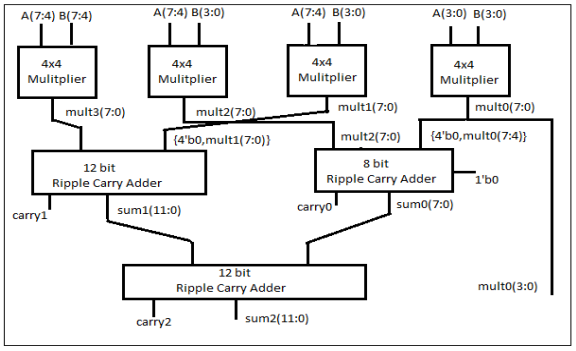


Fig5: Block Diagram of 8 Bit Multiplier[8].

4. TESTING AND RESULT SIMULATION

For the design synthesis of the multiplier Xilinx ISE 14.7 Tools is used. Design entered in the form of Verilog. Here RTL schematic, test bench waveform and device utilization summary has shown. The simulation result is analysed in the ISim simulator.

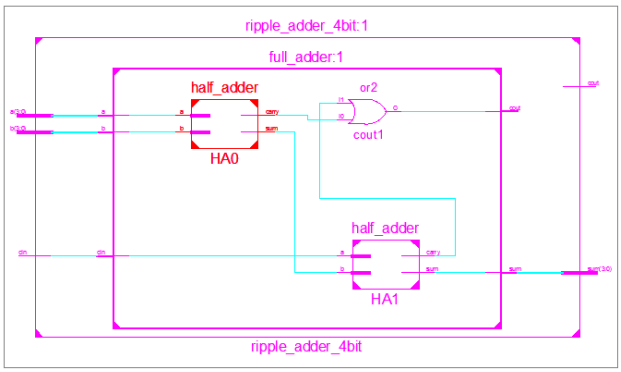


Fig 6: RTL of 4 Bit Ripple Carry Adder

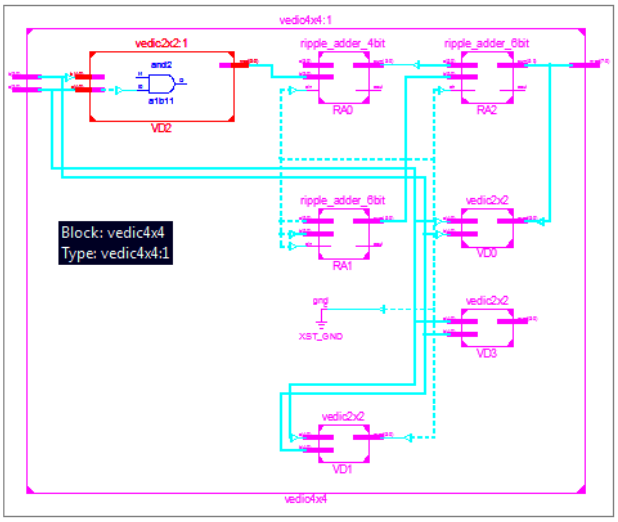


Fig 7: RTL schematics of 4 bit Vedic Multiplier

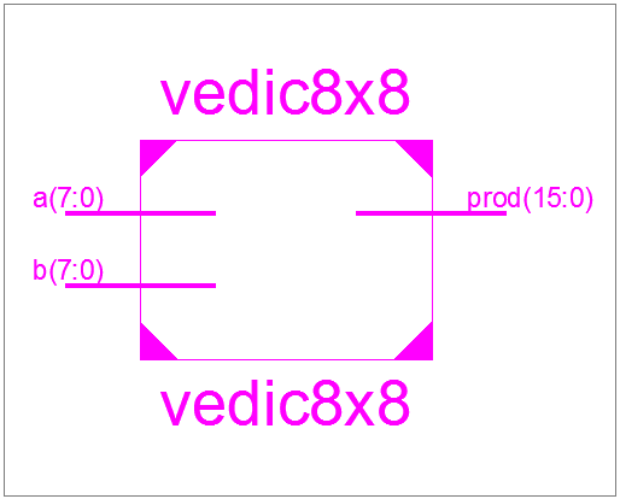


Fig 8: RTL schematic of 8x8 Vedic Multiplier.

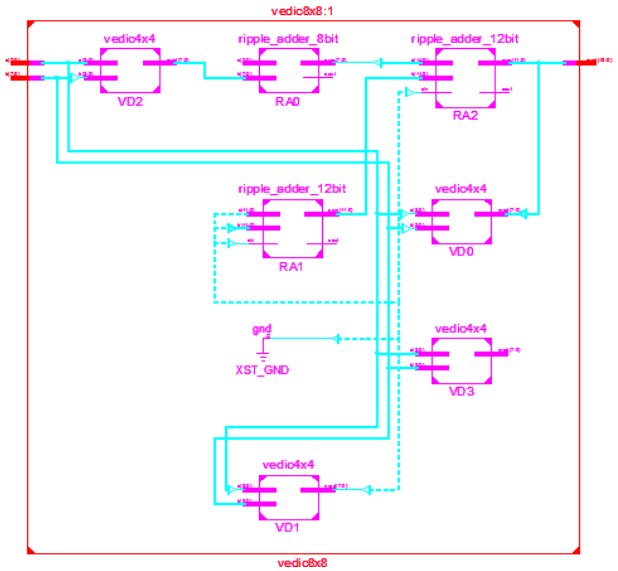


Fig 9: RTL schematics of 8bit Vedic Multiplier

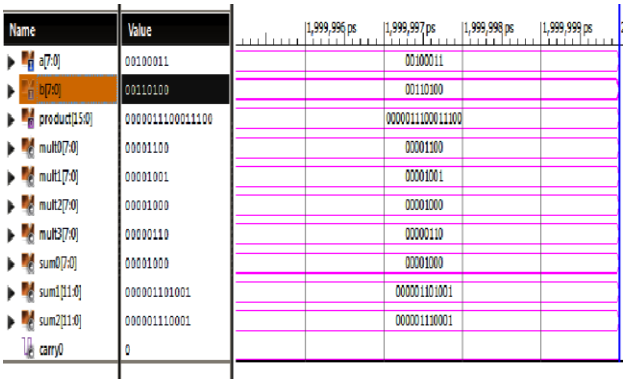


Fig 10: Simulation Result of 8x8 Vedic Multiplier

5. COMPARISON TABLE AND DEVICE UTILIZATION SUMMARY

Table 1. Device Utilization Summary

Number of slice LUT	109 out of 63400
Number of IOs	32
Number of bonded IOs	32 out of 210
Number of LUT Flip Flop	109

Table 2. Comparison between conventional and Vedic multiplier

Design	Conventional Multiplier	Vedic Multiplier
Frequency (MHz)	5.5	13.9
Leakage power(nW)	072.66	082.28
Dynamic power(mW)	13.87	8.66
Area (Gate Count)	2301	1380

6. CONCLUSION

The "Urdhav Tribhayam" technique is used to design the 8 bit Vedic Multiplier in efficient and innovative way . The coding is done in Verilog and it has been synthesis using Xilinx ISE 14.7. The proposed Multiplier is faster than the array and conventional multiplier because of an efficient and structural use of Ripple Carry Adder. The difference in the blocks used is due to the structural modeling. The frequency of the proposed multiplier is higher than the conventional multiplier. Moreover, the number of gates count used is lesser as compared to conventional multiplier. In future, using Vedic Mathematics it is possible to make very fast and efficient ALU or Math Co-processor. Vedic mathematics can be implemented in the field of DSP and ADSP processor to employ the complex calculation by calculating the various terms like FFT and IFFT. The proposed technique for multiplication can be used in latest processors for efficient design in terms of area and speed.

7. ACKNOWLEDGEMENT

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8. REFERENCES

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