Quasi-Floating Gate MOSFET based Current-to-Voltage Converter

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ABSTRACT
This paper demonstrates the use of quasi-floating gate MOSFET (QFGMOS) in the design of a current-to-voltage converter that operates for the input current range of 0 to 50μA. The workability of the circuit has been verified using SPICE simulations for 0.18μm CMOS technology with the supply voltages of ±0.5V. From the simulation results, it has been observed that the proposed circuit has low power dissipation of 50.16μW, bandwidth of 115.6 MHz and total harmonic distortion (THD) is 1.08%.

Keywords
Quasi-floating gate MOSFETs, Current-to-voltage converter, Low-voltage, Low-power, SPICE

1. INTRODUCTION
In today's age of modern electronics, development of portable, battery operated devices has gained prominence. The design of these devices is tightly constrained with the requirement of small size and long battery lifetime. This has resulted in an increased interest in the design areas of reduced supply voltage and minimized power consumption. Although scaling of the device supply voltage offers a simple method to significantly reduce the dynamic power dissipation. It is however, limited by the increased delay. To compensate this increased delay the device threshold voltage, V_{TH} can be downscaled. This reduction in V_{TH} cannot be done in direct proportion to the supply voltage due to increased subthreshold leakage and threshold voltage fluctuations.

Over the years several techniques to overcome the constraints of Low Voltage/ Low Power (LV/LP) design have been developed. Some of the techniques are subthreshold MOSFETs, bulk driven MOSFETs, self cascodeMOSFETs, floating gate MOSFETs (FGMOS) [1] and Quasi-floating gate MOSFETs (QFGMOS). Limitations such as poor frequency response and poor linearity are observed in case of subthreshold MOSFET technique [2]. Bulk driven MOSFETs have smaller transconductance and bandwidth compared to gate driven MOSFETs. Self cascode MOSFET technique increases the chip area and also this technique does not provide any benefit in input compliance voltage at input front.

Floating Gate technology is a LV/LP technique that is being widely used for the implementation of both low voltage analog and digital circuits. The FGMOS differs from conventional MOSFET in that it has one more gate called floating gate. The floating gate is surrounded by SiO_2 insulating layers on all sides and hence is electrically isolated [3]. The signal inputs are connected to the floating gate capacitively and its DC operating point is left floating.

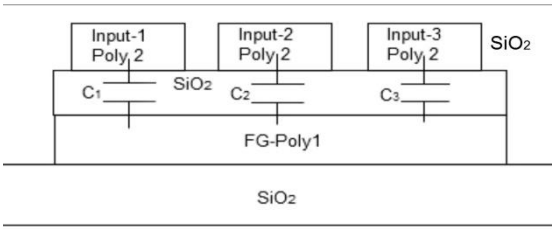

Figure 1. Capacitances in a typical FGMOS transistor [3]

A typical structure of FGMOS is shown in Figure 1 [3]. The multiple device signal inputs (Vi, i=1,2,3) are applied to a second layer of polysilicon placed on top of the SiO_2 layer covering the floating gate. The sizes of the input electrodes used for the input signal coupling determine the values of the capacitors(C_1, C_2, C_3) connecting the inputs to the floating gate. FGMOS allows device operation at downscaled supply voltages by reducing the effective threshold of the device [4]. However this reduction in effective threshold is achieved at the cost of reduced transconductance and gain- bandwidth product. Another drawback of using FGMOS is the charge trapped on the floating gate during fabrication which results in large DC offsets if it is not removed [5].

Quasi-Floating Gate MOSFET (QFGMOS) is a relatively new technique, observed to offer advantages over FGMOS in terms of better frequency response, less chip area and elimination of the initial trapped charge problem [6]. With these advantages over the FGMOS technique experimental verification of QFGMOS based circuits in literature is gaining momentum. Different QFGMOS based circuits such as tunable MOS resistors [7], current conveyors [8] and current mirrors [9-12] have been proposed in recent literature.

This paper presents a current-to-voltage converter circuit using QFGMOS technique and validates the effectiveness of this technique in achieving low voltage/ low power requirements. This paper is organized as follows. Section 2 discusses the QFGMOS device while in section 3 the QFGMOS based current-to-voltage converter circuit is proposed. Section 4 presents the SPICE simulation results. The paper is concluded in Section 5.

2. QFGMOS TECHNIQUE

QFGMOS devices, having evolved from FGMOS devices, also use an additional gate referred to as the quasi floating gate. The quasi-floating gate is connected to one of the DC power rails (V_{DD} or V_{SS}) through a large valued resistor, R_{Large}, implemented using a diode connected MOSFET operating in the cut-off region. In the schematic of an N-input p-type QFGMOS, illustrated in Figure 2 [6], the DC voltage at the gate is determined by V_{bias}($V_{SS}$for this case) coupled through bias transistor (operating in cut-off region).

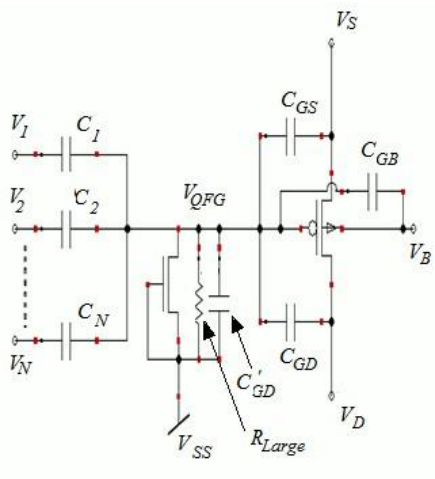

Figure 2.Schematic of N-input p-type QFGMOS [6]

The voltage at the quasi floating gate (V_{QFG}) is given as [6]:

$$V_{QFG} = V_{in}\left(\frac{sR_{Large}\ C_T}{1+sR_{Large}\ C_T}\right) \quad (1)$$

where voltage V_{in} and total capacitance C_T are:

$$V_{in} = \frac{1}{C_T}\left(\sum_{i=1}^{N} C_i V_i + C_{GD}V_D + C_{GB}V_B + C_{GS}V_S\right) \quad (2)$$

$$C_T = \left(\sum_{i=1}^{N} C_i + C_{GD} + C_{GB} + C_{GS} + C'_{GD}\right) \quad (3)$$

where V_D is the drain voltage, V_B is the bulkvoltage, V_S is the source voltage, $C_{i\ (i=1,2,3\ldots,N)}$ are the capacitances between the quasi-floating gate and the control gates, C_{GD}, C_{GB}& C_{GS} are the parasitic capacitances of PMOS to the floating gate and C'_{GD} is the parasitic capacitance of the biasing diode connected NMOS transistor.Using (1) and (2), V_{QFG} becomes:

$$V_{QFG} = \left(\frac{sR_{Leak}\ C_T}{1+sR_{Leak}\ C_T}\right)\frac{1}{C_T}\left(\sum_{i=1}^{N} C_i V_i + C_{GD}V_D + C_{GB}V_B + CGSVS\right) \quad (4)$$

From (4), it is apparent that the input signals encounter a high pass filter with a cut-off frequency $f_C$as:

$$f_c = \frac{1}{2\pi R_{Large}\ C_T} \quad (5)$$

In (5) it can be seen that the very large value of R_{Large} causes the frequency to be very small. Therefore, equation (4) can be written as:

$$V_{QFG} = \frac{1}{C_T}\left(\sum_{i=1}^{N} C_i V_i + C_{GD}V_D + C_{GB}V_B + C_{GS}V_S\right) \quad (6)$$

From (6) it is observed that, the voltage at the quasi floating gate is a weighted average of the ac input voltages determined by capacitance ratios when ignoring parasitic capacitances.

For a 2-input QFGMOS, when a DC bias is applied at the QFG node and input signals are capacitively coupled, the input voltage swings above or below the applied DC bias voltage. Therefore, the DC bias provides an effective threshold voltage that permits a scaled supply voltage environment. The effective threshold voltage is given as [13]:

$$V_{TH,eff} = \frac{V_{TH} - K_2 V_{DD}}{K_1} \quad (7)$$

where, $K_1 = \frac{C_1}{C_T}$ and $K_2 = \frac{C_{GD}'}{C_T}$.

From (7) it is clear that the effective threshold voltage of a 2-input QFGMOS device is lower than the threshold voltage (V_{TH}) of a conventional MOSFET.

3. QFGMOS BASED CURRENT-TO-VOLTAGE CONVERTER

A current-to-voltage converter can convert the current applied to its input terminal into a proportional output voltage. The block diagram of a current-to-voltage converter is shown in Figure 3.

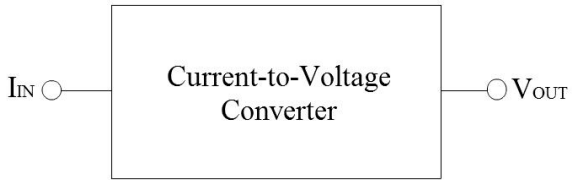

Figure 3.Block diagram of a Current-to-Voltage converter

The proposed QFGMOS based current-to-voltage converter is shown in Figure 4. The transistors MN1 and MN2 are biased in the ohmic region. Transistors MN3, MN4, MP5 and MP6 are biased in the saturation region. The transistors MB1- MB4 are biased in cut-off region.

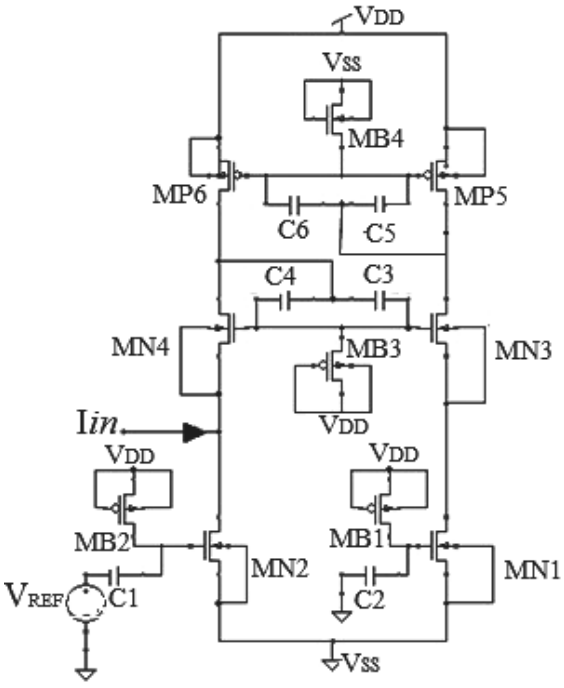

Figure 4.Circuit of a QFGMOS based current-to-voltage converter

The drain currents of MN1 and MN2, i.e. I_1 and I_2, are given as:

$$I_1 = \frac{K_{MN1}}{2}(2(V_{DD} - V_{SS} - V_{TMN1})V_{DS1} - V_{DS1}^2) \quad (8)$$

$$I_2 = I_4 + I_{in} = \frac{K_{MN2}}{2}(2(K_2 . V_{REF} + V_{DD} - V_{SS} - VTMN2VDS2 - VDS22) \quad (9)$$

where, I_4 and I*in* are the drain current of MN4 and the input current, respectively. Also, $K_2 = \frac{C_2}{C_{Total}}$ is the capacitive coupling ratio, K_{MN1}& K_{MN2} are transconductance parameters of MN1 and MN2, V_{TMN1}& V_{TMN2} are their threshold voltages and V_{REF} is applied as the bias voltage that controls the gain of the circuit.

Transistors MP5 and MP6 form a current mirror which duplicates current I_1 as:

$$I_1 = I_3 = I_4 \quad (10)$$

where I_3 and I_4 are drain currents of MN3 and MN4 respectively.

The drain current I_3 of MN3 is given as:

$$I_3 = \frac{K_{MN3}}{2}(V_{GS3} - V_{TMN3})^2$$

$$\text{or} V_{GS3} = \sqrt{\frac{2I_3}{K_{MN3}}} + V_{TMN3} \quad (11)$$

where K_{MN3} is the transconductance parameter of MN3 and V_{TMN3} is its threshold voltage.

Also, the gates of MN3 and MN4 are at the same potential, therefore:

$$V_{GS3} + V_{DS1} = V_{GS4} + V_{DS2} \quad (12)$$

Since, $V_{GS3} = V_{GS4}$, (12) is simplified as :

$$V_{DS1} = V_{DS2} \quad (13)$$

Using (9),(10) and (13), the input current I*in* is given as:

$$I_{in} = \frac{K_{MN2}}{2}(2. K_2 . V_{REF} . V_{DS2}) \quad (14)$$

For the simplification it has been assumed that MN1 and MN2 are perfectly matched i.e. K_{MN1}=K_{MN2} and V_{TMN1}=V_{TMN2}.

Equation (14) can also be written as:

$$V_{DS2} = \left(\frac{1}{K_{MN2} K_2 V_{REF}}\right) I_{in} \quad (15)$$

From (15) it is clear that the output voltage is directly proportional to the input current which verifies the current-to-voltage conversion behaviour of the proposed circuit.

4. SIMULATION AND RESULTS

The proposed QFGMOS based current-to-voltage converter is simulated using SPICE in 0.18µm CMOS technology. The circuit operates at the supply voltages of ±0.5V. The DC characteristics of the circuit for a variation in I*in* from 0 to 50µA and for different values of V_{REF} ranging from 0.35V to 0.5V have been plotted in Figure 5. Distortion analysis of the proposed circuit was performed for I*in*'s peak value of 25µA at the frequency of 100MHz and the THD was observed as 1.08%. The power dissipation of the circuit is 50.163µW.

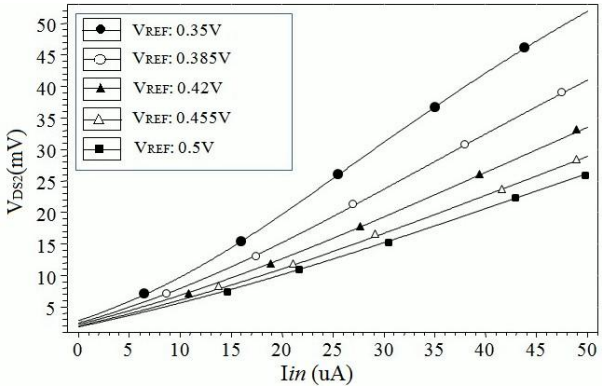

Figure 5.I-V characteristics of QFGMOS based current-to-voltage converter

Table 1 compares the proposed QFGMOS based current-to-voltage converter with the FGMOS based converter [14] and the gate-driven converter [15].

Table 1. Comparison of QFGMOS based current-to-voltage converter with current-to-voltage converters reported in [14, 15]

Circuit Parameters	QFGMOS based current to voltage converter	FGMOS based current-to-voltage converter [14]	Current-to-voltage converter [15]
Supply Voltages (V)	V_{DD}=|Vss|=0.5	V_{DD}=|Vss|=0.75	V_{DD} =2.5
Current range	0-50µA	0-35µA	0-35µA
Power Dissipation	50.16µW	137µW	Not Available
THD (%)	1.08	0.68	Not Available
3 dB frequency (MHz)	115.6	1.1	Not Available

The table points out the advantages offered by the QFGMOS based current-to-voltage converter in terms of its low supply voltage requirement, wide input current range, low THD and low power dissipation.

5. CONCLUSION

This paper presents a QFGMOS based current-to-voltage converter. The current-to-voltage converter circuit has various applications in conventional electronic circuits. It is used for the conversion of the current detected by sensors, such as a photodiode, into a proportional voltage output. It also has applications in digital-to-analog converter (DAC) blocks. Based on the simulation results, it is concluded that the proposed circuit exhibits low power dissipation and low voltage requirement with an extended input current range, making it an efficient converter to be used for the implementation of the mentioned applications in future. An improvement in the bandwidth of the circuit is also observed. SPICE simulation results have been used to demonstrate the workability of the proposed circuit.

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