Design and Analysis of High Performance Novel 3T XOR Gate based 32-bit Adder at 28nm Technology

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ABSTRACT
In this paper, we designed and simulated a low power one bit, 8-bit and 32-bit full adder circuits namely Novel 10T, N14T, FA24T, CPL (complementary pass-transistor logic) and DPL (double pass-transistor logic). All the adders are tested by using one bit, 8-bit and 32-bit ripple carry adder architecture using Tanner EDA tool version 13.0. The one bit Novel 10T, N14T, XOR/XNOR function technique has been used for the generation of full adders. The proposed design successfully works with the buffering circuit in the full adder design. All full adder circuits are simulated withT-SPICE using 28nm Technology with 500 Mega Hertz frequency at 0.9 volt supply voltage. Due to lesser length requirement in the individual transistor, all the design of adders require lesser area as compared to existing design results in the tables. There is also improvement in terms of power, delay and power-delay-product (PDP).

Keywords
Full adder, Ripple carry adder, Average power, Delay, Power-delay-product (PDP), Leakage power, Noise margin.

1. INTRODUCTION
With the increasing demand of high speed portable devices and electronic systems much of the research efforts is directed towards increasing the speed of digital systems which has made present day technologies as a powerful work stations, personal computers and high definition multimedia capabilities. Most of the above mention devices are portable and strongly dependent upon the battery power. The other reason is to save energy in battery operated instruments same as electronic watches where average power is in microwatts. Average power is calculated by given pulse widths at input. As the frequency is increasing, power consumption is increasing and also the reliability of the devices is decreasing that is why power saving is becoming the important requirement for low power design and also important parameter of digital VLSI design [6].

2. DESIGN OF FIVE TYPES OF FULL ADDERS
There are different types of CMOS full adder circuits. This section reviews the five styles of one bit full adder circuits, which are operated at 500 Mega Hertz frequency with 0.9 volt supply voltage by using 28nm Technology. The first full adder structure in this section one bit Novel 10T shown in Figure 1. N10T has 10 transistors. One bit N14T full adder with 14 transistors based on XOR gate and transmission gate multiplexer has been presented shown in Figure 2. One bit FA24T structure is shown in Figure 3. FA24T has 24 transistors. The structure of FA24T has two transistors less than bridge and has better power consumption. However, in FA24T the Sum generator should wait to receive the Cout signal from the Cout generator. Design of one bit complementary pass-transistor logic (CPL) type logic style, there are 24 transistors. Figure 4 shows circuit diagram of one bit CPL type adder Design of one bit double pass-transistor logic (DPL) is also designed, which has 34 transistors. Figure 5 shows circuit diagram of one bit DPL type adder.

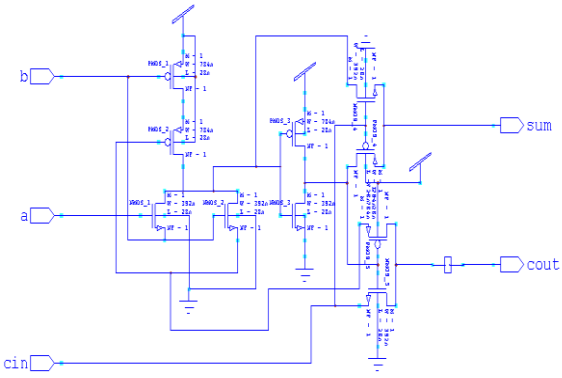


Fig 1: Design of one bit N10T full adder

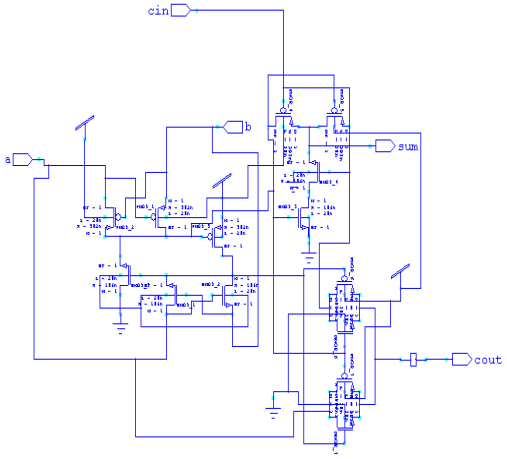


Fig 2: Design of one bit N14T full adder

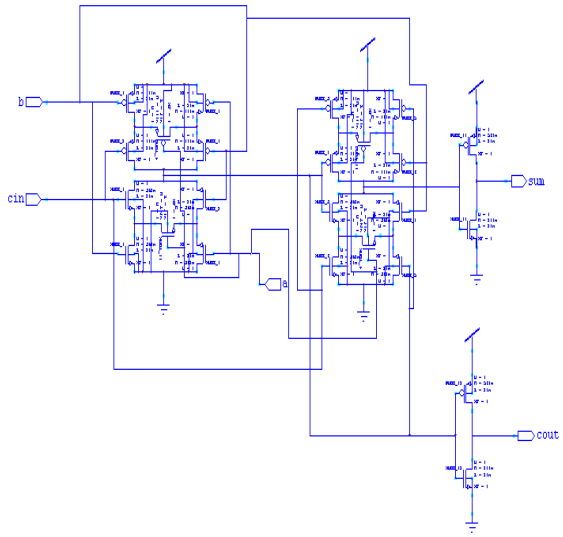


Fig 3: Design of one bit FA24T full adder

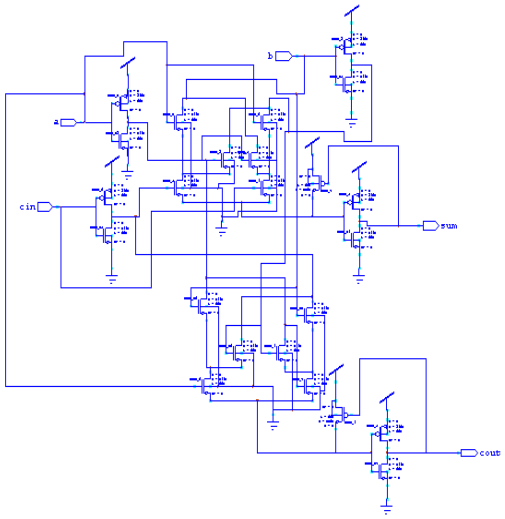


Fig 4: Design of one bit CPL logic style full adder

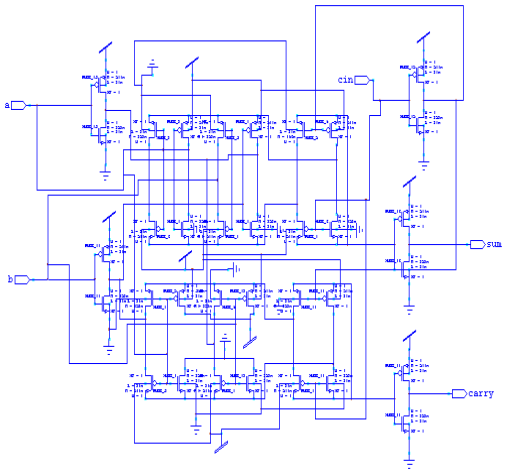


Fig5:Design of one bit DPL logic style full adder

3. IMPLEMENTATION OF FULL ADDER CIRCUITS

One bit N10T and N14T full adder circuits are shown in Figure 1 and Figure 2. These circuits are XOR and XNOR gate based circuits. In the Novel 10T adder circuit, 3 transistors are used for generating of XOR functions [3]. In one-bit binary full adder, three one-bit inputs: A, B and Cin and outputs: sum and carry.

$$Sum = (A \oplus B) \oplus Cin) \qquad (1)$$

$$Carry = A.\ B + Cin\ (A \oplus B) \qquad (2)$$

The motive of this paper is to design a low power full adder circuit with the N10T method. The full adder circuit is shown in Figure 1. Compared to the various structures, a typical one bit full adder in N10T logic has only 10 transistors and the number of interconnections between them is highly reduced by using XOR/XNOR gates. In one bit complementary pass transistor (CPL) full adder, there are 24 transistors. In one bit double pass-transistor logic (DPL) full adder, there are 34 transistors.

4. SIMULATION RESULTS

All full adder circuits operate in 500 Mega Hertz frequency range with voltage supply is 0.9 volt at 28nm technology by varying width. Output waveform of one bit N10T is shown in Figure 6, which shows better simulation results than other four types of full adders.

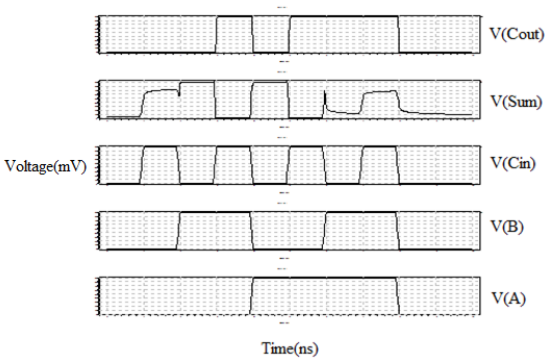


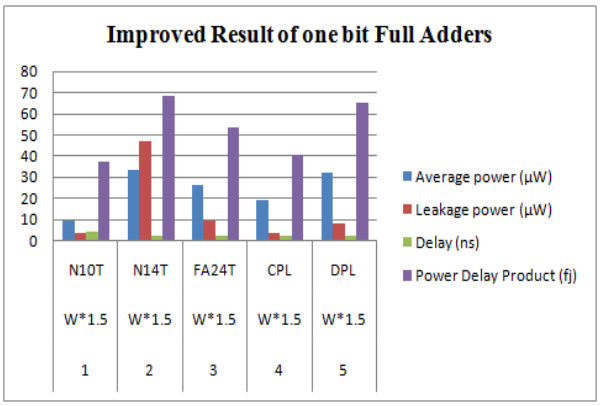
Fig 6: Output waveform of one bit N10T full adder

4.1 Simulation Result of One Bit Full Adders

In the Table 1, simulation results compared [3], [5] performance of full adders has been there, compared circuits [3] simulations are performed at 0.35µm Technology with 1.8 volt supply voltage, compared circuits [5] are performedat 0.18µm technology with 1.8 volt supply voltage and at 100MHz frequency, these results compared with present work. Simulation results compared[9], compared circuit [9] is performed at 0.18µm technology with 1.8 volt supply voltage in 200MHz frequency range, result [9] compared with present work. In compared results [3], [5], [9], leakage power is not measured. Table 1 shows simulation result of one bit full adders compared. In the present work, circuits operate in 500 Mega Hertz frequency with 0.9 volt supply voltage at 28nm Technology and leakage power is also measured in the present work.

Table 1: Result of five types of one bit full adders compared

S. No.	Parameters	[3]	[5]			[9]	Present Work				
		N14T	N10T	FA24T	CPL	DPL	N10T (W*1.5)	N14T (W*1.5)	FA24T (W*1.5)	CPL (W*1.5)	DPL (W*1.5)
1	SupplyVoltage (V)	1.8	1.8	1.8	1.8	1.8	0.9	0.9	0.9	0.9	0.9
2	Technology (nm)	350	180	180	180	180	28	28	28	28	28
3	Average Power (µW)	132.003	1.13	1.66	2.5	184.8	9.14	33.38	25.80	18.80	31.55
4	Maximum Delay (ns)	0.16	73.5	137.9	141.1	0.28	4.03	2.04	2.06	2.16	2.06
5	Power DelayProduct (fj)	21.120	83.055	228.914	352.75	51.744	36.834	68.095	53.148	40.608	64.993
6	Leakage Power (µW)	-------	-------	-------	-------	-------	2.93	47.09	9.15	3.01	7.88
7	No. of Transistors	14	10	24	18	32	10	14	24	24	34



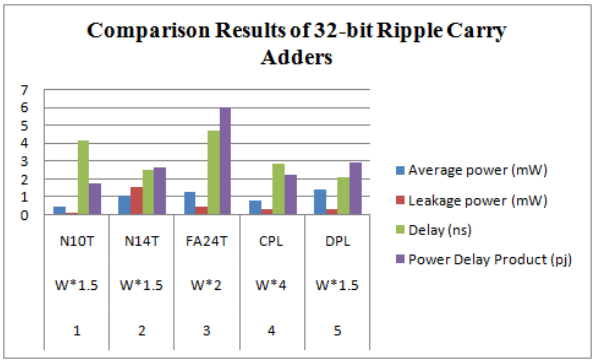
Graph of one bit N10T, N14T, FA24T, CPL and DPL type full adders

4.2 Simulation Result of 8-Bit Ripple Carry Adders

In Table 2,N10T (CLRCL-Complementary and Level Restoring Carry Logic) [10] is performed at 0.35µm Technology with 3.3 volt supply voltage in 132 Mega Hertz frequency. N14T [10] is performed at 0.35µm Technology with 3.3volt supply voltage in 273 Mega Hertz frequency. In this result [10], leakage power is not measured. Present workperforms in 500 Mega Hertz frequency with 0.9 volt supply voltage at 28nm Technology.

4.3 Simulation Result of 32-Bit Ripple Carry Adders

Comparison result of 32-bit N10T, N14T, FA24T, CPL, DPL type ripple carry adders are given in the Table 3. In these types of adders, N10T is better than all other four types of adders, which has lesser average power and power-delay-product. CPL and DPL type full adders have also lesser power-delay-product as compared to FA24T full adder. CPL type adder has lesser average power as compared to N14T, FA24T and DPL type adders as shown in the Table 3.



Graph of 32- bit N10T, N14T, FA24T, CPL and DPL type ripple carry adders

Table 2: Result of five types of 8-bit ripple carry adders compared

S. No.	Parameters	[10]		Present Work				
		N10T(CLRCL)	N14T	N10T(Width *1.5)	N14T(Width *1.5)	FA24T(Width*2)	CPL(Width *4)	DPL(Width* 2.5)
1	Supply Voltage (V)	3.3	3.3	0.9	0.9	0.9	0.9	0.9
2	Technology (nm)	350	350	28	28	28	28	28
3	Average Power (µW)	0.783	0.812	105.38	319.34	204.83	191.45	405.61
4	Delay(ns)	7.43	3.66	0.98	0.57	0.92	0.66	0.37
5	Power DelayProduct (fj)	5.817	2.971	103.272	182.023	188.443	126.357	150.075
6	Leakage Power (µW)	-------	-------	24.65	377.96	98.19	66.31	106.75

Table 3: Result of five types of 32-bit ripple carry adders compared at 500MHz frequency by using 28nm technology

S. No.	Parameters	N10T(Width*1.5)	N14T(Width*1.5)	FA24T(Width*2)	CPL(Width*4)	DPL(Width*1.5)
1	Supply Voltage (V)	0.9	0.9	0.9	0.9	0.9
2	Average power (mW)	0.42	1.05	1.28	0.79	1.39
3	Delay(ns)	4.14	2.48	4.70	2.83	2.09
4	Power DelayProduct (pj)	1.738	2.604	6.016	2.235	2.905
5	Leakage power (mW)	0.09	1.51	0.39	0.26	0.25

4.4 Noise Margin of XOR Gate Based One Bit Full Adders

Noise margin is calculated from the formula given below [2] :

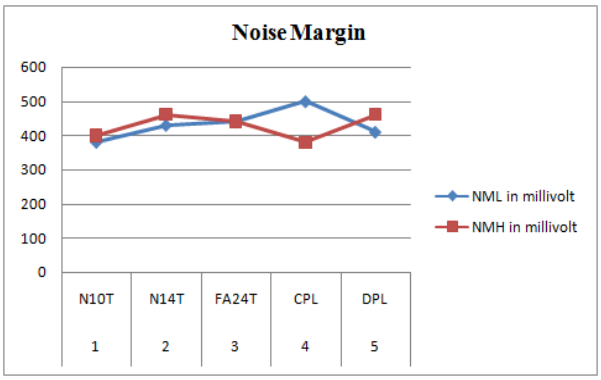
$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

Noise margin is the amount by which a signal exceeds the minimum amount of proper operation. In VLSI system, Noise margin (in circuits) is the amount of noise that a circuit couldwithstand without compromising the operation of the circuit.Noise margin at low voltage and noise margin at high voltage of one bit N10T, N14T, FA24T, CPL, DPL type full adders are shown in the Table 4. N10T has lesser noise margin at low voltage level as compared to other four types of full adders.

Table 4: Result of noise margin of five types of one bit full adders

Name of Adder	V_{IL} in volt	V_{OL} in volt	V_{OH}= V_{DD} in volt	V_{IH} in volt	NM_L in mV	NM_H in mV
N10T	0.380	0	0.9	0.500	380	400
N14T	0.430	0	0.9	0.440	430	460
FA24T	0.440	0	0.9	0.460	440	440
CPL	0.500	0	0.9	0.520	500	380
DPL	0.410	0	0.9	0.440	410	460



Graph of noise margin of one bit N10T, N14T, FA24T, CPL and DPL type full adders

5. CONCLUSION

In the present work, five types of one bit, 8-bit, 32-bit full adder circuits are designed based on ripple carry adder architecture with T-spice simulation from the netlists, in 500MHz frequency with 0.9v supply voltage at 28nm technology. The aim of this work had been power and delay reduction in the full adder circuit. In this operation, N10T, N14T, FA24T, CPL, DPL adders are introduced. Delay of one bit N10T is 94.51% improved and 55.65% power-delay-product (PDP) improved [5]. In case of one bit N14T, average power is 74.71% improved [3] and one bit FA24T, delay is 98.50% improved and PDP 76.78% improved [5]. In case of one bit CPL, delay is 98.46% improved and PDP 88.48% improved [5] and one bit DPL, average power is 82.92% improved [9]. In case of 8-bit N10T, delay is 86.81% improved and delay of 8-bit N14T is 84.42% improved [10]. In case of 32-bit adder circuits, result of N10T adder circuit is better than four other types of adders. From present work, result of N10T is better than four other types of adders. All the designed adder circuits in this paper can be optimized for higher frequency range up to GHz. Reduction in area and improvement innoise margin can be the future scope of this paper.

6. ACKNOWLEDGEMENTS

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