Evolution of Transistor Technology from BJT to FinFET -- A study

Aman kumar
Student
chandigarh university
Gharuan,India

Bobbinpreet Kaur
Assistant Professor
Chandigarh University
Gharun,India

Mamta Arora
Assistant Professor
Chandigarh University
Gharun,India

ABSTRACT
The presentation of FinFET Technology has opened new sections in Nano-innovation. The arrangement of ultra-thin fin empowers stifled short channel effects. It is an alluring successor to the single gate MOSFET by the righteousness of its prevalent electrostatic properties and relative simplicity of manufacturability. Fin type field-impact transistors (FinFETs) are promising substitutes for mass CMOS at the Nanoscale. FinFETs are double gate device. The two gates of a FinFET can either be shorted for higher execution or autonomously controlled for lower spillage or decreased transistor number. These offers ascend to a rich outline space. Thus, a few difficulties and barricades that FinFET innovation needs to face to be focused on other innovation choices like, high get to resistance identified with the greatly thin body, implementation of strain promoters and manufacturability identified with the non-planar procedure and tight process control.

Keywords
Transistors; short channel effects; FinFET; fin shape; SRAM

1. INTRODUCTION
In the view of the fabrication of MOSFET, the minimum channel length has been decreasing continuously. The persuasive driving this to grow interested in high-speed devices and expanding enthusiasm for rapid devices on a huge scale coordinated circuits. As scaling approaches more than one physical limit and as new device structures and new materials are presented. So, FinFET transistor has been offered to prevent the issues because of downscaling of MOSFET dimension i.e. Reduce the short channel effects like DIBL sub threshold conduction, punch through, hot electrons etc. This result makes it more difficult for the voltage on a gate electrode to deplete the channel underneath and stop the flow of carrier through the channel through raising the channel above the surface of the wafer instead of creating the channel just below the surface. It is conceivable to wrap the gate around up to three of its sides and offering much more prominent electrostatic control over the bearers inside it. Originally, FinFET was created for the utilization on SOI wafer, late propensities have made it achievable to deliver working FinFETs on the mass silicon wafer and fortify the productivity of specific parameters. The lofty doing profile used to control or control spillage into the mass substrate invaluably affects DIBL. FinFET has numerous focal points over planar mass devices. They display more present per unit territory than organizer device. In light of tallness of the fin can be utilized to make the channel with a superior viable volume. The important test of FinFET circuit was a 4-phase inverter by Rainey et al in 2002 and the timeliest report of FinFET ring oscillator was disseminated by Nowak et al [1]. FinFET SRAM cells have been represented in 2002 and 20 MB SRAM exhibit in 2004 [1].

2. TRANSISTOR OVERVIEW
A transistor is a three-terminal device. There are the different types of the transistor has been developed till now .A most common transistor is bipolar junction transistor(BJT).To overcome the shortcoming of the bit scientist has introduced the other transistors like FET, mosfet, FinFET etc.

2.1 Bipolar Junction Transistor
A BJT is a dynamic semiconductor device framed by two P-N intersections whose capacity is the enhancement of an electric current. Bipolar transistors are produced using 3 segments of semiconductor material with 2 coming about P-N intersections. One P-N intersection is between the emitter and the base; the other P-N intersection is between the collector and the base. Note that the emitter and collector are normally doped to some degree in an unexpected way, so they are infrequently electrically compatible. Bipolar transistors are named either NPN or PNP as indicated by their N-type and P-type materials. Their essential development and concoction treatment is suggested by their names. So an NPN transistor is shaped by presenting a dainty area of P-type material between two locales of N-type material. Then again, a PNP transistor is framed by presenting a flimsy locale of N-type material between two districts of P-type material.

Applications

i. High-speed digital logic
ii. Amplifiers
iii. Temperature sensors
iv. Logarithmic converters

2.2 Field Effect Transistor
The FET is based on the possibility that charge on an adjoining thing can pull in charges within a semiconductor channel. The FET comprises a semiconductor channel with anodes at either end alluded to as the drain and the source. A control terminal called the gate is placed in the close region to the channel so that its electric charge can impact the channel. Thusly, the gate of the FET controls the stream of transporters (electrons or gaps) spilling out of the source to drain. So, this can be the method of controlling the size as well as a state ofthe conductive channel. A field-effect transistor (FET) is a kind of transistor routinely used for frail sign upgrade. The device can build basic or propelled signals. It can in like manner switch DC or limit as an oscillator. There are an extensive variety of sorts of FET accessible for which there are diverse names.

1) The JFET utilizes a converse one-sided p–n intersection to discrete the gate from the body.
2) The MOSFET (metal–oxide–semiconductor field-effect transistor) uses as the insulator (regularly SiO2) between the gate and the body. [2]
3) The DGMOSFET (double gate MOSFET) is a FET with two insulated gates.
4) The HIGFET (heterostructure insulated gate field-effect transistor) is presently utilized predominantly as a part of research.
5) The TFET (tunnel field-impact transistor) depends on band-to-band tunneling.
6) The MESFET (metal–semiconductor field-effect transistor) substitutes the p–n intersection of the JFET with a Schottky hindrance; and is utilized as a part of GaAs and other III-V semiconductor materials.
7) The NOMFET is a nanoparticle natural memory field-impact transistor.
8) The GNRFET (grapheme Nanoribbon field-impact transistor) utilizes a grapheneNanoribbon for its channel.

2.3 Metal-Oxide-Semiconductor Field Effect Transistor

In spite of the way that the MOSFET is a four-terminal device with source (S), gate (G), drain (D), and body (B) terminals, [3] the body (or substrate) of the MOSFET is often connected with the source terminal, making it a three-terminal device like other field-impact transistors. Relentless scaling of metal-oxide-semiconductor (MOS) device is the well-worn driver of movement and advancement in the microelectronic business, with today's pushed development passing on a high-performing device at the most reduced nm advancement hubs. Further scaling attempts will be confined by troubles which are currently an issue – tunneling bearers through ultrathin gate dielectrics, short-channel impacts, spoiling sub edge execution, and conceivable quantum-mechanical results for device operation.

3. FinFET EXISTENCE

Notwithstanding the way that, BJT are the moderate device as appear differently in relation to the MOSFET. There is some extraordinary variable which enhanced MOSFET than the BJT. So that MOSFET are using as a part of the various applications. They are also called voltage controlled device. Be that as it may, when downsized the MOSFET to get higher speed short channel impacts are emerges. To defeat this SCF FinFET appeared. FinFETs are new period transistors which use tri-gate structure. Rather than planar transistors where the Gate anode was (generally) over the channel, the gate-cathode "wraps" the direct from three sides in FinFETs.

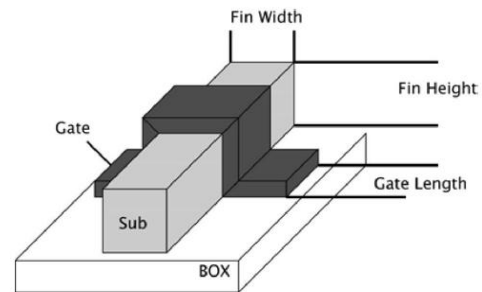


Fig 1: Drawing of the FinFET device [4]

3.1 FinFET Memoirs

The primary multi-gate transistor was that distributed by Hieda et al. [5] in 1987.After two years in 1989, Hisamato et al. created an SOI structure which they called a completely drained incline channel transistor (DELTA) [6]. SOI also enabled even gate-all-around (GAA) transistor making a precursor to silicon nanowire devices. Stacking more than one nanowire on top of each other displayed extended drive current limit for a given foot formed impression size of a transistor [10].This was the at first reported assembling of a FinFET-like structure this was the initially reported manufacture of a FinFET-like structure. In 1990s UC Berkeley group drove by Dr. Chamming Hu proposed another structure for the transistor that would lessen spillage current. FinFETs have pulled in expanding consideration over the previous decade in light of the debasing short-channel conduct of planar MOSFETs [7-12]. Figure 2 shows the better short-channel execution of FinFETs over planar MOSFETs with the same channel length [13].

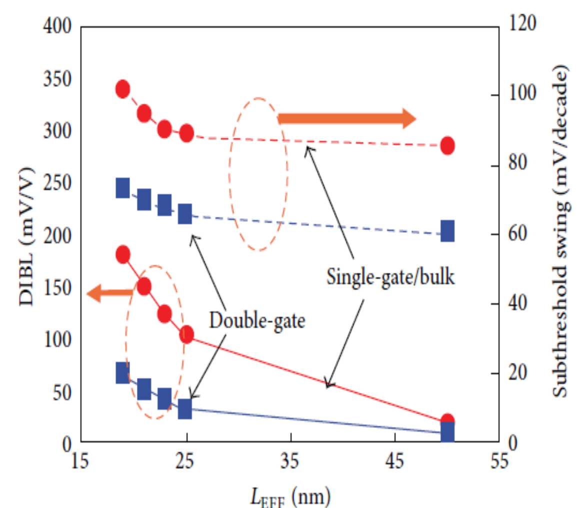


Fig 2: DIBL and sub threshold swing versus effective channel length for double gate and bulk FET [13]

In the FinFET channel is raised so that conduction is occur due to the raised channel Structural comparison between planar MOSFET and FinFET is shown in the figure 3.

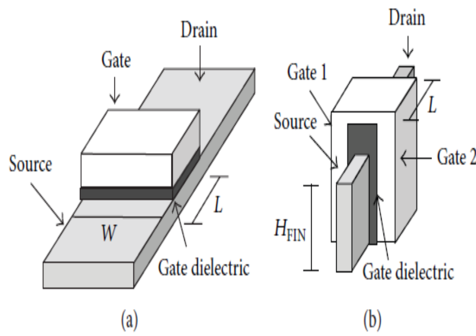


Fig 3: Structural comparison between (a) planar MOSFEET and (b) FinFET [3]

Hence, the height of the channel (Hfin) decides the width (W) of the FinFET. This prompts an extraordinary property of FinFETs known as width quantization. This property says that the FinFET width must be a multiple of Hfin, that is, widths can be expanded by utilizing various fins. Hence, self-assertive FinFET widths are unrealistic. Although smaller fin heights offer more flexibility [14, 15]. In spite of the fact that FinFETs actualized on SOI wafers are extremely well known, FinFETs have additionally been executed on bulk and SOI wafers [16-18]. Figure 4 appears FinFETs actualized on mass and SOI wafers. Not at all like bulk are FinFETs, where all fins share a common Si substrate (too known as the bulk), fins in SOI FinFETs physically isolated.

Consequently, the height of the channel (H_{fin}) chooses the width (W) of the FinFET. This prompts a phenomenal property of FinFETs known as width quantization. This property says that the FinFET width must be numerous of Hfin, that is, widths can be extended by using different fins. Consequently, self-assured FinFET widths are implausible. Although smaller fin heights offer more flexibility [14, 15]. Notwithstanding the way that FinFETs realized on SOI wafers are to a great degree understood, FinFETs have furthermore been executed on mass and SOI wafers [16-18]. Figure 4 shows up FinFETs completed on mass and SOI wafers. Not in any manner like mass are FinFETs, where all fins share a typical Si substrate (excessively known as the mass), fins in SOI FinFETs physically secluded.

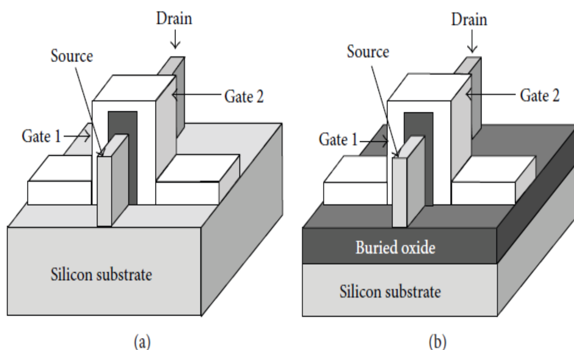


Fig 4: Structural comparison between (a) bulk and (b) SOI FinFETs [3]

3.2 FinFET Classification

There are two primary types of FinFETs: shorted-gate (SG) and independent gate (IG). SG FinFETs are otherwise called three-electrode (3T) FinFETs and IG FinFETs as four-electrode (4T) Fin. In SG FinFETs, both the front and back gates are physically shorter, while in IG FinFETs, the gates are physically isolated (Figure 5). In this manner, in SG FinFETs, both gates are together used to control the electrostatics of the channel. Consequently, SG FinFETs appear higher on-current (Ion) furthermore higher off-current (Ioff or the sub threshold current) contrasted with those of IG FinFETs. IG FinFETs offer the adaptability of applying distinctive signs on the other hand voltages to their two gates.

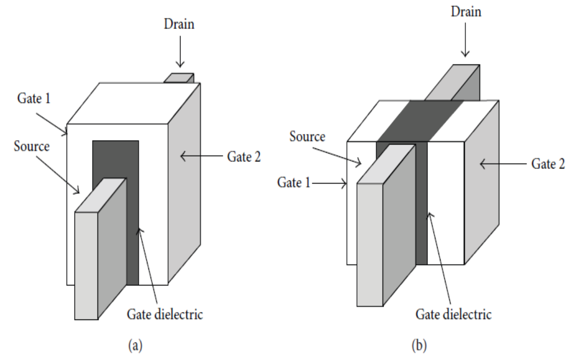


Fig 5: Structural comparison between (a) SG and (b) IG FinFET [3]

This empowers the utilization of the back-gate predisposition to regulate the Vth of the front gate straightly. In any case, IG FinFETs bring about a high zone punishment because of the requirement for setting two separate gate contacts. There are essentially two noteworthy innovations for FinFETs fabricating: Silicon-on-Insulator (SOI) FinFETs and Bulk FinFETs. The primary FinFETs were made on top of protecting layer. The way that the Current can't stream "underneath" the gate when the transistor is in OFF state lessens the spillage current. Elective strategies for preventing spillage current from streaming in the bulk were presented later, which took into consideration assembling of Bulk FinFETs.

4. TECHNOLOGY IN FinFET

Earlier as developed the MOSFET technology but we got some short channel effects so, we moved on to the FinFET technology where the channel is raised.

4.1 5nm FinFET Technology Node

There are many technologies developed through the FinFET. Here Figure 6 demonstrates the structure of a 5nm FinFET device. The FinFET device comprises a thin silicon body, with a thickness of T_{fin}, [19] which is wrapped by gate electrodes. The device is termed semi-planar as the present streams parallel to the wafer plane, and the channel is framed opposite to the plane. The successful gate length LG is twice large as the fin height h_{fin}.The spacer length LSP is an imperative outline parameter that straightforwardly identifies with the short channel impacts [19]. Every fin has two gates: a front gate and a back gate. The FinFET Device permits free control of the front and back gate by scratching ceaselessly the gate electrode at the highest point of the channel. The FinFET device model created in considers a shorted gate mode, in which the front gate and back gate are entwined to accomplish the most astounding drive quality [20]. Note that in this work we concentrate on the shorted gate FinFET device as the autonomous gate device experience suffers from many fabrication issues in practice.

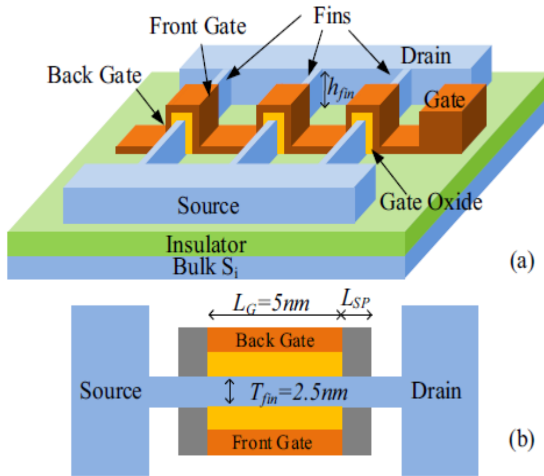


Fig 6: (a) Perspective view and (b) top view of the5nm FinFETdevice [19]

4.2 SRAM

The SRAM cells began to face challenges when device scaling began to happen. Once more, planar innovation, in the end, neglected to meet the prerequisites with device scaling. The FinFET innovation is one of the rising procedures in this circumstance. There are numerous device methodologies of FinFETs to be specific Tunnel FinFET (TFET), intersection less FinFET, pseudo-turn FinFET. By utilizing these device approaches as a part of the SRAM cells, we can beat the SCE in the SRAM. Supply voltage scaling is feasible for TFET without expanding the static force utilization. For SRAM circuit, it is prescribed to utilize 8T/10T cell to accomplish the craved read/compose commotion edge rather than a 6T cell for TFETs. In [21], the creators shown a FinFET based pseudo-turn transistor on the other hand pseudo-turn FinFETs (PS-FinFETs) and he examined that is a non-unpredictable SRAM cell. Intersection less FinFETs (JL FinFETs) encounters less process multifaceted nature than reversal mode FinFETs (IM FinFETs). In [22], they reported that JL-FinFET shows better short channel qualities and higher ON-OFF current proportion contrasted with IM FinFETs.

5. DESIGN CHALLENGES

Although, as increased the speed and reduced the size of the transistor but we are having with some design challenges which we have to remove or reduce.

5.1 Fin Pattering

With a specific end goal to coordinate or surpass powerful width of a FinFET device with that of a planar device put inside of the same foot shaped impression on the wafer, FinFETs should be extremely tall or a greater amount of those should be put per pitch of dynamic zone. For the most part, development of two fins for each base pitch permits sensible fin perspective proportion that meets or surpasses successful width of comparing planar device. Lithographic designing of such fin has a few key downsides:

1. Double designing is required to split the base pitch. The natural overlay error between two fin patterns could prompt undesired fin pitch variety that affects down-stream handling.
2. craved fin width, generally twice littler than the littlest measurement that had been printed in this way, that of the gate length, is beneath well controllable abilities of optical lithography, bringing about poor fin width control.
3. Line edge unpleasantness (LER) of the process prompts generous nearby fin width variability (LWR).

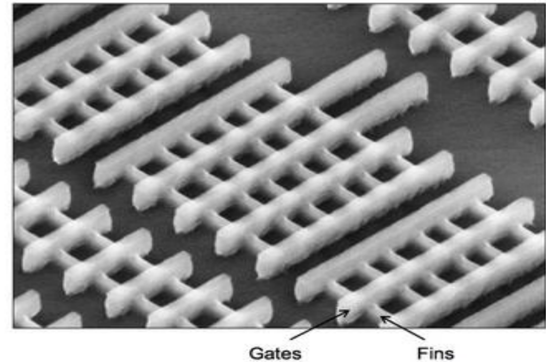


Fig 7: Fin Pattern

Utilizing spacer-characterized self-adjusted double designing (SADP) significantly eases dimensional issues and uses one cover layer as opposed to two. Smaller fin pitches would require SADP technique to be connected twice. The utility of SADP altogether brings down neighborhood variability of fin width brought on by LER, as the spacer LER along its two edges generally mirror one another prompting abundantly enhanced LWR, or fin width variety. EUV lithography, while fit for conveying better-controlled line width for fins than optical lithography, will most likely be unable to enhance the LER of the last in this way leaving SADP as the fin designing technique for decision for 7nm technology node and beyond.

5.2 Fin Orientation

An ostensible introduction of fins, along <110> heading on (100) wafers results in FinFET current streaming on (110) sidewall surfaces. Gap versatility is sizably higher on (110) surface than on (100) yet the distinction diminishes with expanding strain. Electrons stream to some degree slower along (110) plane than on (100) in planar devices. Be that as it may, in FinFETs, quantum imprisonment results in very diverse conduct – electron portability gets to be similar or better for (110) sidewall conduction than for(100) [1].Development of epitaxial material on (100) balance surfaces results in uniform thickness expand that may be wanted in a few circumstances than that of precious stone molded structures developed on (110) wall.

5.3 Fin measurement variability

Fin stature and width can have the solid effect on device execution variability. Of the two, fin stature variety is for the most part more basic [1] device compelling electrical width is specifically identified with fin stature. Consequently, any fin tallness variety because of the variety of fin shaping procedures specifically exchanges to device width variety. Not at all like in planar devices, where dynamic territory designing variety influences just the tightest of transistors, all fin based devices experience the ill effects of the same rate of device width error. This variability is basically identified with the meaning of fin stature by STI dielectric break process in the wake of cleaning planarization and can reach a few percent of each device width.

5.4 Device doping

In a perfect world, one would covet no doping in FinFET channel. However, some light doping might be required to set elective limit voltages in specific devices or better control of under-the-fin spillage current. Those doping are ordinarily doing with implantation. Source/channel doping, which requires high dosages of dopant, countenances huge challenge as far as expanded arrangement resistance. This is identified with insert harm in the fins that, because of fine's geometry, is held in higher sums than in relating planar structures [1]. High temperature (300-400C) inserts, plasma-based doping or purported monolayer doping techniques convey dopants all the more conformably and with less harm to the balance. On the other hand, the in-situ doped epitaxial material is stored in source/channel range to convey the dopant. This can be conveyed with or without evacuation of the fin in source/channel zone preceding epi.

5.5 FinFET Parasitic Capacitance vs. Planar

FinFET has naturally higher parasitic capacitance than comparing planar device. It comprises essentially of the gate to fin capacitance between part of the gate over the fin and the top of the fin, and can be streamlined down to around 5% above planar devices. This capacitance diminishes with diminishing fin pitch and expanding fin stature, per viable device width [1]. Bulk FinFET intersection capacitance between source/channel zone and device well/substrate could be a few times littler than in planar device.

5.6 Reliability

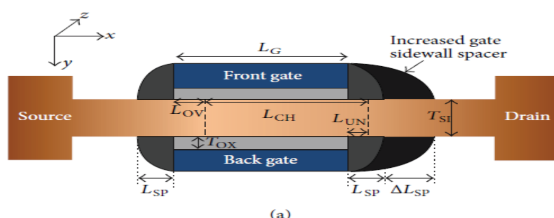
FinFET completely exhausted operation gives lower transverse field in the device. These prompts make strides NMOS unwavering quality for dielectric breakdown (TDDB) too for limit voltage flimsiness (PBTI) seen experiencing significant change from planar 32nm to FinFET based 22 nm innovation nodes. PMOS unwavering quality for both TDDB and NBTI appears unchanged for FinFETs.

6. SPECIFICATION OF FinFET

There are many merits of FinFET with respect to BJT or others devices. Some of the specification of the FinFET is listed below.

6.1 Attribute of FinFET

FinFETs (Figure 8) can prompt enhanced short-channel qualities. In view of an aberrant increment in the channel length. Nonetheless, this change comes at the expense of an expanded design range. This asymmetry likewise crushes the routine compatible source-channel idea in CMOS [23]. An asymmetry is made in the channel-to-source current *IDS* and source-to-deplete current *ISD* on account of the additional underlay. This asymmetry affects FinFET pass transistor performance.



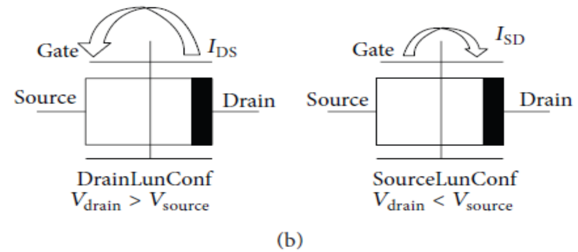


Fig 8: Asymmetric drain spacer extension (ADSE) FinFET [23]

6.2 Comparison between Transistors

The transistors BJT and MOSFET are both valuable for amplification and switching applications. Yet, they have essentially distinctive attributes. BJT, as in Bipolar Junction Transistor, is a semiconductor device that supplanted the vacuum tubes of the days of yore. It is a current-controlled device. Whereas Metal Oxide Semiconductor Field-Effect Transistor, or just MOSFET, and MOS transistor, is a voltage-controlled device. Dissimilar to the BJT, there is no base current present.

Table 1. Comparison betweenTransistors

S. N.	Elements	BJT	MOSFET	FinFET
1	Transistor	Bipolar	Unipolar	Multi-gate or tri-gate architectures
2	Region	A BJT has an emitter, collector and base.	MOSFET has a gate, source and drain.	Conducting channel wrapped by a thin silicon "fin"
3	Applications	They are preferred for low current applications	MOSFET are for high power functions.	FinFET technology that is used within ICs using less power
4	Operation	Dependent on the current at the base	Depends on the voltage at the gate	Much lower power consumption
` 5	Cost	Cheap	Expensive	Expensive

6.3 Advantages of FinFET Technology

FinFETs are new generation transistors which utilize tri-gate structure. In contrast to planar transistors where the Gate electrode was (usually) above the channel, the Gate electrode "wraps" the channel from three sides in FinFETs. The prompt and evident point of interest of FinFETs is that the successful width of the channel gets to be:

Weff=2HSi+WSiWeff=2HSi+WSi (1)

Beyond any doubt, FinFET takes into consideration diminishing of DIBL impact because of the characteristically

more elevated amount of Gate control over the channel. This control originates from the way that might exhaustion areas are limited by the Fin itself and don't reach out into the bulk. However, DIBL is still one of the central point's which influence FinFETs threshold voltages.

FinFETs have the accompanying key favorable circumstances over bulk MOSFETs:

1) Diminished leakage,
2) Excellent sub-threshold incline,
3) Better voltage picks up without debasement of commotion or linearity. This makes them appealing for digital and low-frequency RF applications around 5 GHz
4) Faster exchanging speed. (originates from lower input capacitance and higher element current thickness)
5) Lower power utilization (originates from lower parasitic capacitance and better on/off attributes).
6) Excellent electrostatic control of the channel.
7) Smaller variability.

7. CONCLUSION

A FinFET is another sort of multi-gate 3D transistor that offers huge execution enhancements and forces decrease contrasted with existing planar CMOS devices. In a FinFET, the gate of the device wraps over the leading drain-source channel. This outcome in better electrical properties, giving lower edge voltages and better execution and diminishments in both spillage and element power.FinFET device has been proposed as a promising substitute for the customary bulk CMOS-based device at the Nanoscale. The fin thickness and the gate oxide thickness are the most basic measurements in the outline of FinFETs because of the solid effect of these device parameters on the proficiency of the FinFET engineering in smothering the short-channel impacts and upgrading the on-current. FinFET turned into a promising VLSI innovation for later future because of its unprecedented properties. FinFET innovation has entered the business sector. High execution rationale has adjusted this device and will proceed to utilize it for a few eras into the future. SO, presentation of FINFET innovation towards significantly littler innovation hubs expanding innovative difficulties and limiting its determinations consider more.FINnFETs stand ready to empower the following big leap for PC, interchanges, and consumer devices of all types.FinFETs have alluring qualities, such as excellent control of short channel effects, the ability to tune their execution for vitality proficiency or performance, which implies they can be utilized as the basis of adaptable SoC processes. However, FinFET technology has made new difficulties regarding fabrication processes, corner impacts, quantum impacts. This can be overcome by adopting the new fabrication process. The FinFET is an innovation that is utilized inside ICs. FinFETs are not accessible as discrete devices. However FinFET innovation is turning out to be more far reaching as highlight sizes inside coordinated circuits fall and there is a developing need to give especially more elevated amounts of joining with less power utilization inside incorporated circuits.

8. REFERENCES

[1] Bibin Lawrence R Int. Journal of Engineering Research and Applications ISSN: 2248-9622, Vol. 5, Issue 12, (Part - 1), pp.77-80, December (2015)

[2] Yuhua Cheng, Chenming Hu "MOSFET classification and operation". MOSFET modeling & BSIM3 user's guide Springer. p. 13. ISBN 0-7923-8575-6(1999)

[3] Debajit Bhattacharya and Niraj K. Jha, "FinFETs: From Devices to Architectures," Advances in Electronics, vol. 2014, Article ID 365689, 21 pages, 2014. doi:10.1155/2014/365689

[4] J. P. Sun, Wei Wang, Toru Toyabe, IEEE Transactions On Electron Devices, **Vol. 53**, No. 12, December (2006)

[5] K. Hieda et al., IEDM Tech. Dig., p. 736 (1987)

[6] D. Hisamoto, T. Kaga, Y. Kawamoto, and E. Takeda, "A fully depleted lean-channel transistor (DELTA)—a novel vertical ultra-thin SOI MOSFET," in Proceedings of the International Electron DevicesMeeting (IEDM'89), pp. 833–836, Washington DC, USA, December (1989)

[7] D. Hisamoto, W.C. Lee, J. Kedzierski et al., "FinFET—a selfaligned double-gate MOSFET scalable to 20 nm," IEEE Transactions on Electron Devices**, vol. 47**, no. 12, pp. 2320–2325, (2000)

[8] B. Yu, L. Chang, S. Ahmed et al., "FinFET scaling to 10nm gate length," in Proceedings of the IEEE International DevicesMeeting (IEDM '02), pp. 251–254, San Francisco, Calif, USA, December (2002)

[9] S. Tang, L. Chang, N. Lindert et al., "FinFET—a quasi-planar double-gate MOSFET," in Proceedings of the International of Solid-State Circuits Conference, pp. 118–119, February (2001)

[10] M. Guillorn, J. Chang, A. Bryant et al., "FinFET performance advantage at 22 nm: an AC perspective," in Proceedings of the Symposium on VLSI Technology Digest of Technical Papers (VLSIT '08), pp. 12–13, June (2008)

[11] F.-L. Yang, D.-H.Lee, H.-Y. Chen et al., "5nm-gate nanowire FinFET," in Proceedings of the Symposiumon VLSI Technology- Digest of Technical Papers, pp. 196–197, (June 2004)

[12] X.Huang,W.-C. Lee, C.Kuo et al., "Sub 50-nm FinFET:PMOS," in Proceedings of the IEEE International DevicesMeeting (IEDM 99), pp. 67–70,Washington, DC, USA, December (1999)

[13] E. J. Nowak, I. Aller, T. Ludwig et al., "Turning silicon on its edge [double gate CMOS/FinFET technology]," IEEE Circuits and Devices Magazine, **vol. 20**, no. 1, pp. 20–31, (2004)

[14] M. Alioto, "Comparative evaluation of layout density in 3T, 4T, and MT FinFET standard cells," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, **vol. 19**,no. 5, pp. 751–762, (2011)

[15] N. Collaert, M.Demand, I. Ferain et al., "Tall triple-gate devices with TiN/HfO2 gate stack," in Proceedings of the Symposium on VLSI Technology, pp. 108–109, June (2005)

[16] 16.T.-S. Park, H. J. Cho, J. D. Choe et al., "Characteristics of the full CMOS SRAM cell using

body-tied TG MOSFETs (Bulk FinFETs)," IEEE Transactions on Electron Devices, **vol. 53**, no. 3, pp. 481–487, (2006)

[17] H. Kawasaki, K. Okano, A. Kaneko et al., "Embedded bulk FinFET SRAM cell technology with planar FET peripheral circuit for hp32 nm node and beyond," in Proceedings of the Symposium on VLSI Technology (VLSIT '06), pp. 70–71, June (2006)

[18] S. Y. Kim and J. H. Lee, "Hot carrier-induced degradation in bulk FinFETs," IEEE Electron Device Letters, **vol. 26**, no. 8, pp.566–568, (2005)

[19] S. K. Gupta, W. Cho, A. A. Goud, K. Yogendra, and K. Roy, "Design space exploration of FinFETs in sub-10nm technologies for energy efficient near-threshold circuits," Device Research Conference (DRC), (2013)

[20] N. K. Jha, and D. Chen, Nano-electronic Circuit Design, Springer Press, (2011)

[21] Kerber, P. et al, "Strained SOI FinFET SRAM Design" Electron Device Letters IEEE (Volume: 34, Issue: 7), pp: 876– 878,(2013)

[22] Ming-Hung Han et al, "Device and Circuit Performance Estimation of Junction less Bulk FinFETs", Electron Devices, IEEE Transactions on (Volume:60 , Issue:6), pp:1807 – 1813, (2013)

[23] A. Goel, S. K. Gupta, and K. Roy, "Asymmetric drain spacer extension (ADSE) FinFETs for low-power and robust SRAMs,"IEEE Transactions on Electron Devices, vol. 58, no. 2, pp. 296–308, (2011)