Design Review on High-Swing, High Performance CMOS Operational Amplifier

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ABSTRACT
In this paper a review on the high-swing, high performance CMOS operational Amplifier is carried out and based on the literature, a design procedure for a high-swing high performance Single Stage (HSHPSS) CMOS operational amplifier is proposed using theoretical design equations. A proposed design equation based procedure provides a quick and effective mechanism for estimating the MOS circuit parameters of the operational amplifier.

Keywords
Operational amplifier, Load capacitance, Slew rate, Power Dissipation.

1. INTRODUCTION
Advancement of microelectronic (VLSI) in last decades, became heart of today's designing electronics industry in wireless communications systems. All efforts ultimately decreasing the power consumption and reducing the size of analog circuits enabling the portable electronics devices.

Designing analog circuits with high performance is really a challenging task with high persistent towards reduced supply voltages. Op-amp is major concern in analog circuit. At high voltages, performance characteristics shows trade – off between power, gain and speed,. High output swing, high gain, high PSRR and Low offset voltage are the characteristics that define performance of analog circuit. Key parameters in op-amp are reducing supply voltages and output swing. Due to the advancement in operational amplifier from last decades in a Two-Stage differential op-amp architecture to its performance characteristics Telescopic operational amplifier involving less high gain, low noise, power consumption, etc.

In this paper the design procedure for HSHPSS complementary metal oxide semiconductor Telescopic operational amplifier is proposed using theoretical analysis. The exactable swing of the operational amplifier is obtained by employing the current source and tail of device in the linear region. Swap among performance factors such as output swing, PSRR Gain, bias voltages, slew rate, Phase margin, bandwidth, CMRR, , power are made evident.

2. HIGH SWING IN OPERATIONAL AMPLIFIER
Noise *kT/C* is the dominant noise in analog circuits, the relationship between operational amplifier performance parameters such as SNR, speed (S) and power consumption (P) shown by the following equation.

$$\frac{SNR.S}{P} = \frac{(Swing)^2}{\gamma\left(\frac{kT}{C}\right)} \cdot \frac{\beta\left(\frac{gm}{C}\right)}{V_{sup}(\lambda I)} \qquad (1)$$

Here β, λ and γ constants are the closed loop feedback factor of operational amplifier, the amount of noise effecting at output of device and the ratio of total current utilizing by the operational amplifier to the current passing through its input. Here, dominant pole position decides the speed of the op-amp. The above expression shows as follows

$$\frac{SNR.S}{P} \propto \frac{(Swing)^2}{V_{sup}} \qquad (2)$$

Where, in this case $g_m \propto$ current flowing through input device, when the transistor are in weak/ saturation inversion region. The constant of proportionality at the end is a function of architecture of operational amplifier and the switched-capacitor circuitry around the operational amplifier. It is concluded from above mathematical expression (2) that increasing swing of the operational amplifier leads to improvement of overall performance ,which leads to achieve higher SNR or lower power or speed [2,10].

3. SWING IMPROVEMENT METHODOLOGY
As shown in Figure. 1, transistors for enhancing swing (M_7–M_9) are driven into linear region and V_{margin} is not considered across these devices. Assuming that drain-to-source $V_{ds,tail}$ is at tail and $V_{ds,load,}$ is at load transistor, then output swing is shown as $2V_{sup} - 6V_{ds,sat} - 2V_{margin} - 2V_{ds,tail} - 2V_{ds,load,}$ theoretically $V_{ds,\ sat}$ = 200 mV, V_{margin} =100 mV, $V_{ds,\ tail}$ =80 mV, and $V_{ds,\ load}$ = 160 mV, and $2V_{sup}$ (differential output swing)=1.88 V, this is not more than telescopic amplifier voltage 0.7 V approx, but in case of folded-cascode amplifier voltage is 100 mV approx. The enhancement swing stems is not only the difference among $V_{ds,\ sat}$ and the voltage across op-amp operating in the linear region and V_{margin} is not considered when device operating in linear region. Any reduction $V_{ds,tail}$ improves two fold differential swings as the tail transistor cut into output swing from both sides of the operational amplifier. Swing almost enhanced by $4V_{margin}$ by elimination the marginal voltage across the tail and the load transistor. By pushing the transistors tail

and load both working in linear region there is improvement in swing improve the swing with slightly reducing CMRR and differential gain of the operational amplifier. Both positive and negative PSRR values remains the same with less power dissipation and have good slew rate [13,25].

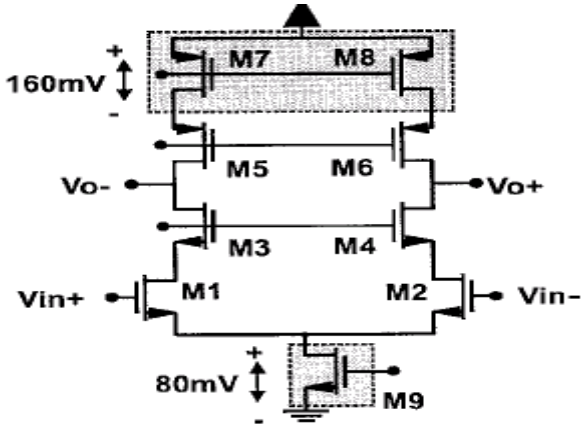

Fig .1. Methodology for enhancing swing

4. DESIGN SPECIFICATIONS

Following are the design parameters

- Load capacitance (C_L)
- Unity gain bandwidth (GB)
- Power Dissipation (P_{diss})
- Slew rate (SR)

5. DESIGN STEPS

5.1 Bias current is estimating by estimating GBW in dominant node. Here tail current is abbreviated as I_{ss} , then we have

$$2\pi f_T = \frac{2I_{ss}}{(V_{GS} - V_{TH})} \frac{1}{C_L}$$

5.2 Tail transistor M_9 is design assuming characteristics of transistor is in linear region and also calculate W and L. Following equation is used to find

$$I_{SS} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_9 \left(2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right)$$

where $V_{GS} \geq V_T$

$$V_{DS}\ \pi\ V_{GS} - V_T$$

5.3: Calculate the V_{B2} (bias voltage) of M_9 using following equation

$$V_{B2} = V_{GS9} - V_{Th}$$

5.4: Differential pair circuit is design by assuming both transistor working in saturation mode and bias current is used to calculate aspect ratios. The equation used is

$$I_{SS} = \mu C_{ox}\left(\frac{W}{L}\right)_{1,2} (V_{GS} - V_{Th})^2$$

5.5: Calculate the CM voltage that allows device (M_9) suppose to be in saturation.

$$V_{in\ cmv} >= V_{sat,\ 9} + V_{GS1}$$

5.6: Design the HCCM an bias voltage is calculated for both transistors (applied to its gates) using following equation and also calculate aspect ratios M_3 and M_4 by assuming both working in saturation mode and matching.

$$V_{B1} - V_2 - V_{Th,\ n} = V_{sat,\ 3}$$

Here $V_{Th,,}$ is the Threshold voltage, V_2 at node 2 and V_{B1} is applied at high Compliance current mirror. The current equation is

$$I_{SS} = \mu C_{ox}\left(\frac{W}{L}\right)_{3,4} (V_{GS} - V_{Th})^2$$

where $V_{GS} = V_{B1} - V_{sat,\ 2} - V_{Th,\ n}$

5.7: Design the CCM (Cascode Current Mirror stage) for four PMOS transistors. They are identical, drain and gates are connected together so same current passing through them.M_5 and M_6 (transistor) are in saturation mode and M_7 and M_8 are operating in linear region. The current flowing is same that was in HCCM stage. Following current equation calculate the aspect ratios .

$$I_{5,6} = \mu C_{ox}\left(\frac{W}{L}\right)_{5,6} (V_{GS} - V_{Th})^2$$

Where $V_{GS} = V_{DD} - 3V_{Th,p}$

The M_5 and M_6 (cascode load) transistors characteristics are in deep linear region. The current equation is given as follows

$$I_{SS} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_{7,8} \left(2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right)$$

Where $V_{GS} \leq V_T$, $V_{DS}\ \phi\ V_{GS} - V_T$

6. CONCLUSION AND FUTURE SCOPE

The theoretical proposed design equation based procedure provides an effective and quick mechanism for estimating the MOS circuit parameters of operational amplifier. The performance requirements operational amplifier designed with these calculated procedure will able to satisfy the requirements to a good extent. The theoretical design equations highlighted the principal factors affecting the performance parameters, which made it very easy to redesign the circuit for different sets of specifications.

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