Study and Analysis of Two Partially Adiabatic Inverters (PADI)

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ABSTRACT

The dynamic power requirement of CMOS circuits is rapidly becoming a major concern in the design of personal information systems and large computers.
Battery operated portable computers and wireless communication products have often been used. Thus low power integrated circuit design has been strongly demanded for implementation. One of the promising techniques of low power design is adiabatic logic. Adiabatic means no exchange of energy with the environment. This paper compares between positive feedback adiabatic inverter (PFAL) and 2N2N2P adiabatic logic inverter.
The simulation is done using 0.35 TSMC CMOS technology.

KEYWORDS

Adiabatic, VLSI, PFAL, 2N2N2P, TSMC

INTRODUCTION

Moore's law describes the requirements of the transistors for VLSI circuits [1, 3]. The law gives an empirical observation about the component density and performance of integrated circuits. In recent years there is a huge demand for low power and low noise circuits. CMOS circuits is the heart of today's advanced device. The sources of power dissipation in a CMOS circuit are i) static power dissipation due to leakage current ii) dynamic power dissipation due to charging and discharging of load capacitance. iii) Short circuit power dissipation due to conducting of pull up and pull down network in saturation for a very short period of time.

In a CMOS inverter ½ cv^2 energy is lost in the pull up network during charging and the same amount of energy is lost during discharging in the ground. Energy saving can be obtained if the energy which is lost to the ground during discharging in a CMOS circuit is feedback to the supply voltage itself. If the recycling is done properly, then the efficiency of the logic circuits can be increased. This can be achieved by use of adiabatic logic circuits.

Adiabatic switching, which ideally operates as a reversible thermodynamic process, without loss or gain of energy. Adiabatic computation works by making very small changes in energy levels in circuits sufficiently slow, ideally resulting in no energy loss.

Fully adiabatic inverters can recover all the charges but they have very complex synchronization behavior. Partially adiabatic logic inverters are easy to implement.

In this paper we will compare two adiabatic inverters. They are PFAL inverter and 2N2N2P inverter.

In figure 1 and 2 we have given the basic charging and discharging technique of simple and adiabatic inverters.
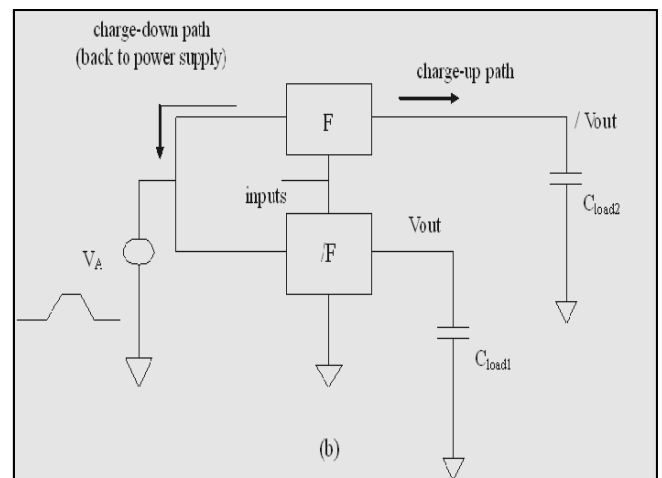

Fig1. Adiabatic inverter

The power supply used for adiabatic inverters are trapezoidal or sinusoidal voltage source. The voltage supply also acts as clock of the circuit [6].

ADIABATIC LOGIC

The word ADIABATIC comes from a Greek word that is used to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In real-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, one can achieve very low energy dissipation by slowing down the speed of operation and only switching transistors under certain conditions. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as energy recovery logic .

Adiabatic circuit design styles can be divided into two categories, semi or partially adiabatic circuits and completely adiabatic circuits. Partially adiabatic logics have some non adiabatic dissipation, while complete adiabatic or fully adiabatic logics do not have any non adiabatic dissipation.

Adiabatic circuits can use a diode-based configuration to reduce the power dissipation. The examples are 2N-2N2D , Adiabatic Dynamic Logic (ADL) , Improved Adiabatic and Dual-rail Adiabatic Pseudo-Domino Logic (DAPDL).Transistor based adiabatic logic styles dissipates energy essentially due to the threshold voltage drop across MOS transistors for the charging and discharging of the output nodes logic circuits belonging to this category are 2N-2P ,2N-2N2P Positive Feedback Adiabatic

Logic(PFAL),Pass-transistor Adiabatic Logic (PAL) ,Clocked Adiabatic Logic (CAL) and Improved Pass-Gate adiabatic Logic (IPGAL)[5,6].

Each adiabatic system consists of two main parts, the digital core design made up of adiabatic gates and the generator of the power-clock signals.
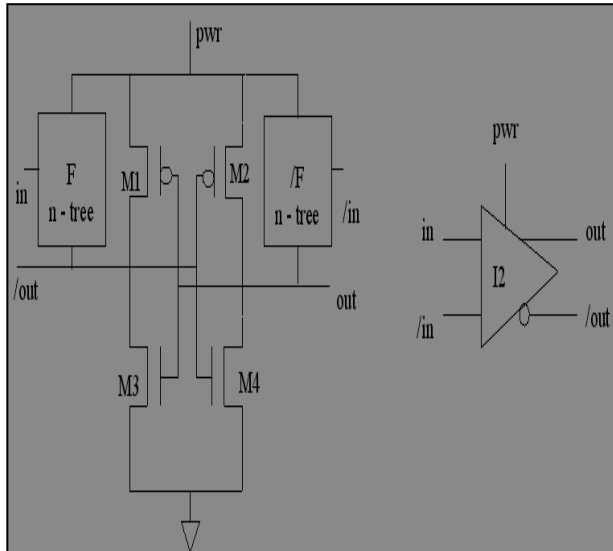

Fig2. PFAL inverter

PFAL inverter is made of a latch which consists of two PMOS transistors and two NMOS transistors.   The two n-trees are used to realize the logic functions. The functional blocks are parallel with the PMOS of the adiabatic amplifier [7, 8].

The power clock supply PC has a phase shift of 90° compared to the dual-rail encoded input signals in and compliment in. When the input signal in is low (compliment in is high), the output signal out follows the oscillating power clock supply PC where as compliment out stays at ground and vice versa.

The two major differences with respect to ECRL are that the latch is made by two PMOSFETs and two NMOSFETS, rather than by only two PMOSFETs as in ECRL logic, and that the functional blocks are in parallel with the transmission PMOSFETs. Thus the equivalent resistance is smaller in case of PFAL inverter [7, 8].

Use of MOSFET gives lowest power dissipation. We will show that among the adiabatic logic families PFAL gives largest energy saving with respect to static CMOS circuits [12].

The 2N2N2P logic is a partially adiabatic logic as PFAL logic. It has a pair of cross coupled NMOS transistors. These transistors help to get non floating output.

The primary advantage of PFAL over ECRL and 2N-2N2P is that the functional blocks are in parallel with the transmission pMOSFETs (see Fig. 3, right). Thus the equivalent resistance is decreased when the capacitance needs to be charged, leading to a reduction of the energy dissipation at high frequency.
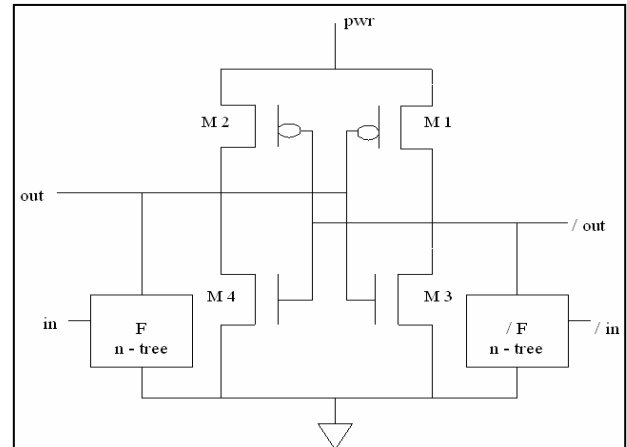

Fig3. 2N2N2P logic inverter

SIMULATION RESULTS

We have calculated the power dissipation in various frequencies using SPICE simulation tool. We have also calculated delay associated with various inverters in various frequencies. Next the power-delay product at various frequencies is calculated.

Inverters	Frequency		
	10MHz	100MHz	1GHz
2N2N2P	20 µW	45 µW	110 µW
PFAL	17 µW	36 µW	81 µW

Table 1: Comparison of power dissipation between adiabatic inverters

Inverter	frequency		
	10MHz	100MHz	1GHz
2N2N2P	1.2ns	2.9ns	4.9ns
PFAL	0.98ns	1.6ns	2.65ns

Table 2: Comparison of delay between adiabatic inverters

Inverter	frequency		
	10MHz	100MHz	1GHz
2N2N2P	24	130.5	539
PFAL	16.6	57.6	214.6

Table3: Comparison of Power-Delay Product between adiabatic inverters
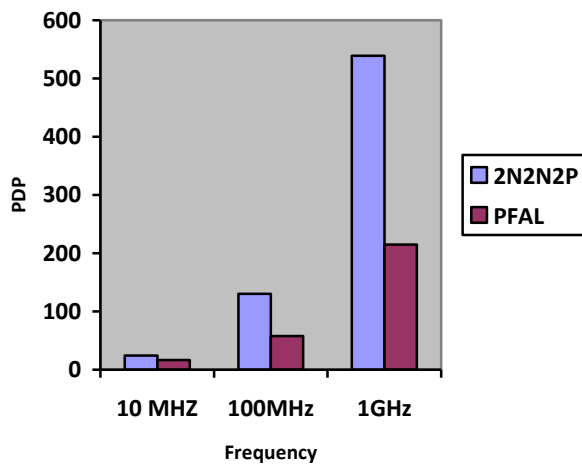
Comparison of PDP

Fig4. Comparison power delay product between 2N2N2P and PFAL adiabatic inverter

CONCLUSION

We have calculated PDP using the equation.PDP = Power dissipation (P_S) x Propagation delay (P_d) .PDP is measured using the unit energy consumed per switching event. PDP is also known as switching energy. From the simulation results it can be seen that PFAL inverter has less power dissipation compare to the 2N2N2P logic. It can also be seen that both the adiabatic logic styles require same number of transistors. We have also calculated the delays of the adiabatic inverters. PFAL shows lowest energy dissipation among adiabatic logic families based on cross-coupled transistors. It is also found that PFAL inverter has low power delay product.

ACKNOWLEDGEMENT

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