

# Frequency Compensation of Two Stage Op-Amp using Triode Mode Compensation Stage

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## Abstract

A frequency compensation technique for the improvement of unity gain bandwidth (UGB) and power supply rejection ratio (PSRR) of two stage operational amplifiers is presented in this paper. Performance of proposed op-amp is compared with classical miller compensated op-amp and op-amp proposed by G. Blakiewicz [13]. The technique exploits the triode mode operation of a MOSFET in the compensation stage which leads to the improvement in the UGB and Power Supply Rejection Ratio (PSRR). Small signal analysis for these parameters is carried out and theoretical improvements are verified through simulations in cadence VIRTUSO environment using UMC 0.18  $\mu\text{m}$  CMOS process technology.

## Keywords

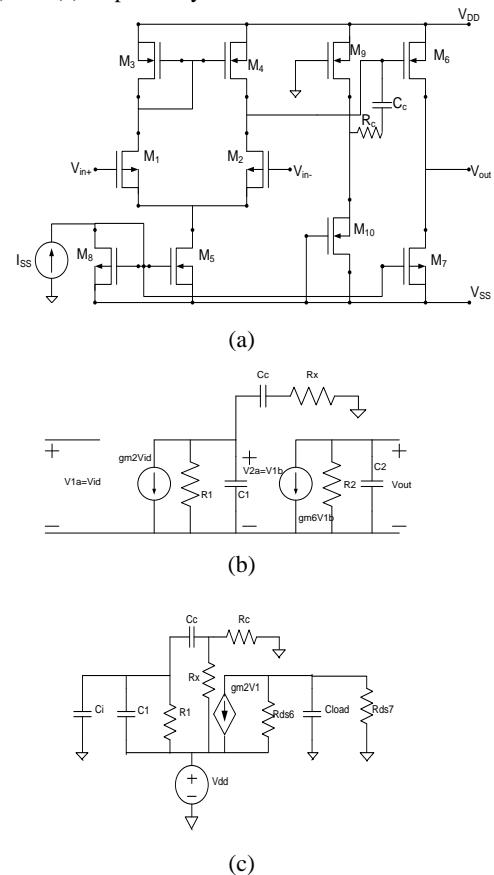
Miller compensation, triode mode MOSFET, unity gain bandwidth, Power supply rejection ratio, phase margin, Op-amp.

## 1. INTRODUCTION

Most integrated circuit realizations nowadays include both digital and analog functions, on the same chip. Most often, the analog blocks on the chip sense and get affected by the spikes on the ground and supply lines generated by the digital blocks. Coupling effects tend to deteriorate the dynamic range of high performance analog functions, so these effects need to be controlled and minimized [1]. The most important specification with this respect is the PSRR. The operational amplifiers (op-amps) are considered as important building blocks in mixed signal systems. The popular two stage operational amplifier shows a poor PSRR to supply voltage. At higher frequencies, the output drive transistor becomes 'diode connected' [2], with its drain ac shorted to its gate by the compensating capacitor which couples the supply signal to the output. It is seen mostly that the PSRR is degraded at higher frequencies due to the compensation circuitry [3-5]. A cascade technique was developed to overcome this drawback [6], [7] and was successful too but at the cost of reduction in common mode input range. Various techniques have been reported earlier from a voltage current buffer scheme to multipath compensation schemes [2], [8-12] which emphasize on a single effective low frequency dominant pole which provides a proper phase margin at the cost of  $-3$  dB bandwidth of open loop gain. In this paper the compensation technique reported in [13] is modified using a triode mode operating MOSFET in the compensation circuitry and a resistor in series with the compensation capacitor. The resulting topology offers higher UGB, PSRR and a suitable phase margin.

## 2. PROPOSED TECHNIQUE

The proposed technique takes an idea from [13] with a modification in the region of operation of the MOSFETS. The MOSFET of the compensation stage is operated in the triode region and a resistance is added in series with the compensation capacitor. The resulting circuit diagram, its small signal models for GB and PSRR are shown in Figure 1 (a), (b) and (c) respectively.



**Figure 1. (a) circuit diagram of the proposed structure, (b) small signal model for gain bandwidth calculation, (c) small signal model for PSRR calculation [2].**

The gain from the above model is found to be

$$\frac{V_o}{V_i} = \frac{R_1 R_2 g_{m1} g_{m2} (1 + s R_x C_c)}{(1 + s R_2 C_L) \{ (1 + s R_1 C_1) (1 + s R_x C_c) + s C_c R_1 \}} \quad (1)$$

This gives the poles as

$$P_1 = 1/R_1 C_c (R_x/R_1),$$

$$P_2 = 1/R_x C_l, \quad P_3 = 1/R_x C_1, \quad (2)$$

$$PSSR_{\text{dominant}}^+ = 1/R_1 (C_c + C_i + C_1) + R_x C_c$$

The UGB comes out to be

$$UGB = \sqrt{\frac{gm_1 gm_2}{(R_x/R_1) C_c C_l}} \quad (3)$$

Comparing the dominant pole  $P_1$  and UGB frequency to those derived in [13] we see that the DC voltage gain of the compensation stage ( $A_c$ ) is replaced by  $(R_x/R_1)$ , the latter being less than 1, ( $A_c$  was set around 10) which in turn increases the dominant pole frequency and the GB.  $R_x$  here is the triode resistance of the MOSFET  $M_8$  and  $R_1$  is the output resistance of the first stage. The ratio  $(R_x/R_1)$  being less than one and in the denominator increases the magnitude of the whole fraction. The above PSRR dominant pole position when compared to the equation from [13] through simulations we find out that the modified circuit has a high dominant pole frequency which increases the bandwidth for high PSRR.

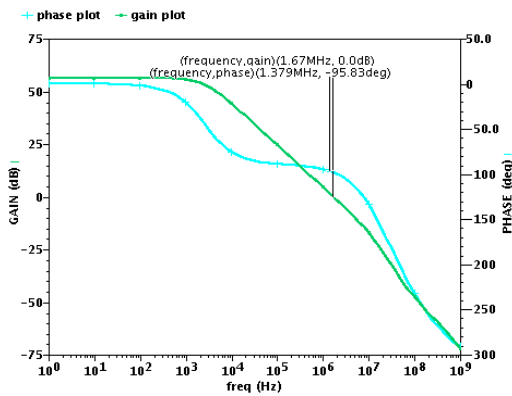


Figure 2 (a) Gain and phase vs frequency for classical miller compensated op-amp

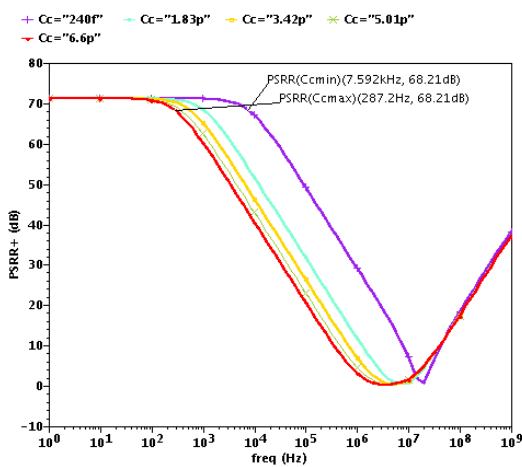


Figure 2 (b) PSRR+ vs frequency for classical miller compensated op-amp for different values of  $C_c$

### 3. SIMULATION RESULTS

The circuits are simulated in cadence VIRTUSO environment using UMC 0.18  $\mu\text{m}$  CMOS process with dual power supply of  $\pm 1.8$  volts. Three operational amplifiers were designed: 1) classical miller compensated, 2) as given in [13] and 3) using proposed technique. Simulations for UGB and PSRR are carried out for a range of capacitive loads from 1 pf to 30 pf which gives the  $C_c$  as 24 pf to 6.6 pf.

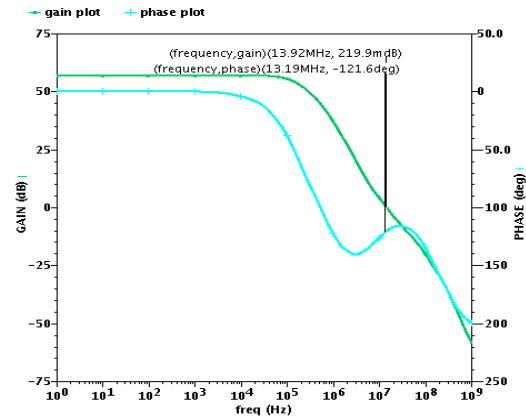


Figure 3 (a) Gain and phase vs frequency for op-amp reported in [13]

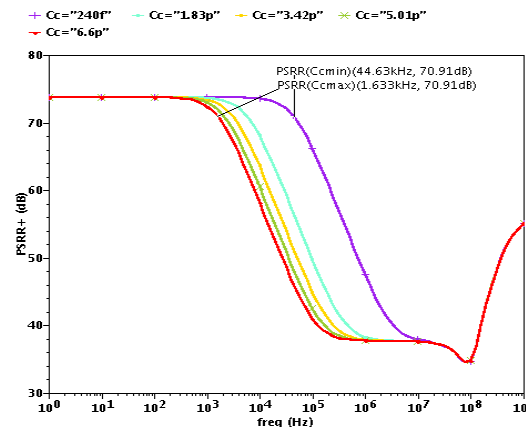


Figure 3 (b) PSRR+ vs frequency for op-amp reported in [13] for different values of  $C_c$

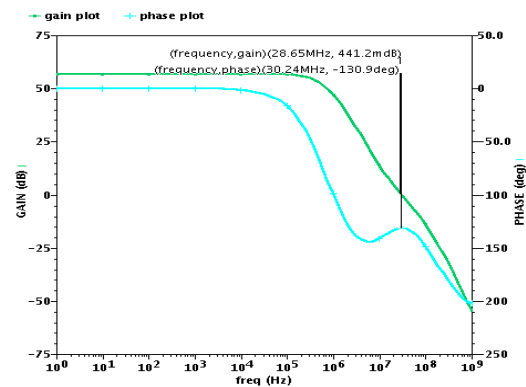
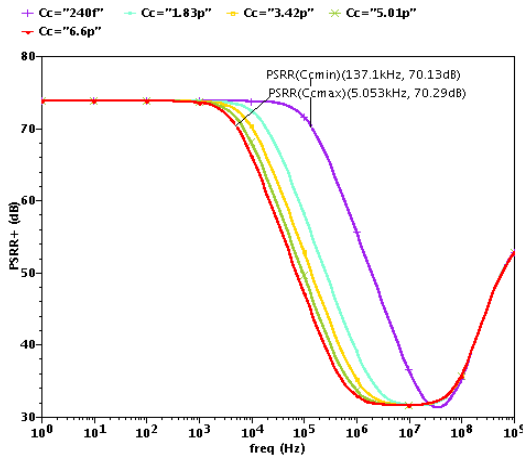


Figure 4 (a) Gain and phase vs frequency for proposed op-amp



**Figure 4 (b) PSRR+ vs frequency for proposed op-amp for different values of Cc**

Plots for gain and phase vs frequency-applying load of 10 pf in 1) classical miller compensated, 2) as given in [13] and 3) using proposed technique are given in Figure 2 (a), Figure 3 (a) and Figure 4 (a) respectively. Similarly, plots for PSRR vs frequency for  $C_c$  varying between 24 pf to 6.6 pf are obtained as given in Figure 2 (b) (classical miller compensated), Figure 3(b) (reported in [13]) and Figure 4(b) (proposed). Significant improvement in the unity gain frequency and the PSRR for wide bandwidth was noted for the proposed technique which varies as an inverse function to the  $C_c$ . The improvement is noted at the cost of degraded phase margin at higher capacitive loads which renders the system marginally stable for those loads. Result summary is presented in Table 1.

**Table 1. Results Summary**

Performance Parameters	Op-amp			
	Classical miller compen.	Reported in [13]	proposed	
DC voltage gain in dB	60 dB	60 dB	60 dB	
Power consum.	1240 $\mu$ w	512 $\mu$ w	512 $\mu$ w	
Area occupied	3700 $\mu$ m <sup>2</sup>	1875 $\mu$ m <sup>2</sup>	1915 $\mu$ m <sup>2</sup>	
Compen. Cap	4 pf	0.25 pf	0.25 pf	
-3 dB reduction in PSRR	7.594 KHz	44.77 KHz	124.2 KHz	
$C_L = 5$ pf	GB	1.59 Mhz	24.2 Mhz	48.1 Mhz
	Phase	86.0 deg	67.6 deg	47.6 deg
$C_L = 10$ pf	GB	1.64 Mhz	14.0 Mhz	30.0 Mhz
	Phase	83 deg	60.3 deg	49.2 deg
$C_L = 20$ pf	GB	1.57 Mhz	8.28 Mhz	18.7 Mhz
	Phase	77 deg	47.7 deg	44.7 deg
$C_L = 30$ pf	GB	1.57 Mhz	6.53 Mhz	13.9Mhz
	Phase	70 deg	44 deg	40 deg

## 4. CONCLUSION

The technique described above is applicable to most of the op-amp configurations and its effectiveness with the classical circuit has been verified theoretically as well as experimentally. A significant improvement in bandwidth for high PSRR and UGB is found with an optimization in the chip area.

## ACKNOWLEDGEMENT

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## REFERENCES

- [1] Willy M.C.Sansen, "Analog design Essentials" (Published by Springer, PO Box 17, 3300 AA Dordrecht, The Netherlands).
- [2] Ribner D.B., Copeland M.A. "Design techniques for cascoded CMOS op-amps with improved PSRR and common-mode input range", IEEE J. Solid-State Circuits, 1984, 19, pp. 919–925M.
- [3] Steyaert M.S.J., Sansen W.M.C. "Power supply rejection ratio in operational transconductance amplifiers", IEEE Trans. Circuits Syst., 1990, 37, (9), pp. 1077–1084.
- [4] Sackinger E., Goette J., Guggenbuhl W. "A general relationship between amplifier parameters, and its application to PSRR improvement", IEEE Trans. Circuits Syst., 1991, 38, (10), pp. 1173–1181
- [5] Allen P.E., Holberg D.R. "CMOS analog circuit design" (Oxford University Press, New York, 2002, 2nd edn.), Ch. 6.4
- [6] R. D. Jolly and R. H. Mc Charles, "A low-noise amplifier for switched-capacitor filters," IEEE J. Solid-State Circuits, vol. SC-II, pp. 1192–1194, Dec. 1982.
- [7] D. J. Allstot and W. C. Black Jr., "Technological design considerations for monolithic MOS switched-capacitor filtering systems," I'proc. IEEE, vol. 71, pp. 967-986, Aug. 1983.
- [8] Ahuja B.K., "An improved frequency compensation technique for CMOS operational amplifiers", IEEE J. Solid-State Circuits, 1983, 18, (6), pp. 629–633.
- [9] Aloisi W, Palumbo G., Pennisi S. "Design methodology of Miller frequency compensation with current buffer/amplifier", IET Proc. Circuits, Devices Syst., 2008, 2, (2), pp. 227–233
- [10] Hurst P., Lewis S., Keane J., Aram F., Dyer K. "Miller compensation using current buffers in fully differential CMOS two-stage operational amplifiers", IEEE Trans. Circuits Syst. I, 2004, 51, (2), pp. 275–285
- [11] Leung K.N., Mok P.K.T., Ki W.H., Sin J.K.O. "Three-stage large capacitive load amplifier with damping-factor-control frequency compensation", IEEE J. Solid-State Circuits, 2000, 35, (2), pp. 221–230
- [12] Leung K.N., Mok P.K.T. "Analysis of multistage amplifier frequency compensation", IEEE Trans. Circuits Syst. I, 2001, 48, (9), pp.1041–1056.
- [13] G. Blakiewicz, "Frequency compensation for two-stage operational amplifiers with improved power supply rejection ratio characteristic" . IETCircuits, Devices & Systems doi: 10.1049/iet-cds.2010.0059 IS