Testing the Effect of different Switch Box Architectures on Detailed Routing in FPGA

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ABSTRACT

FPGA detailed routing problem is an interesting problem in VLSI field because of the limited routing resources in island style FPGA architectures. In this paper, the effectiveness of various switch boxes (Subset, Wilton and Universal) in FPGA detailed routing has been tested using a Boolean satisfiability (SAT) based approach. A SAT instance is formulated for each routing problem and routability is tested using a back-end SAT solver. The performances of different switches have been tested and compared in terms of routability and minimum channel width.

Keywords

FPGA, Switch Box, Detailed routing, Satisfiability

1. INTRODUCTION

FPGA detailed routing problem is an interesting design problem because of the limited routing resources in island style FPGA architectures. Several algorithms have been tested for solving this problem. The "net at a time" approach is a sequential approach where nets are routed one by one. Each individual net of a circuit is laid down separately. However, selection of nets may introduce a net ordering problem, because invalid sequence of net selection may identify a routable circuit as unroutable. Algorithms based on the concurrent approach consider all nets of a circuit simultaneously for routing. A negotiation-based performance driven routing for FPGAs is presented in [11]. An integrated method for placement and routing is presented in [9]. VPR [3] is very popular FPGA routing tool. In terms of minimizing routing area, VPR outperforms all published FPGA place and route tools. Although the algorithms used are based on previously known approaches, they presented several enhancements that improve run-time and quality. The current VPR versions can work on heterogeneous FPGAs also. ROAD and ROAD-HOP [1, 2] are the detailed routers that explore the solution space using Bump-and-Refit (B & R) approach. All these algorithms belong to the group of sequential routing methods (net-at-a-time).

The other set of algorithms which consider all nets simultaneously provide good results, since all possible paths are explored simultaneously. Boolean satisfiability (SAT) based detailed routing is an interesting approach that makes it possible to consider all nets concurrently. In this approach the FPGA detailed routing problem is converted into a series of constraints which are expressed as a single Boolean function. This function is then solved by any available SAT solver like GRASP [10], RelSAT [8], SATO [20], Zchaff [19] etc. Any valid assignment of the Boolean variables which satisfies the function expresses valid routability. SAT provides not only valid solution for the problem; it searches all possible paths for complete routing solution. If it is unable to find a solution, it proves that the circuit is unroutable which a sequential method does not provide.

Devadas was the first to reformulate a routing problem as an equivalent SAT problem [5]. Wood and Rutenbar [17] used Binary Decision Diagrams (BDDs) [4] for channel routing in FPGAs. In [12] authors have proposed a "route-based" FPGA detailed routing approach using Boolean SAT, which shows a performance improvement over a previously proposed "track-based" approach. An extension of the classical 2-layer routing in [5] for segmented channel routing using SAT for row based FPGAs was proposed in [7]. In [15], the authors propose SAT based methodology for detailed routing using the graph colouring approach.

In all the above cases, routing has been done on two-pin nets for simplicity and ease of modeling. Multi-terminal nets of a circuit are decomposed into two-pin nets before formulating the problem. Except VPR all other algorithms mentioned above find routing solution for the FPGAs with Subset switching structure. [14] presents a satisfiability based method for solving the board-level multi-terminal net routing problem in the digital design of clos-folded FPGA based logic emulation systems.

In this paper we have tested the effectiveness of different switching structures in FPGA routing. The proposed method works on multi-pin net structure without decomposing nets into two-pin nets. Multi-pin net routing implicitly removes pin dogleg problem [3, 6] without requiring any extra constraint for it. A track-encoding technique is used to formulate the routing problem into equivalent SAT problem on different switching architectures.

We have formulated our detailed routing model based on the standard island style FPGA architecture layout [18, 3] with a two dimensional array of configurable logic blocks (CLBs), connection blocks (CBs) and switching blocks (SBs). Three parameters channel width (W) i.e. the number of tracks in a channel, connection block flexibility ($F_C \leq W$) i.e. the number of tracks that each pin may connect to, and switching block flexibility (F_S) i.e. the number of other tracks that each wire segment entering an SB can connect to, define the routing capacity of the given FPGA architecture. The restrictions on the values of F_C and F_S makes the detailed routing problem more complex. In other words the architectures of CBs and SBs directly affect the solution of the routing problem or more specifically, affect the minimum number of tracks, required for complete detailed routing.

The next section describes the routing with different switch boxes for detailed routing in FPGAs. Section 3 gives details
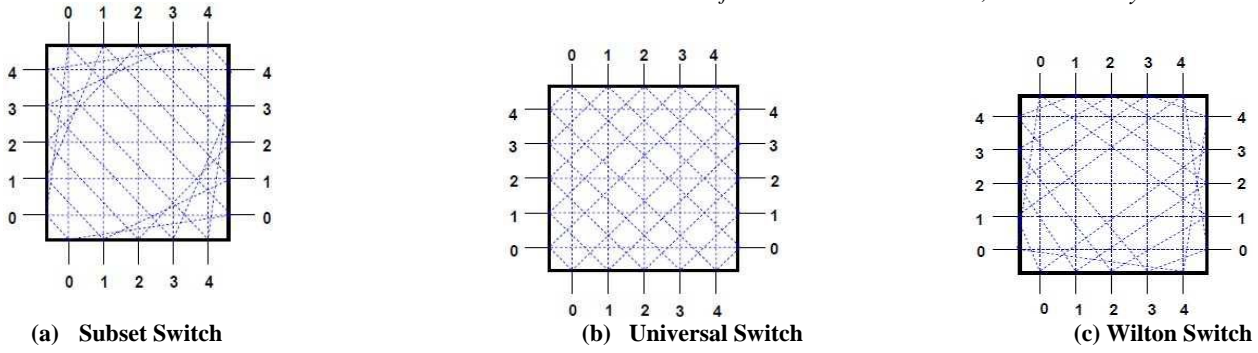
| (a) Subset Switch | (b) Universal Switch | (c) Wilton Switch |

Fig 1: Switch box architectures

of our experiments and the results obtained with benchmark circuits. Section 4 concludes the paper.

2. ROUTING WITH SUBSET WILTON AND UNIVERSAL SWITCHES

In this paper, SAT based detailed routing of multi-pin nets has been proposed with different switching structures. The two fundamental detailed routing constraints: 1) each net should be assigned to any specific track in their respective channels and 2) any two electrically distinct nets sharing common routing area should not be assigned to same track in that area, must be maintained by all routing solutions.

Track encoding is the technique which has been applied here to convert the routing problem into equivalent SAT (decision) problem. In this technique, each detailed routing constraint is represented by a set of CNF (Conjunctive Normal Form) clauses. The conjunction of all these clauses for all constraints generates an atomic Boolean function which implicitly represents routing problem as a SAT problem. Further this function is solved by any powerful SAT solver available and the result of the solver says the circuit is routable if the result is "satisfied" otherwise unroutable in that specified architecture. The constructions of CNF clauses and the Boolean function totally depend on the specified routing architecture i.e., the channel width (W), connecting block flexibility (F_C) and switching block flexibility (F_S). In this paper we have considered $F_C = W$ and $F_S = 3$. The W is assigned different values at different instance for constructing distinct SAT functions for getting minimum channel width which makes the circuit routable.

The algorithm behind the technique creates a distinct track-variable for each distinct segment of the nets. The domain of values of each variable is $\{0, 1, 2, ... (W − 1)\}$. The values in this domain define the track indices. Consequently each track-variable is encoded by $\lceil \log(W) \rceil$ Boolean variables. The routing rules defined above are covered by three disjoint constraints.

1. **Track Assignment**: It ensures that a net would be assigned to any of the available track in a channel.
2. **Switching**: It guarantees that a net running through one channel can switch to any other adjacent channel.
3. **Exclusivity**: It restricts two nets which are sharing common connecting block from being assigned to same track in that connecting block.

A track assignment constraint is created for each multi-pin net for the segment of the net which has the "source" pin connected with it. It can be defined by equation (1).

$$(t_{ij} = 0 \vee t_{ij} = 1 \vee \cdots \cdots \vee t_{ij} = W - 1) \tag{1}$$

Where t_{ij} is the track-variable for the jth segment of net i.

The switching constraint is the main focus in this paper. The formulation of the routing problem is greatly influenced by the switching structure. For various switching block structure the form of the switching constraint is different. This constraint defines a net assigned to one particular track in a channel, which track it will be assigned to after switching in its next adjacent channel. For one multi-terminal net more than one switching constraints are formulated if the net has more than one switching in its length.

The internal structure of a *subset* switch is shown in figure 2(a). The internal structure of this switch impels the net segments to be placed in the same track index in different channels. The formulation of switching constraint for this switch can be expressed by equation (2) using track variables.

$$t_{ij} = t_{ik} \tag{2}$$

where t_{ij} and t_{ik} are track-variables for the jth and kth segments of net i and the net is switched from segment j in one channel to segment k in another channel.

The *Wilton* switch has a different type of structure. The figure in 2(c) shows the structure which allows segments of a net to be assigned to different tracks in their respective channels. The switching constraints for this switch are formulated based on equation (3).

$$\begin{aligned}
\vee_i^{W-1} \{ &(t_{0,i} \wedge t_{2,i}) \vee (t_{1,i} \wedge t_{3,i}) \vee (t_{0,i} \wedge t_{1,(W-i) \bmod W}) \\
&\vee (t_{1,i} \wedge t_{2,(i+1) \bmod W}) \vee (t_{2,i} \wedge t_{3,(2W-2-i) \bmod W}) \vee \\
&(t_{3,i} \wedge t_{0,(i+1) \bmod W}) \}
\end{aligned} \tag{3}$$

Where $t_{m.n}$ track incidence, m is the switch block side within ($0 \leq m \leq 3$) and n is the track number within the range ($0 \leq n \leq W − 1$) shown in figure 2.

The switching constraints using track-variables for the universal switches can be constructed according to the expression in equation (4).
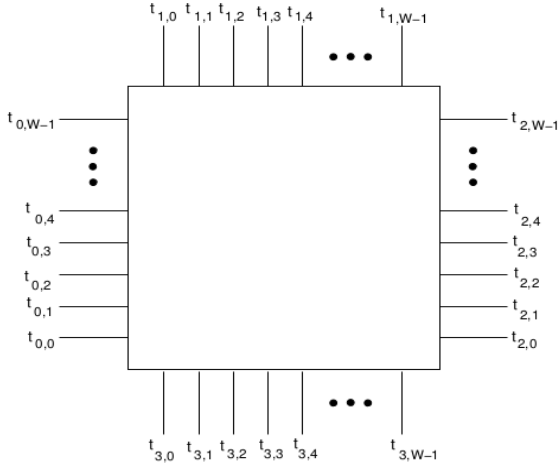
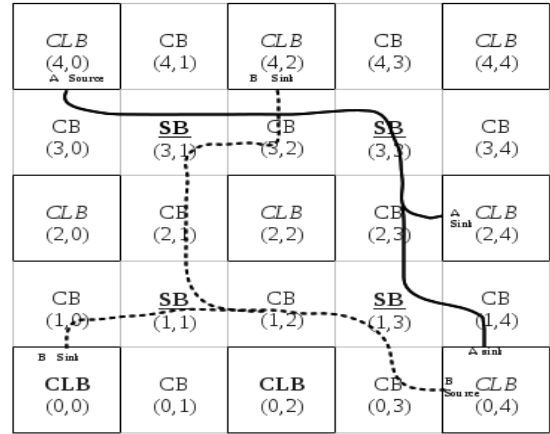**Fig 2: Generalized switch block diagram with track indices.**

Fig 3: Two nets A and B globally routed through various CBs (Connecting Blocks) and SBs (Switching Blocks). A net has one "source" and multiple "sink" attached to CLBs (Configurable Logic Blocks).

$$\bigvee_{i}^{W-1}\{(t_{0,i} \wedge t_{2,i}) \vee (t_{1,i} \wedge t_{3,i}) \vee (t_{0,i} \wedge t_{1,(W-i-1)\bmod W})$$
$$\vee (t_{1,i} \wedge t_{2,i}) \vee (t_{2,i} \wedge t_{3,(W-i-1)\bmod W}) \vee (t_{3,i} \wedge t_{0,i})\}$$

(4)

For all types of architectures the exclusivity constraint for any pair of net segments sharing common connecting block can be expressed by the expression below.

$$t_{ip} \neq t_{jq} \qquad (5)$$

Where t_{ip} and t_{jq} are track-variables for p segment of net i and q segment of net j residing in same connection block respectively. The formulations of all types of constraints can be clearly explained by example (1) for the small given routing problem in figure 3.

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Example 1: In the figure 3 two multi-terminal nets A and B are routed by global router in the specified channels. Table 1 shows the various segments of the nets and the corresponding track-variables created for them. The track assignment constraints for net A and B are expressed as

$$t_{A0} = 0 \vee t_{A0} = 1 \vee t_{A0} = 2 \vee t_{A0} = 3 \vee t_{A0} = 4 \qquad (6)$$
and
$$t_{B0} = 0 \vee t_{B0} = 1 \vee t_{B0} = 2 \vee t_{B0} = 3 \vee t_{B0} = 4 \qquad (7)$$

SB(3,1) describes best the switching constraints for different switch blocks for the given problem. Net B has made a switching at SB(3,1) from CB(2,1) to CB(3,2). To show the differences in the formulations of the switching constraints for different switching structures we take only one switch block SB(3,1) as a sample. The formulas for the net B at switch SB(3,1) for different switches are as follows:

Subset Switch:

$$t_{B3} = t_{B4} \qquad (8)$$

Wilton Switch:

$$(t_{B3} = 0 \wedge t_{B4} = 3) \vee (t_{B3} = 1 \wedge t_{B4} = 2) \vee$$
$$(t_{B3} = 2 \wedge t_{B4} = 1) \vee (t_{B3} = 3 \wedge t_{B4} = 0) \vee \qquad (9)$$
$$(t_{B3} = 4 \wedge t_{B4} = 4)$$

Table 1: Track-Variables and Boolean variables needed for the multi-pin nets shown in Fig. 3

Net	Segment	Span	Track Variable
A	0	CB(3,0)–CB(3,2)	t_{A0}
	1	CB(2,3)–CB(2,3)	t_{A1}
	2	CB(1,4)–CB(1,4)	t_{A2}
B	0	CB(0,3)–CB(0,3)	t_{B0}
	1	CB(1,2)–CB(1,0)	t_{B1}
	2	CB(2,1)–CB(2,1)	t_{B2}
	3	CB(3,2)–CB(3,2)	t_{B3}

Universal Switch:
$$(t_{B3} = 0 \wedge t_{B4} = 4) \vee (t_{B3} = 1 \wedge t_{B4} = 3) \vee$$
$$(t_{B3} = 2 \wedge t_{B4} = 2) \vee (t_{B3} = 3 \wedge t_{B4} = 1) \vee \qquad (10)$$
$$(t_{B3} = 4 \wedge t_{B4} = 0)$$

The exclusivity constraint is formulated at the common area CB (3, 2) where nets A and B both are running through. Switching blocks do not have any effect on this constraint. This constraint at that connecting block can be expressed as

$$t_{A0} \neq t_{B4} \qquad (11)$$

∎

All the above formulations have been constructed on the track-variables. But ultimately these track-variables are encoded by Boolean variables and the constraints are represented in terms of Boolean expressions. Finally, the Boolean expression is converted into conjunctive normal forms (CNF) and the conjunction of all the CNFs gives a single Boolean function which represents the routing problem as a decision problem. To convert the routing problem into equivalent SAT problem, one particular routing architecture is considered i.e.

Table 2: Minimum Channel Width Required for Detailed Routing with Different Switching Architectures.

Circuit	Subset	Wilton	Universal[16]
9sym	7	5	7
9symml	8	6	7
apex7	5	4	5
alu2	9	8	8
C499	8	6	7
C880	8	7	8
C1350	7	6	7
example2	7	5	6
term1	6	5	6
too-lrg	9	8	9
vda	11	9	10
k2	12	9	11
e64	10	8	8
misex3c	9	8	8

predefined channel width, connecting and switching block flexibilities, and particular switching block structure.

3. EXPERIMENTAL RESULT

In this section, we have experimentally tested the effectiveness of the different switching structure on FPGA detailed routing using multi-pin net track encoding formulation. The experiments are implemented on standard MCNC benchmark circuits [14]. We have used VPR [3] for placement and global routing for all the circuits. The technique described in this paper is conducted using C and the Zchaff solver [19] is used as the underlying SAT solver. All experiments were conducted on Core2Duo Fedora 12 system with 2 GB RAM. During the formulation of our techniques, different SB architectures have been targeted on island style FPGAs.

Using the global routing solution generated by VPR a single Boolean function is formulated in case of all the switching block architectures based on "net to track assignment" of multi-pin nets. This Boolean function is subsequently evaluated by the Zchaff SAT solver on decreasing values of channel width W with starting value obtained from VPR global routing information. The detailed routing constraints for technique (Multi-Pin Net Track Encoding) discussed in this paper are represented as a series of CNF clauses and the conjunction of clauses generates a single Boolean function which completely represents the routing problem as a SAT problem. The CNF clauses or the entire Boolean function is constructed based on the FPGA architecture with $F_S = 3$ and

$F_C = W$.

Results of the detailed routing solutions obtained are shown in Table 2. In the table, minimum channel width required for complete detailed routing are listed for various circuits on different switching structures. For every switch, switching block flexibility is 3, but routing solutions are different. Routing solutions with "Wilton switch" gives better result than other two switches and "Universal switch" is better than "Subset switch" for some circuits. The difference in result is due to the overall flexibility of switches. "Subset switch" is more restricted than other two switches. It restricts all segments of a net to be assigned to the same track for entire

span of the net in different channels. But "Universal switch" is sometimes relaxed in internal architecture than "Subset". The "Wilton switch" is more relaxed than all other switches and hence it provides better result in all aspects of detailed routing solutions.

4. CONCLUSION

This paper introduces SAT based formulations for FPGA detailed routing on three different switching architectures for multi-pin net structures. The solutions obtained show the routing capability of different switch boxes in terms of routabily and minimum channel width. The Wilton switch gives the better results than other two switching types owing primary to its greater flexibility.

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