Design of Ultra Low Power LC VCO in 45 nm Standard CMOS Process

Anindita Sahu
School of Electronics Engineering
KIIT University
Bhubaneswar, India

Sushanta K. Mandal
School of Electronics Engineering.
KIIT University
Bhubaneswar, India

ABSTRACT
This work presents design of a fully integrated Voltage Control Oscillator (VCO) implemented in 45 nm standard CMOS process. The designed LC VCO operates at 9.06 GHz with 634.28µW power consumption from 1 V supply. The design achieves phase noise as -97.48dBc/Hz at an offset of 1MHz and the figure of merit (FOM) of the LC-VCO is calculated as -178.60dBc/Hz for the un-buffered VCO. For buffered VCO the phase noise becomes -97.69dBc/Hz at an offset of 1MHz and the FOM is -178.81dBc/Hz.

General Terms
Radio frequency integrated circuit design

Keywords
RF IC, LC VCO, CMOS process, low power

1. INTRODUCTION
The rapid growth in wired and wireless communication has raised an increasing demand for smaller, low cost, low power and low noise devices. Radio frequency integrated circuit (RFIC) which was often used in military & cable TV in the past are now heart of every communication industry. In such applications replacing the battery frequently is not realistic; hence the power consumption of the whole system must be extremely small so as to maximize the battery life. The fully integrated system on chip (SOC) has continuously driven down the manufacturing costs. The low cost results the ultimately improves the consumer demand.

The increasing demand for wireless communication motivates the growing interest in personal communication trans-receiver. A fully integrated trans-receiver is an effective element for providing high-speed wireless communication network. The fully integrated voltage controlled oscillator (VCO) is one of the most important building blocks in a trans-receiver system [1-5].

An important building block of a RF system is the local oscillator (LO), which is usually implemented as a VCO inserted in a phase-locked-loop (PLL). Oscillators are autonomous systems that require no external excitation to produce a periodic output, when a phase-locked mechanism is provided; a stable frequency can be generated. Using mixers, the stable frequency can translate data to a desired intermediate frequency in Transreceivers, as well as it can generate precise clock signals that trigger events in digital circuits. Due to its low noise and low power capability and its easy on chip integration, the LC-VCO topology has been extensively used in RF applications.

2. VCO DESIGN
2.1 Basic Concept
The first step in designing an oscillator is to choose a circuit topology or type. A conventional balanced NMOS LC-VCO is shown in Fig 1. The circuit shows poor performance due to several losses associated with it. These losses are due to passive inductor, capacitor and the MOSFETs (Mn1, Mn2: the active devices). On-chip spiral inductors have low quality factor that dominates the losses of the LC tank [6-8].

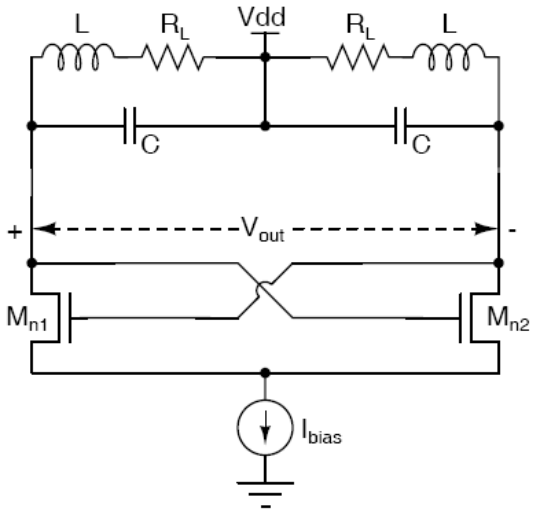

Fig 1: Balanced NMOS LC-VCO

2.2 Varactor Structure
The starting point for this design was a tank circuit with C = 0.032 pF and L = 8 nH which resonates near 10 GHz. The total tank capacitance is comprised of the variable tuning capacitance (varactors) and parasitic capacitances. The tuning capacitance is implemented in a differential fashion by connecting two identical PMOS varactors in series as shown in Fig 2. This gives the tank varactor capacitance value as half of the individual varactors. For a balanced circuit it creates a virtual ground at the common node. The tuning voltage is applied at this node through a resistor. Because of the virtual ground, the differential varactor connection does not require AC currents to flow into the bulk.

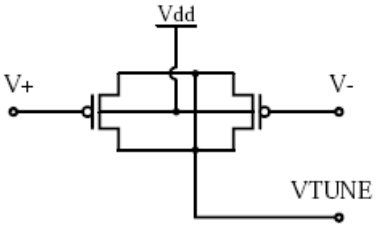

Fig 2: Series Varactor Connection

A 32 fF capacitor could conceivably be implemented in this process using a PMOS transistor that is 14.8 µm in length and width. However, such an implementation would have very poor performance since the resistance of the channel (R_{ch}) and the gate (R_g) would be excessive. The MOS varactors for the VCO design were realized using the minimum gate length allowed in the process (45nm). Each of the two series varactor consist of three parallel devices with 10 fingers each with W=4.2µm and L=45nm. Fig 4 shows a plot of the simulated total varactor capacitance (i.e. the series combination of Fig 2) versus the control voltage. This C-V curve was generated using a transient simulation in Spectre.

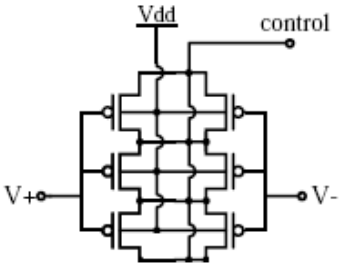

Fig 3: Varactor implementation structure

The tuning voltage was varied over a number of simulation runs and the capacitance was calculated from the displacement current through the varactors for each run. The C-V Curve is shown in the Fig 4. It has been achieved by doing the parametric analysis and simulated using Spectre.

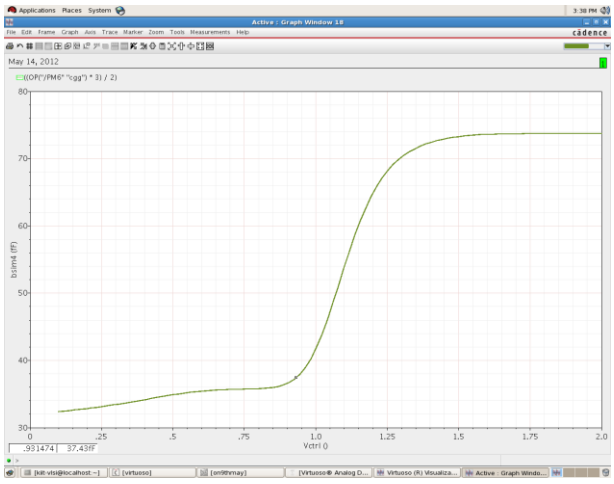

Fig 4: Simulated total Tank capacitance vs. control voltage

The tuning curve of the VCO is determined by these large-signal average capacitance plots shown in Fig 4. Fig 5 shows the tuning curve of the -G_m VCO using the inversion mode capacitance value. Here the Varactor has the tuning range of 1.64GHz. I-MOS can be operated at higher frequencies. The tuning range of an oscillator can be calculated as

$$\text{Tuning Range} = \frac{2(f_{max} - f_{min})}{(f_{max} + f_{min})} \times 100\%$$

The tuning range obtained in this thesis is 1.64GHz (19.47%). The amplitude of the oscillations did not vary significantly over the tuning range.

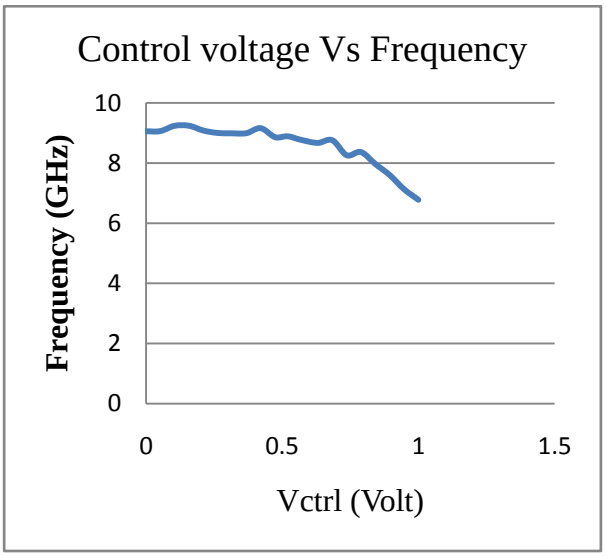

Fig 5: Control voltages Vs Frequency of oscillation

2.3 Oscillator Design

The inductor assumed in this design is a loss less inductor and the inductance value taken for the design is L=8 nH. The varactor taken in this design is a PMOS varactor with capacitance value C=32fF.

As extracting the oscillator output directly into 50 Ω test equipment, it would severely load the oscillator. The output of the oscillator must be presented with high impedance. This can be achieved in two different approaches. The first approach involved using a resistive divider to extract the signal. In this case a 1KΩ resistor is connected in series with each of the output. This method of extracting the oscillator signal will be referred to as the un-buffered case. The complete un-buffered VCO design is shown in the Fig 6.

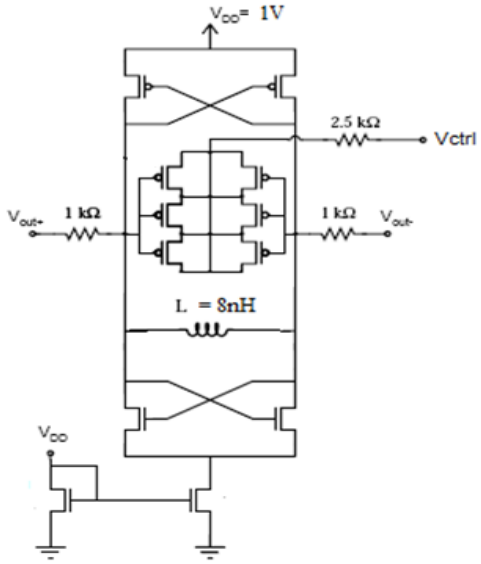

Fig 6: Complete Un-buffered VCO

The other approach to present high impedance to the oscillator output through the use of an active buffer circuit. The complete buffered VCO circuit is shown in Fig 7. This circuit provides low phase noise.

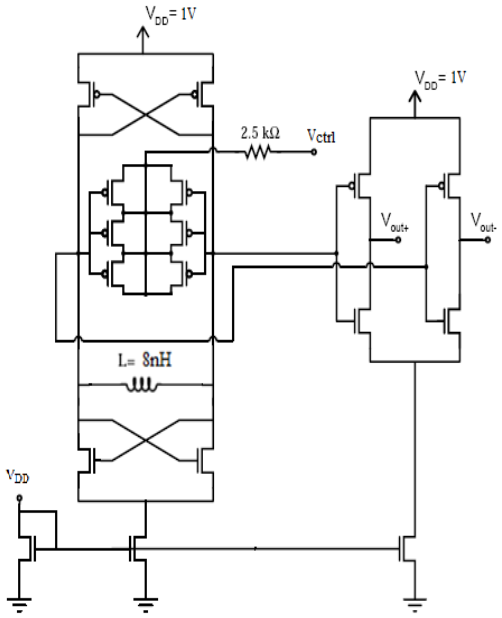

Fig 7: Complete Buffered VCO

3. SIMULATED RESULTS

The oscillators of this thesis were simulated using Spectre. Spectre is a SPICE like software package integrated into the Cadence IC design system. This design has been done in 45nm CMOS process technology.

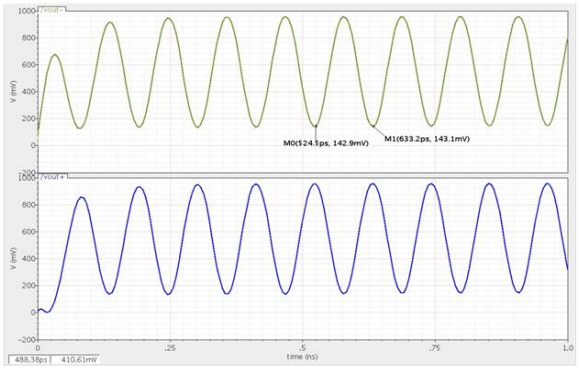

Fig 8: Oscillator outputs V_{out}+ and V_{out}-

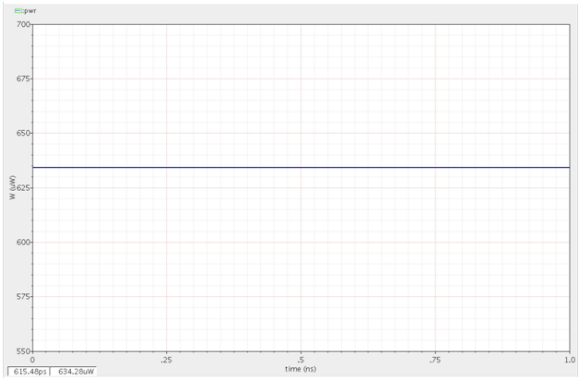

Fig 9: Power dissipation of the circuit

The circuit provided with supply voltage of 1V.The power consumption of the total circuit is 634.28µW shown in the Fig 9.The current of the circuit can be calculated as

$$P_{dissipation} = V_{supply} I_{bias}$$

$$I_{bias} = \frac{P_{dissipation}}{V_{supply}} = \frac{634.28\mu W}{1V} = 0.634mA$$

While these transient simulations are useful for evaluating oscillator parameters, they tell the designer very little about the phase noise performance of the circuit. The Spectre circuit simulator can simulate phase noise, using a periodic steady-state approach.

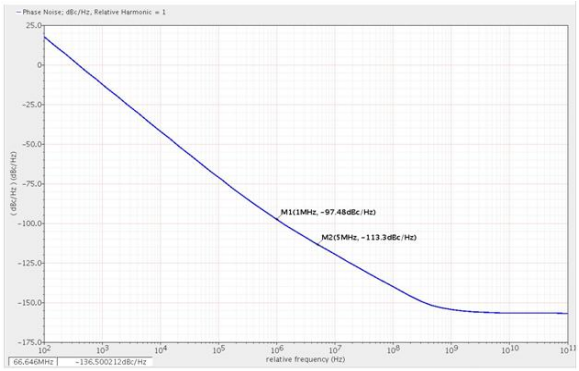

Fig 10: Phase noise analysis curve of un-buffered VCO

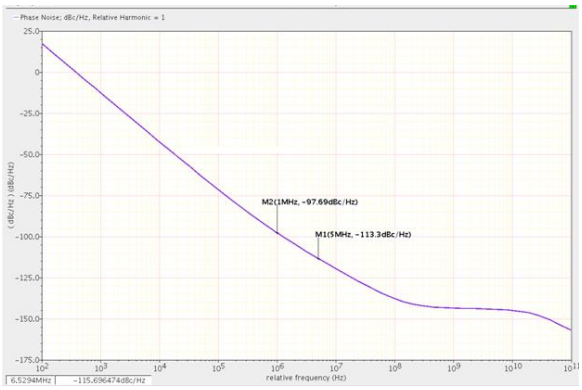

Fig 11: Phase noise analysis curve of Buffered VCO

4. CONCLUSIONS

The goal of this research was to create wireless system-on-a-chip. To this end an RF VCO was implemented in a digital CMOS process technology. It is very difficult to achieve all the better parameter values for a design, so we have to compromise with some parameter values. The figure of merit has been calculated by using the formula

$$VCO_{FOM} = L(f_{offset}) - 20\log\left(\frac{f_{osc}}{f_{offset}}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right)$$

The buffered oscillators had a tendency to drift more than the un-buffered oscillator. Phase noise achieved by the buffered VCO is better than that of the un-buffered VCO. The FOM of the un-buffered VCO is obtained as VCO_{FOM} = -178.60 dBc/Hz. The FOM of the buffered VCO is obtained as VCO_{FOM} = -178.60 dBc/Hz.

In this work the design has obtained the frequency of oscillation as 9.06GHz, Power consumption of 634.28µW with a supply of 1V, Phase noise as -97.48dBc/Hz @1MHz offset and the figure of merit of the LC-VCO is calculated as -178.60dBc/Hz for the un-buffered VCO. For buffered VCO the phase noise becomes -97.69dBc/Hz @1MHz offset and the FOM is -178.81dBc/Hz.

5. REFERENCES

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