Design and Simulation of Hybrid SET-CMOS based Hysteresis Circuits: Schmitt Trigger, with their Realization

A.Jana
Dept. of Electronics & Telecommunication Engineering
Jadavpur University, Kolkata

R. S. Halder
Dept. of Electronics & Telecommunication Engineering
Jadavpur University Kolkata

S.S.Singh
School of Electronics Engineering, KIIT University, Bhubaneswar

J.K.Sing
Dept. of Computer Science & Engineering
Jadavpur University kolkata

Subir Kumar Sarkar
Dept. of Electronics & Telecommunication Engineering
Jadavpur University,

ABSTRACT
Hybrid SET-CMOS circuits which combine the merits of both the SET [Single Electron Transistor] and CMOS promises to be a practical implementation for future low power ultra-dense VLSI/ULSI circuit design. In this work, an SET-CMOS hybrid hysteresis circuit is proposed. The MIB model for SET and BSIM4 model for CMOS are used. The operation of the proposed circuit is verified in Tanner environment.

Keywords
Single Electron Transistor, CMOS, Hybrid CMOS-SET Circuits, MIB, T-Spice..

1. INTRODUCTION
The term "hysteresis" is derived from ὑστέρησις, an ancient Greek word [1] meaning "deficiency" or "lagging behind". It was coined by Sir James Alfred Ewing. Hysteresis is desirable in a Schmitt trigger because it prevents noise form causing false triggering. The difference between the two threshold voltages is known as hysteresis.

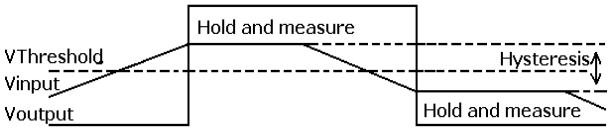

Fig 1: Hysteresis

Whenever the input voltage goes over the High Threshold Level, the output of the comparator is switched HIGH or LOW. The output will remain in this state, as long as the input voltage is above the second threshold level, the Low Threshold Level. When the input voltage goes below this level, the output of the Schmitt Trigger will switch. A Schmitt trigger is an electronic circuit that is used to detect whether a voltage has crossed over a given reference level.

However, there have been reports suggesting that the MOS transistor cannot shrink beyond certain limits said by its operating principle [2, 5]. Over recent years this realization has led to exploration of possible successor technologies with greater scaling potential such as single electron device technology. Single Electron Device (SED) Technology is the most promising future technology to meet the demand for increase in density, performance and decrease in power dissipation in future VLSI circuits. The Single Electron devices have potential to manipulate electrons on the level of elementary charge, are thus considered to be the devices that will allow such a charge. In addition to their low- power nature [4], the operation of SED is more guaranteed even when device size is reduced to the molecular level. It is also mentionable that the performance of the SED improves as its size reduces more.These properties are quite beneficial for large scale devices. The most important three-terminal SED is single-electron transistor. The schematic structure of SET is shown in Fig. 2.

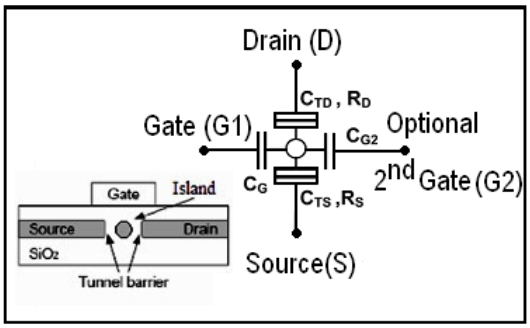

Fig. 2: Schematic structure of SET and its equivalent circuit

2. NEED OF HYBRIDIZATION
SET has attracted attention as a candidate for future VLSI mainly due to its three virtues: nanoscale feature size, ultralow power dissipation, and unique Coulomb blockade oscillation characteristics. In spite of such interesting properties, the practical implementation of the SET is questionable because of its low current drive and lack of mature room temperature operable technology. SET advocates low power consumption and new functionality (related to the Coulomb blockade oscillations), while CMOS has advantages such as high-speed driving and voltage gain that can compensate for the intrinsic drawbacks of SET. Though a complete replacement of CMOS by SET is not easy, but simultaneously it is also true that the combination of SET and CMOS can bring a new era in VLSI technology [2,3].

3. HYBRID SET-CMOS INVERTING & NON INVERTING SCHMITT TRIGGER
The circuit for Hybrid SET-CMOS Inverting & Non Inverting Schmitt Trigger is shown in Fig. 3.

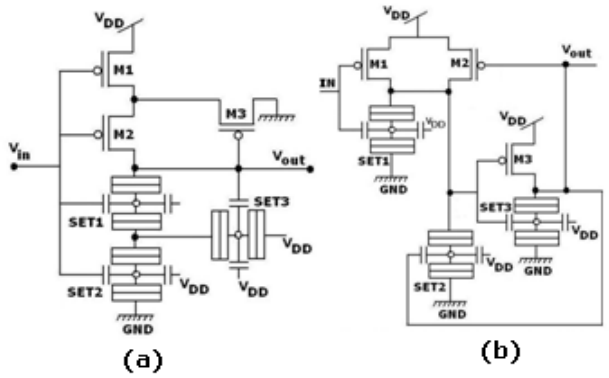

Fig.3: (a) Inverting Schmitt Trigger & (b) Non-Inverting Schimitt trigger

For Inverting Schmitt Trigger the circuit consists of three p-type MOSFETs M1, M2 & M3 and three SETs SET1, SET2 & SET3. At Vin = 0 V, M1 & M2 are turned on, then Vout = VM1 = VM2 = VDD. At the same time SET1 & SET2 are turned off. M3 is off; SET3 is on. So, VSET1 = VDD-VTSET. At Vin = VTSET, SET2 starts to turn on, SET1 is still off. Vout = VDD. At Vin = voltage increases from 0 to VDD, Assume SET1 will be off, while both SET2 & SET3 will operate in saturation region. If Vin increases, VSET1 decreases. At Vin = VDD, SET1 & SET2 are on, so that the output voltage is VM1= 0V. M1 & M2 are off and M3 is in saturation. At Vin = voltage decreases from VDD to 0, M1 will on, M2 will off and M3 will be in the saturation region.

In this way we can describe about the operation of non-inverting Schmitt trigger also. The SPICE simulation results are plotted in Fig.4 for a sinusoidal input voltage. The expected hysteresis behavior and the two switching thresholds are clearly seen in the simulation results.

From the simulation of inverting Schmitt trigger we get the following results: Vth (Upper) = 639.84mV, Vth (Lower) = 541.13mV

Hysteresis = 98.72mV.

And from simulation for non-inverting Schmitt trigger we get Vth (Upper) = 190.94mV,Vth (Lower) = 8.12mV,Hysteresis = 182.81mV.

Table 1.Values of Parameters used for the simulation

Device	Parameters	Voltage Level
SET	R_{TD} = R_{TS} = 1MΩ, C_{TD} = C_{TS} = 0.1aF, C_{G1} =0.27aF, C_{G2} = 0.125aF	Logic0=0V, Logic1= 0.8V V_{DD}=0.8V
PMOS	V_{TH} = -220mV, W/L = 100nm/65nm and default values of BSIM4.6.1 model for other parameters	Logic0=0V, Logic1= 0.8V V_{DD}=0.8V

The logic operations of the circuits were first examined by simulation using T-Spice simulation software. The simulated input-output waveform is depicted in Fig.4. The logic operation is found to be correct. Then we went for the power and delay calculations of our proposed circuit to find out whether our proposed model is better than MOSFET model or not. We performed our simulations taking the parameter values given in Table 1.First we are taking consideration of Hybrid SET-MOSFET based Non-inverting Schmitt trigger circuit. In this circuit 3 nos of MOSFET and 3 nos of SETs are used. Using the above table [Table 2] values we get that the total power consumption by an Inverting Schmitt trigger circuit, using hybrid model, is 3150nW and total delay is 123 pS because 3 MOSFETs are consuming 3000 nW power and delay of 3 MOSFETs are 120 pS. Parallely in that same circuit 3 SETs are consuming 150 nW power and their delay is 3 pS. In this circuit the total power consumption is 3150 nW due to 3 nos of SETs and 3 nos of MOSFETs [3000 nW+ 150 nW]. And the delay is 123 pS [For 3 nos of MOSFET 120 pS and 3 nos of SET 3 pS]. But if we implement the above circuit with MOSFETs only then we will find that the total power consumption would be 6000 nW and the total delay would be 240 pS. So hence we can get a conclusion that if we use hybrid SET-MOSFET based Non-inverting Schmitt trigger circuit than normal MOSFET based circuit then the whole circuit will consume less power and the delay will be lesser. Parallely we may take another conclusion that the same type of advantages we may get in case of hybrid non-inverting Schmitt trigger also. In Fig.5, we have shown a comparison graph of delay and power consumption using MOSFET based and SET-CMOS based circuit

4. CONCLUSION

The design and simulation of hybrid CMOS-SET Schmitt Trigger is described here. Since the SET and CMOS are placed in series, the hybridization is found to improve the gain of the circuit. The performances of the proposed circuits are verified by simulation using T-Spice. It is found that the power consumption of MOSFET circuit is two times more than the power consumption of hybrid circuit. It is also found that the delay is 2.5 times lesser in hybrid circuits. The simulation results show that the performances of the circuits presented in this paper are satisfactory thereby establishing the feasibility of using the proposed hybrid circuits in future low power ultra-dense VLSI/ULSI circuits.

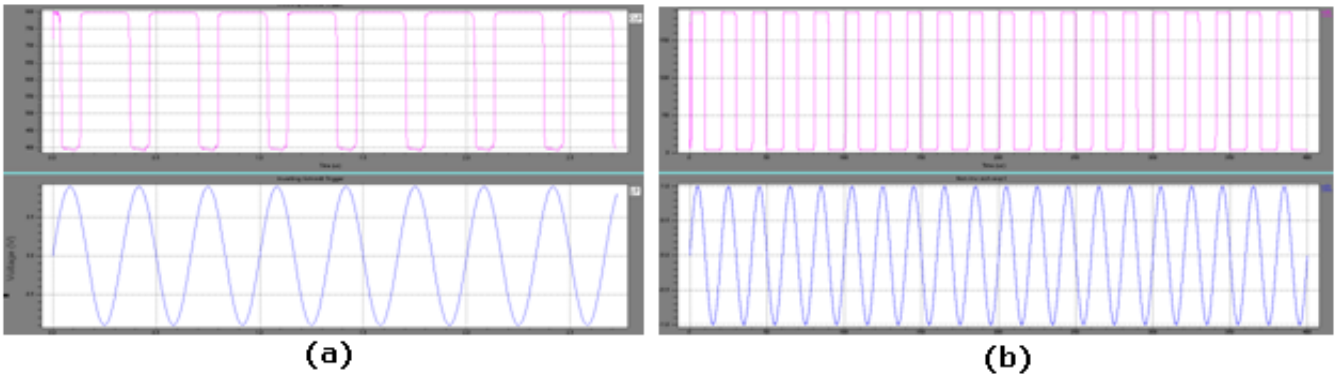

Fig.4 : Simulation results of (a)Inverting Schmitt Trigger (b) Non-inverting Schmitt Trigger using Hybrid SET-MOS.

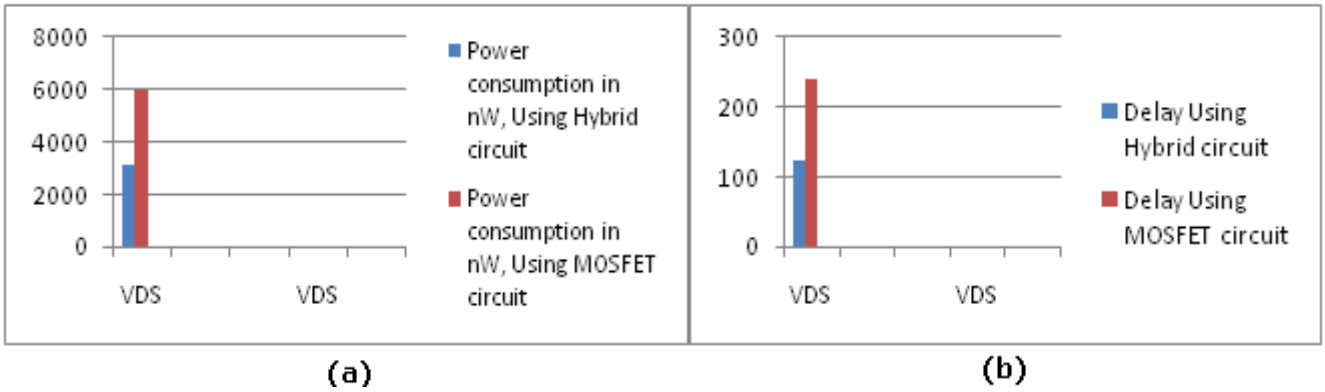

Fig.5: Comparison of (a) power consumption & (b) delay using Hybrid model and normal MOSFET model [Inverting circuit]

5. ACKNOWLEDGMENTS

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