# Dual Material Gate Nanoscale SON MOSFET: For Better Performance

Bibhas Manna
Dept. of E.T.C.E.
Jadavpur University
Kolkata, India

Saheli Sarkhel
Dept. of E.T.C.E.
Jadavpur University
Kolkata, India

Ankush Ghosh
Dept. of ECE,
Dream Institute of Technology,
Bishnupur
Kolkata, India

S. S. Singh
School of Electronics Engineering,
KIIT University
Bhubaneswar, India

Subir Kumar Sarkar
Dept. of E.T.C.E.
Jadavpur University
Kolkata, India

## ABSTRACT
A simple analytical model of a nanoscale fully depleted dual-material gate (DMG) SOI and SON MOSFETs has been developed and their performance comparison analysis is presented in this paper. An analytical model for the surface potential and threshold voltage has been developed both for these structures using a generalized 2D Poisson's equation solution. The DMG SON MOSFET technology is found to have more potential against various short channel effects (SCEs) thereby offering further device scalability with improved immunity.

## General Terms
Semiconductor Devices, ICs, VLSI & Embedded Systems.

## Keywords
SOI/SON MOSFET, Threshold Voltage, Short Channel Effect, DIBL.

## 1. INTRODUCTION
The main problem associated with this downscaling of MOS devices in the nanometer regime is the various short channel effects (SCEs). The predominant SCEs are Drain induced barrier lowering (DIBL), two dimensional charge sharing effect, channel length modulation, velocity saturation, impact ionization, gate tunneling or hot carrier effect etc. The conventional Bulk CMOS technology belonging to sub-micron regime could not overcome this fundamental physical limitation [1] which leads to a several non-conventional geometry MOS technology, among which fully depleted silicon-on-insulator (FDSOI) MOSFET has got more attention to the researchers. The reduced coupling effect of channel with source/drain and substrate in FD SOI structure initiates less SCEs thereby allowing the further device miniaturization [2]. Though FD SOI is better candidate for future MOSFET technology, there are some serious issues like growth technique of buried oxide, control of buried layer thickness etc. To overcome such drawbacks in FD SOI structure, an improved version of SOI called Silicon-on-nothing (SON) replacing BOX by air has been proposed recently [3-4]. SON has lower dielectric permittivity than oxide as a result the parasitic capacitances between source/drain and substrate are reduced and therefore higher circuit speed can be expected with SON devices [4].

Various SCEs can be reduced by introducing a new structure called a dual-material gate (DMG) MOSFET [5]. The DMG MOSFET structure has two metals M1 and M2 of different work functions $\Phi_{M1}$ and $\Phi_{M2}$ respectively. These two metals are placed together side by side forming a single gate electrode and provide a step in the surface potential profile, which thereby increases the drain current characteristics and suppresses various SCEs. The peak electric field in the drain end is also reduced for a DMG MOSFET compared to its single gate counterpart, indicating that the average electric field under the gate is also increased. The step function profile of the surface potential practically screens the region under M1 (the gate with higher work function) form the drain potential variation, thus providing an efficient protection against DIBL. In our present work, an analytical 2D Poisson's solution based surface potential and threshold voltage model has been proposed for DMG SOI and SON MOSFET. In our modeling approach, we first calculated the surface potential profile along the channel region of DMG structures and then the effective threshold voltage has been derived from that surface potential minimum.

## 2. ANALYTICAL MODELING
A schematic cross-sectional view of a generalized layered structure of fully depleted SOI/SON MOSFET is shown in Fig. 1 with gate metals M1 and M2 of lengths L1 and L2, respectively.

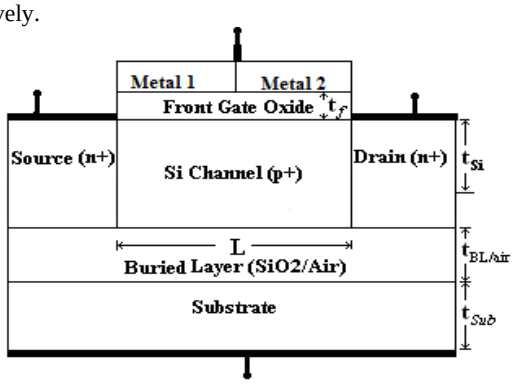


**Figure.1. A generalized Layered structure of DMG SOI/SON-MOSFET with metal 1 (with work function of 4.63 eV) and metal 2 (with work function of 4.17 eV).**

Under the assumptions that impurity density in the channel region and influence of charge carriers on the electrostatics of the channel are uniform, the potential distribution before the

onset of strong inversion in the silicon channel region can be given as:

$$\frac{d^2\psi(x,y)}{dx^2}+\frac{d^2\psi(x,y)}{dy^2}=\frac{qN_a}{\varepsilon_{si}} \quad \text{for } 0\le x\le L \text{ (L1+L2)}$$

$$\text{and } 0\le y\le t_{si} \quad (1)$$

Where, $\psi(x, y)$ is the 2-D potential profile in the silicon channel, $N_a$ is the doping concentration of the p-type channel and the substrate and $\varepsilon_{Si}$ is the permittivity of silicon. Considering a parabolic solution of the above equation (1), the 2D potential profile in the channel region under M1 and M2 can be written respectively as [5]

$$\psi_1(x,y)=\psi_{sf1}(x)+k_{11}(x)y+k_{12}(x)y^2 \quad \text{under M1}$$

$$\psi_2(x,y)=\psi_{sf2}(x)+k_{21}(x)y+k_{22}(x)y^2 \quad \text{under M2} \quad (2)$$

Where, $\psi_{sf1}$ and $\psi_{sf2}$ are the front interface potential under M1 and M2 respectively and $k_{11}(x)$, $k_{12}(x)$, $k_{21}(x)$ and $k_{22}(x)$ are x dependent coefficients. As the same calculations have carried out under metal1 and metal2, we can show a generalized calculation valid under both metals for brevity of our model. The eq.(1) can be solved with the four boundary conditions as follows:

At the front interface of the channel;

$$\psi(x,y)=\psi_{sf}(x)|_{y=0} \quad (3)$$

At the back interface of the channel;

$$\psi(x,y)=\psi_{sb}(x)|_{y=t_{Si}} \quad (4)$$

At the source-channel junction;

$$\psi(x,y)=\psi(y)|_{x=0}=V_{bi} \quad (5)$$

At the drain-channel junction;

$$\psi(x,y)=\psi(y)|_{x=L}=V_{bi}+V_{ds} \quad (6)$$

where, $V_{bi}$ is the built in potential, $\Psi_{sb}$ is back interface potential and $V_{ds}$ is the applied drain bias. Solving eq.(1) using eqs.(2),(3), (4), (5) and (6), we get the surface potentials under M1 and M2 respectively as[5]:

$$\psi_{sf1}=C_1\exp(r_1x)+C_2\exp(r_2x)-(n_1/m) \quad (7)$$

$$\psi_{sf2}=C_3\exp\left(r_1(x-L_1)\right)+C_4\exp\left(r_2(x-L_1)\right)-(n_2/m) \quad (8)$$

where, $m_1=m_2=m$, $r_1=\sqrt{m}$ and $r_2=-\sqrt{m}$ are the roots of the eqs. (7) and (8) respectively and the constant coefficients are given as:

$$m_1=m_2=\left[\frac{2\left(1+\frac{C_f}{C_b}+\frac{C_f}{C_{si}}\right)}{t_{si}^2(1+2\frac{C_{si}}{C_b})}\right]$$

$$n_1=\frac{qN_a}{\varepsilon_{si}}-\frac{2}{t_{si}^2\left(1+2\frac{C_{si}}{C_b}\right)}\left[V_{gs1}^{'}\left(\frac{C_f}{C_b}+\frac{C_f}{C_{si}}\right)-V_{ss}^{'}\right]$$

$$n_2=\frac{qN_a}{\varepsilon_{si}}-\frac{2}{t_{si}^2\left(1+2\frac{C_{si}}{C_b}\right)}\left[V_{gs2}^{'}\left(\frac{C_f}{C_b}+\frac{C_f}{C_{si}}\right)-V_{ss}^{'}\right]$$

$$C_1=\left[\frac{\left(V_{bi}+\left(\frac{n_2}{m}\right)+V_{ds}\right)-\exp(-r_1L)\left(V_{bi}+\frac{n_1}{m}\right)-\frac{(n_2-n_1)}{m}\cosh(r_1L_2)}{1-\exp(-2r_1L)}\right]\exp(-r_1L)$$

$$C_2=\left[\frac{\left(V_{bi}+\frac{n_1}{m}\right)-\left(V_{bi}+\left(\frac{n_2}{m}\right)+V_{ds}\right)\exp(-r_1L)+\frac{(n_2-n_1)}{m}\cosh(r_1L_2)\exp(-r_1L)}{1-\exp(-2r_1L)}\right]$$

$$C_3=C_1\exp(r_1L_1)+\frac{(n_2-n_1)}{2m} \quad \text{and} \quad C_4=C_2\exp(r_2L_1)+\frac{(n_2-n_1)}{2m}$$

After long mathematical calculation the short channel threshold voltage is obtained as:

$$V_{th}=V_{th}^{eff}+\frac{1}{C_{Si}}\left[\frac{2\phi_F}{C_3}-\frac{C_1}{C_2}-2\phi_F\right] \quad (9)$$

Here, $V_{th}^{eff}$ is the effective threshold voltage considering fringing field and substrate field [7] and $D_1$, $D_2$, $D_3$ are given as;

$$D_1=\{V_{bi}[\sinh(\frac{(L_1+L_2)-x_{\min}}{\lambda})+\sinh(\frac{x_{\min}}{\lambda})]+V_{ds}\sinh(\frac{x_{\min}}{\lambda})\}\{\sinh(\frac{(L_1+L_2)}{\lambda})\}^{-1},$$

$$D_2=1-\frac{[\sinh(\frac{(L_1+L_2)-x_{\min}}{\lambda})+\sinh(\frac{x_{\min}}{\lambda})]}{\sinh(\frac{(L_1+L_2)}{\lambda})},$$

$$D_3=\frac{[\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}]}{[1+\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}]},$$

$$\lambda=\sqrt{\frac{t_{Si}^2[1+2\frac{C_{Si}}{C_{BL/air}}]}{[1+\frac{C_f}{C_{BL/air}}+\frac{C_f}{C_{Si}}]}}.$$

Where, $C_f$: Front interface capacitance, $C_{BL/air}$: Buried Layer capacitance oxide/air, $C_{Si}$: Channel depletion layer capacitance, $X_{min}$: Minimum surface potential of the channel [7].

## 3. RESULTS AND DISCUSSIONS

We have considered a dual material gate SON structure having channel length of 100nm for analytical calculations and subsequent simulation. Two metals with different work functions have been taken as the gate.

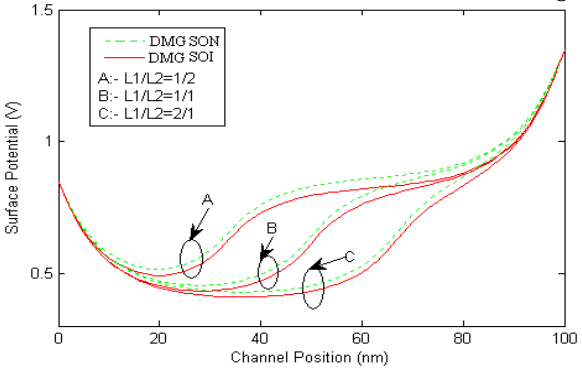


**Figure.2 Surface Potential Distribution along channel position of DMG SOI &SON MOSFET with L=100nm.**

Fig 2 shows the variation of surface potential with channel position for different combinations of gate lengths $L_1$ and $L_2$. It is seen from the figure that the position of minimum surface potential, lying under $M_1$ is shifting toward the source as the length of gate $M_1$ having higher work function is reduced. This causes the peak electric field in the channel to shift more toward the source end and thus there is a more uniform electric field profile in the channel. This happens because as $L_1$ increases, a portion of the channel controlled by the gate metal with larger work-function is increased. This uniformity is more for SON in nano regime, indicating higher immunity to DIBL.

Threshold voltage variation with channel length is shown in Figure.3 for each pair of gate length ratio (viz. L1/L2= 2/1, 1/1, ½ respectively). It is quite evident from the figure that threshold voltage is less in the SON than SOI due to a reduced potential coupling ratio ($P_{CR}= \phi_f / \phi_b$ ) in SON making SON immune to various SCEs.

Figure.4 shows the variation of the drain current with the drain to source voltage incorporating the channel length modulation (CLM), DIBL and other SCEs for two different gate to source voltages. It is clear from the figure that the drain current shows a finite slope in the saturation region if we consider CLM and other effects in our model [5-6].

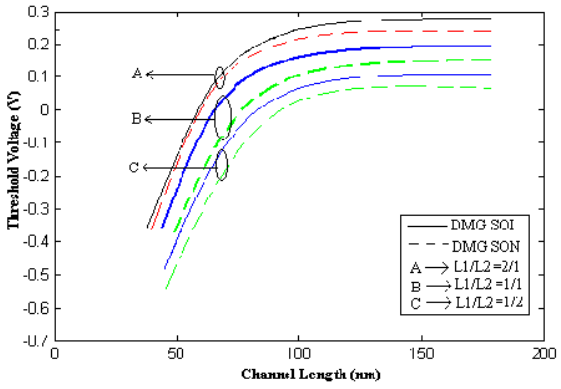


**Figure.3 Variation of threshold voltage with channel length for different values of ( $L_1/L_2$ )of DMG SOI &SON MOSFET.**

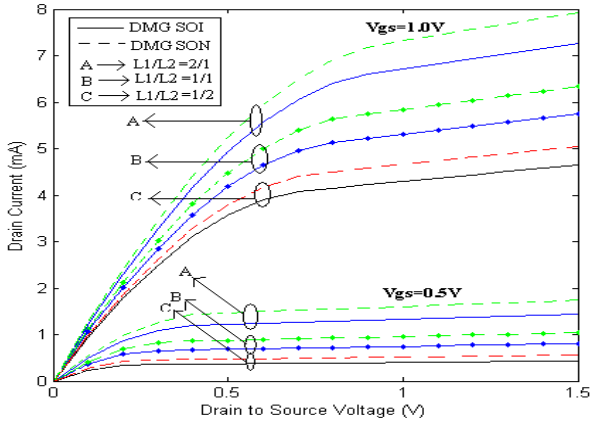


**Figure.4 Variation of drain current with Drain to Source Voltage for different values of gate to source voltages and (L1/L2) ratio.**

## 4. CONCLUSION

Different characteristics of a DMG SON structure are simulated and performance comparison is made with DMG SOI to examine the effectiveness of the DMG structure in fully depleted SON MOSFET by developing a 2-D analytical model for surface potential and threshold voltage. Analytical model based simulation verified that SON is superior over SOI MOSFET due to its more immunity to different Short channel effects (SCEs) and increased current driving capability, thereby having reduced DIBL effect.

## 4. ACKNOWLEDGEMENT

The work is supported by DRDO vide order no. EIRP/ER/1103935M/01/1344 dated 28/06/2011.

## 5. REFERENCES

[1] The International Technology Roadmap for Semiconductor, Emerging Research Devices, 2009.

[2] COLINGE J P. Silicon on insulator technology: materials to VLSI. 2nd ed. Norwell, MA: Kluwer: Kluwer Academic Publishers; 1997.

[3] JURCZAK. M., et al, Silicon-on-Nothing (SON)-an Innovative Process for Advanced CMOS, IEEE Transactions on Electron Devices, 2000; 47(11), 2179-2187.

[4] PRETET. J. et al., Silicon-on-Nothing MOSFETs: Performance, Short-Channel Effects, and Backgate Coupling, IEEE Transactions on Electron Devices, 2004; 51(2), 240-246.

[5] G. Venkateshwar Reddy and M. Jagadesh Kumar, "A New Dual-Material Double-Gate (DMDG) Nanoscale SOI MOSFET-Two-Dimensional Analytical Modeling and Simulation", IEEE Transactions on Electron Devices,vol..4, no.2, pp.260-268, 2005.

[6] K. Suzuki and T. Sugii, "Analytical models for n+-p+ double gate SOI MOSFET's", IEEE Transaction on .Electron Devices, vol. 42, pp. 1940-1948, 1995.

[7] Saptarsi Ghosh, Khomdram Jolson Singh, Sanjoy Deb and Subir Kumar Sarkar, "Two dimensional analytical modeling for SOI and SON MOSFET and their performance comparison", JNEP.3(2011), No.1, P.569-57.