Improvising Low Power SRAM Cell in 32 nm Technology with the use of an Extra nMOST

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ABSTRACT
This paper focuses on reducing the Write Power consumption and delay of a SRAM cell in 32 nm technology. Static Random Access Memory (SRAM) is an important memory device for storing data on a chip. In CMOS, whatever chips and memory devices we see today, are actually made up of the layouts of metals and poly-Si on a highly pure silicon wafer. As the need for fast circuits has grown so, has the power consumption. In SRAM cells write operation is the most power consuming one. With the help of the new proposed design of 7-T SRAM write power can be reduced by about 7.7%, and write delay by 5%; apart from reducing the area of the chip being used by a single SRAM cell by 20.5%. The design has been implemented and simulated using Microwind 3.1 and Dsch 3.5 software.

Keywords
CMOS, low power, delay, SRAM.

1. INTRODUCTION
Static random access memory is very important in modern devices as the device size is shrinking and high speed and low power consumption devices are needed. Efficient utilization of on-chip memory is extremely important in modern ultra-nanoscale CMOS technology. Considerable attention has been paid to the design of low-power, high-performance SRAMs since they are a critical component in both hand held devices and high-performance processors [1]. Lowering supply voltage is one of the first choices of the designers for ultra-low-power design of high-density SRAMs in which the operating voltage below the transistor threshold voltage is extremely challenging [2]. The SRAM cell becomes less stable at low V_{dd}, increasing leakage current and increasing variability [3].

The 6T-SRAM cell (Fig.1) consists of a flip-flop circuit, constructed between a power supply voltage (V_{dd}) and ground (V_{ss}) and two excess nMOS transistors. SRAM is fast because the six-transistor configuration (shown in Fig.1) of its flip-flop circuits keeps current flowing in one direction or the other (0 or 1). The excess nMOS transistors are designed to be larger than the pMOS transistors of the cross coupled circuit of the flip-flop. Each bit in SRAM is stored on four transistors which forms two cross-coupled Inverters. It has two stable state **0** and **1**. T-5 and T-6 are transfer MOSTs, T-2 and T-4 are driver MOSTs and T-1 and T-3 are load MOSTs. MOST T-5 and T-6 are sometimes also referred as access transistors since they control the access to the storage cell during write and read operations from the bit-line pair's performance.

The memory of a SRAM cell, a CMOS Inverter shown in Fig.2, consists of one nMOST and one pMOST. The nMOST discharges the load capacitance quickly and completely but charges up slowly (resulting in reduction of V_t - threshold voltage). The latter of the two charges up quickly without any reduction in V_t.

Thus a COMS circuits enjoys the advantages of both the kind of MOST, fast charging by a pMOST and fast discharging by an nMOST, giving a full swing of V_{dd}. The threshold of a CMOS Inverter circuit V_{TC} is given as [4],

$$V_{TC} = \frac{V_{dd} - |V_{tp}| + V_{tn}\sqrt{\beta_R}}{(1+\sqrt{\beta_R})}, \text{ where}$$

$$\beta_R = \beta_n / \beta_p, \ \beta_n = (W_n / L_n)\,\mu_n C_{OX}$$

$$\beta_p = (W_p / L_p)\,\mu_p C_{OX};$$

Here, β_n and β_p are the conductance of nMOST and pMOST respectively.

$$V_{TC} = V_{dd}/2 \text{ ; for } \beta_n = \beta_p \text{ and}$$

$$|V_{TC}| = V_{tn}$$

V_{TC} increases with increase in V_{tn} while decreases with increase in V_{tp}.

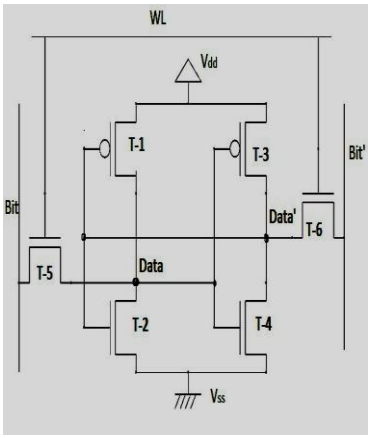

Figure.1 (6-T SRAM)

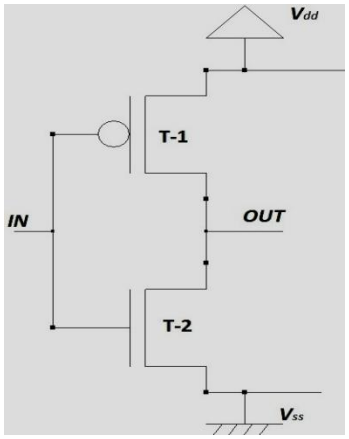

Figure.2 (INV 1)

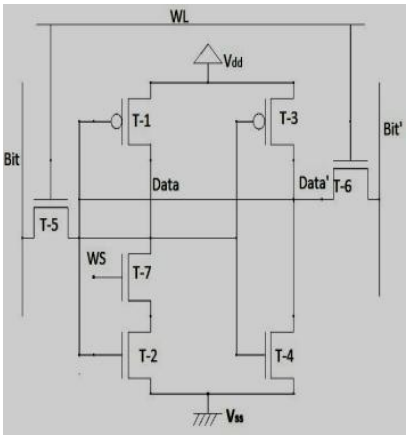

Figure.3 (proposed 7-T SRAM)

2. CONVENTIONAL 6-T SRAM

Fig.1 shows a convention 6-T SRAM cell and Fig.4 is the layout design [5] of it in 32 nm technology made in Microwind 3.1 software. In this 6-T SRAM design $W_5/W_1 = W_6/W_3$=1.25, $W_2/W_5 = W_6/W_4$ =1.40 and $W_2/W_1 = W_4/W_3$ =1.75. T-2 and T-4 are made larger than access transistors T-5 and T-6 so that intermediate voltages don't flip the content of the other storage node. Write operation [6] starts with assigning the values to be written at the Bit and its complimentary value at Bit'. In order to write 1 Bit is pre-charged with high voltage and the complimentary value **0** is assigned to Bit' then WL is set high, which allow value at Bit and Bit' to inter the internal latch circuit and **1** is stored at Data and its complimentary **0** at Data'.

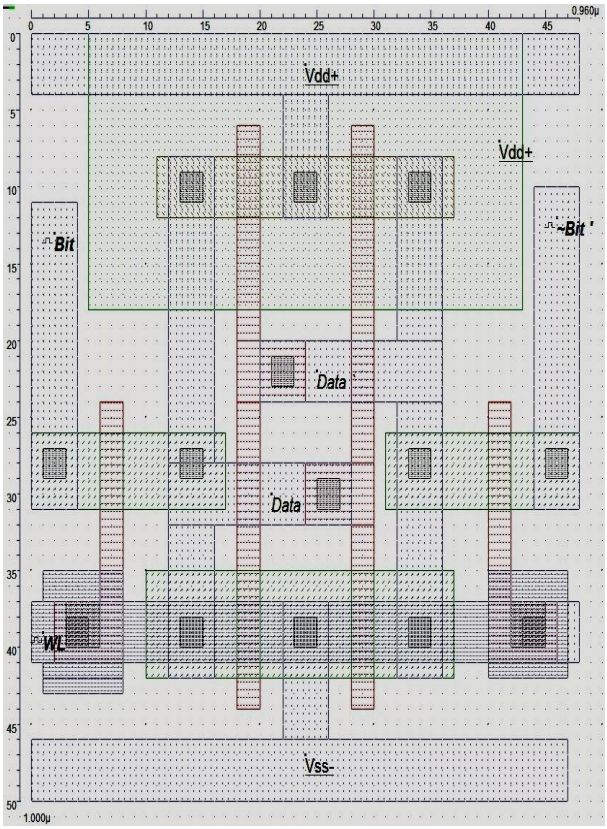

Figure.4 (layout of 6-T SRAM)

3. PROPOSED 7-T SRAM DESIGN

In the new proposed design Fig.3 a new MOST is added in the internal latch circuit. This introduction of a new nMOST in one of the cross-coupled inverter checks the flow of leakage current during flipping of the cross-coupled inverter pair. The **WS** must be at **0** till **0.5 ns** after that, changes in its state don't affect the power consumption of the proposed SRAM cell. In this design also:

$$W_5/W_1 = W_6/W_3 = 1.25,$$

$$W_2/W_5 = W_6/W_4 = 1.40$$

$$W_2/W_1 = W_4/W_3 = 1.75 \text{ and}$$

$$W_7 = W_2 = W_4.$$

The possible layout is shown in Fig.5.

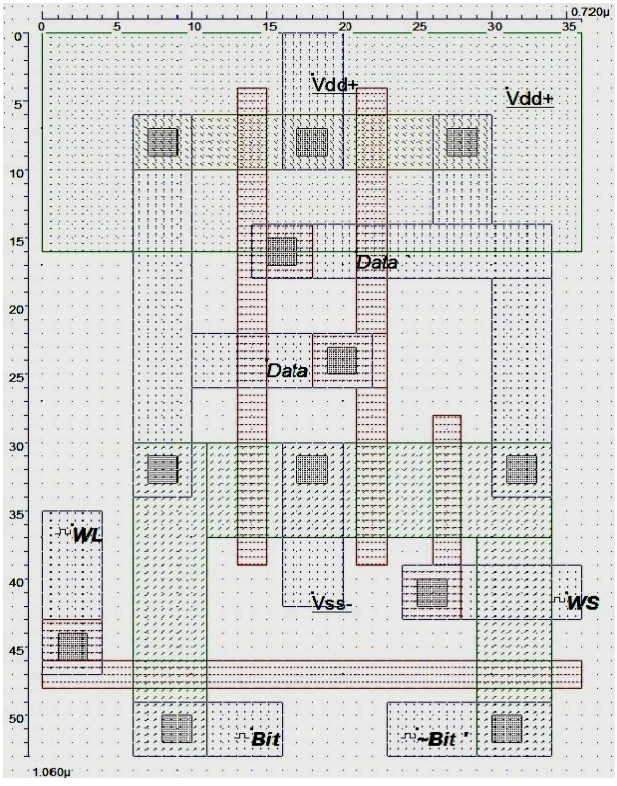

Figure.5 (layout of 7-SRAM)

4. RESULTS AND DISCUSSIONS

The new proposed 7-T SRAM cell shows significant improvement, **20.5**% in Area of the chip used and **7.7**% in power consumption during write operation, apart from **1** ps decrease in write delay. The results have been obtained keeping all the input conditions same. Table-1 compares the result between both the SRAMs. Fig.7 shows the complete working of the proposed 7-T SRAM while Fig.7 compares the Write operation in both SRAMs. WS is there only in 7-T SRAM and the delay in write operation has been shown in-circle in Fig.7.

Table 1: 6-T and 7-T SRAMs output comparison

	6-T SRAM	**7-T SRAM**	**Percentage Improvement**
Area (μm^2)	0.9600	0.7632	20.5
Metal layers	2	1	50
Write delay (ps)	20	19	5
Write Power (µW)	0.026	0.024	7.69

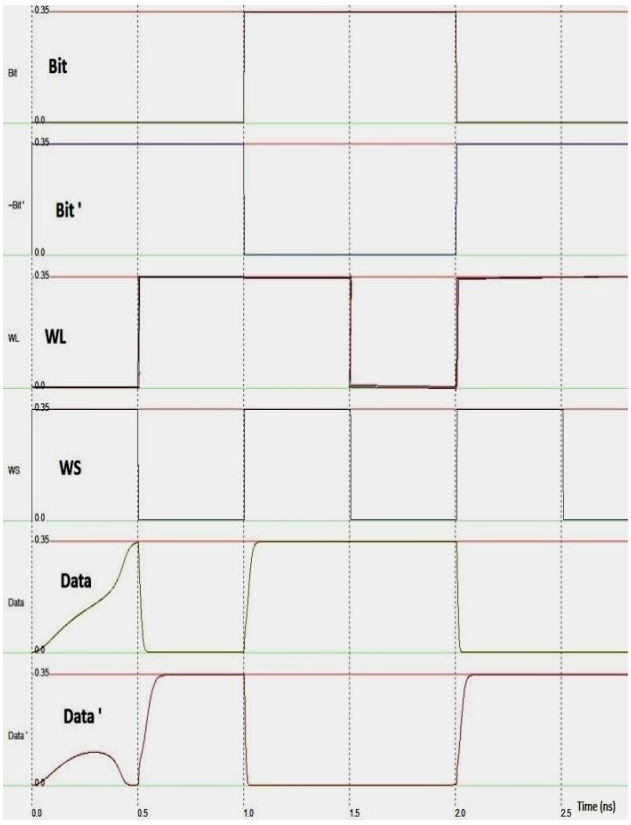

Figure.6 (Output 7-T SRAM)

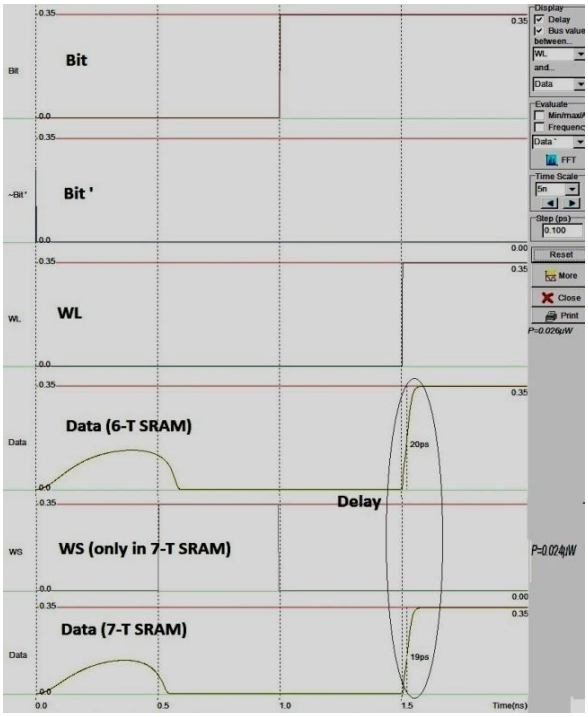

Figure.7 (Write operation of both SRAM)

5. CONCLUSION

The new proposed layout design of 7-T SRAM consumes much less area than the previous 6-T design as well as shows significant improvement in the power consumption during Write operation. The proposed 7-T SRAM is even faster than 6-T SRAM as the delay during write operation is less. So, the proposed 7-T SRAM layout design can be a better replacement of the 6-T SRAM in 32 nm technology.

6. REFERENCES

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