Performance Analysis of AlInN/GaN Underlap DG MOSFET for varying Underlap and Gate length

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ABSTRACT

In this work, we investigate the performance of 18nm gate length AlInN/GaN Heterostructure Underlap Double Gate MOSFETs, using 2D Sentaurus TCAD simulation. The simulation is done using the hydrodynamic model and interface traps are also considered. Due to large two-dimensional electron gas (2DEG) density and high velocity, the maximal drain current density achieved is very high. Extensive device simulation of major device performance metrics such as DIBL, SS, delay, and I_{on}/I_{off} ratio have been done for varying gate length (L_g) and underlap length (L_{un}). Impressive results for Delay, I_{on}, and DIBL are obtained. The results indicate that there is a need to optimize the I_{off} and SS values for specific logic design.

Keywords

Underlap, Heterostructure, 2DEG, HEMT, Ultra thin body (UTB), DIBL, SS, Interface Traps.

1. INTRODUCTION

Lattice matched $Al_{0.83}In_{0.17}N$ /GaN heterostructure devices have shown superior performance in comparison to conventional AlGaN/GaN heterostructure devices because of the substantially higher spontaneous polarization induced 2DEG density [1] and higher electron mobility in the range 1200 to 2000 cm^2/Vs [2]. In High Electron Mobility Transistors (HEMT) gate leakage current is an important factor limiting its performance and reliability [1]. Thus a thin gate dielectric oxide layer is often inserted between the gate metal and the InAlN wideband gap barrier layer [3–5] forming a metal oxide semiconductor-HEMT (MOS-HEMT). Though several single gate InP/InGaAs, AlGaN/GaN and AlInN/GaN MOS-HEMT devices have been reported [6-7], none have reported double gate and underlap double gate MOS-HEMT structure till date to the best of our knowledge. In this paper for the first time, we report 18nm gate length InAlN/GaN Underlap DG MOSFET. Extensive device simulation of major device metrics such as DIBL, SS, Delay, and I_{on}/I_{off} ratio have been done for wide range of gate and underlap lengths

2. Device Description

We simulated $Al_{0.83}In_{0.17}N$/GaN underlap DG MOSFET device (Fig 1) having gate length 18nm, symmetrical underlap lengths of 5nm on both source and drain side, with an undoped Ultra Thin Body (UTB). The source/drain region lengths are 5nm, the front and back gate has high-k Hafniun dioxide (HfO_2) with EOT of 1.2nm. The device source/drain regions doped at 10^{20} cm^3 and uses abrupt doping profile at source and drain ends. Narrow bandgap GaN layer (t_2=4nm) is sandwiched between the two wide bandgap AlInN barrier layers (t_1=1nm) and the channel is confined at the heterostructure interfaces. The barrier layers provides i) strong carrier confinement and (ii) minimizes leakage current I_{off}. Physical properties of GaN and $Al_{0.83}In_{0.17}N$ are listed in table 1.

Table 1 Physical properties of $Al_{0.83}In_{0.17}N$ and GaN

Material	GaN	$Al_{0.83}In_{0.17}N$
E_g (eV)	3.4	4.7
CBO (eV)	0.57	-
VBO (eV)	0.73	-
ε_o	9.5	11.7
Lattice Constant (A)	3.186	3.190
μ_e (cm^2/Vs)	940	1540
μ_h (cm^2/Vs)	22	82

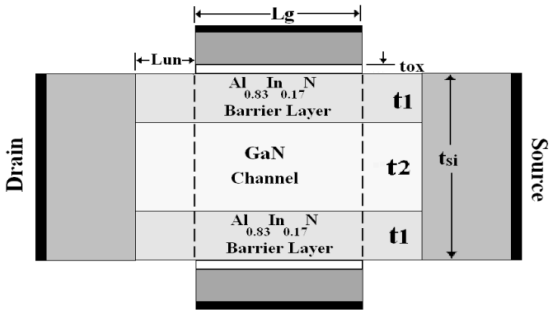


Fig. 1 Heterostructure Underlap DG MOSFET showing underlap near source and drain sides. The channel consists of GaN (t_2=4nm) region and two barrier $Al_{0.83}In_{0.17}N$ (t_1=1nm) regions.

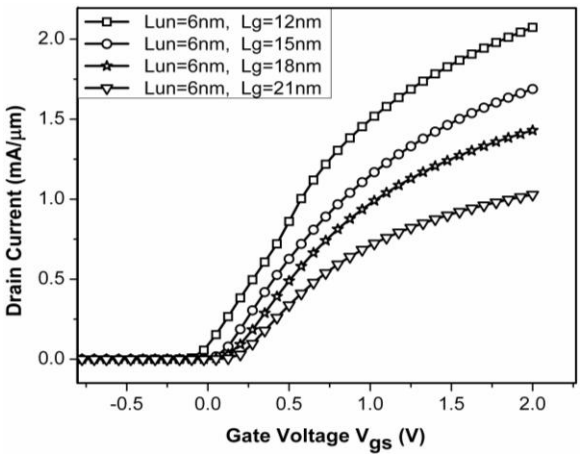
3. Device Simulation Framework

Two dimensional hydrodynamic simulations have been carried out using Sentuarus TCAD. The hydrodynamic model (HD) accurately explains non-equilibrium conditions such as quasi-ballistic transport in the thin regions and the velocity overshoot effect in the depleted regions. Additionally, the model accounts for several physical effects such as bandgap narrowing, variable effective mass, and doping dependent mobility at high electric fields. The HD model solves the poisson equation and continuity equations as follows:

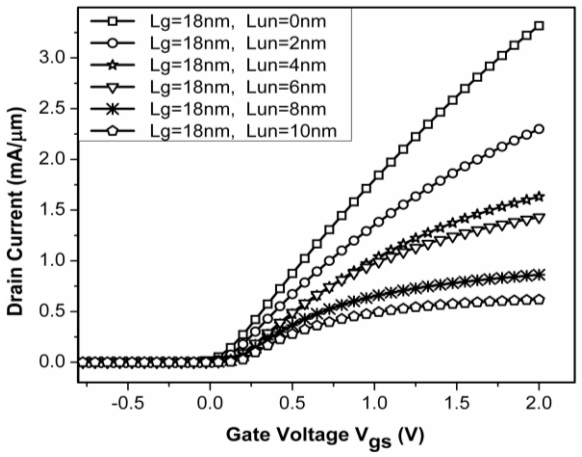
$$\nabla \cdot \varepsilon \nabla \phi = -q(p - n + N_D - N_A) - \rho_{trap.} \quad ...(1)$$

$$J_n = q\mu_n (n\nabla E_c + kT_n \nabla_n + kn\nabla T_n - 1.5nkT_n \nabla \ln m_n) \quad ...(2)$$

where ε is the electrical permittivity, ϕ is the electrostatic potential, q is the electronic charge, n and p are the electron and the hole densities, N_D is the ionized donors concentration, N_A is the ionized acceptors concentration, ρ_{trap} is the charge density contributed by traps and fixed charges, E_C is the conduction band edge energy, T_e is the electron temperature and m_e is the electron effective mass. Field and doping dependent mobility are included HD simulation. For recombination the Shockley–Read–Hall (SRH) model is used with SRH, radiative and Auger recombination values chosen are: τ_{SRH}= 60ns, C_{rad} = 1.4x10^{-9}cm^3/s, and C_{Auger} = 4x10^{-29} cm^6/s[8]. The van Overstraeten–de Man model is implemented for considering impact ionization.



(2a)

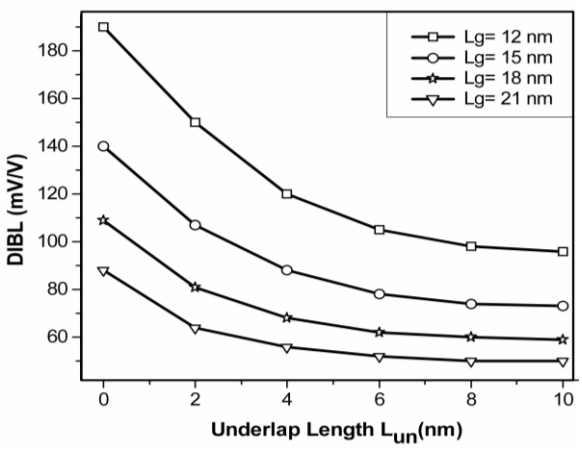


(2b)

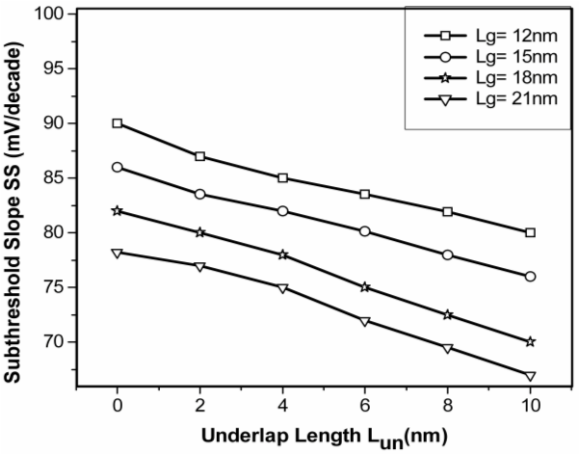
Fig 2: I_D versus V_g characteristics for applied drain voltage is V_d=1V for both devices (a) L_g varied from 12nm to 21nm with L_{un}=6nm. (b) L_{un} varied from 0 to 10nm with constant L_g=18nm.

4. Results and Discussion

The transfer characteristics of the AlInN/GaN MOS-HEMT device for variable gate length (fig 2a) and variable underlap length (fig 2b) depicts very high drain current density (~3.6 mA/μm for L_g=18, L_{un}=0nm), arising from high mobility and velocity of 2DEG in the buried channel. Also there is high current density (2DEG) by virtue of high spontaneous polarization. We observe good drain current saturation arising from considerably lower EOT, with double gate providing much better channel control. We observe high drive current at both low drain and high drain bias, which has significance for high speed logic applications.



(3a)



(3b)

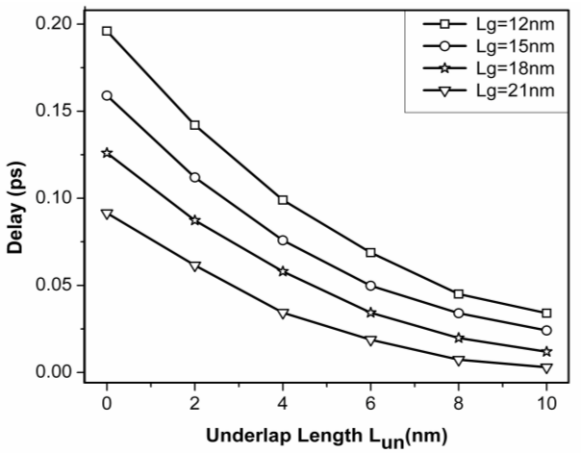
Fig. 3 (a) Variation of DIBL with underlap length L_{un}. (b) Dependence of Subthreshold Slope versus underlap length L_{un}.

DIBL for varying L_{un} and L_g is shown in fig (3a). As underlap length L_{un} increases the drain region moves away from channel and effect of drain potential on channel decreases. As drain region moves apart, barrier lowering insertion of barrier layer causes the channel to move away from the gate dielectric interface, reducing the electrostatic control and thus degrading SS. The observed vales of SS are higher than the ideal 60mV/decade value. SS is observed to decrease linearly with both underlap and gate length variation.

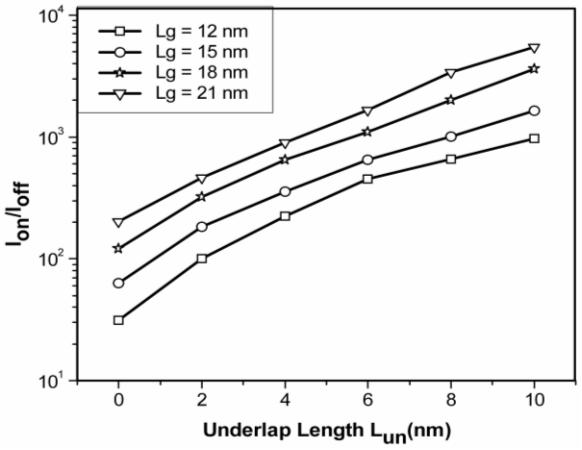
$$DIBL = \frac{\Delta V_{th}}{\Delta V_{ds}} = \left[\frac{(V_{th1} - V_{th2})}{(V_{ds1} - V_{ds2})} \right]$$

$$SS = \frac{\Delta V_g}{\Delta(\log I_d)} \quad ...(4)$$

where V_{th1} is threshold voltage extracted at V_{ds1}=50 mV and V_{th2} is threshold voltage extracted at V_{ds2}=1.0V



(4a)



(4b)

Fig 4: ((a) Variation of intrinsic device delay with underlap length L_{un}. (b) Dependence of I_{on}/I_{off} ratio on underlap length L_{un}.

Intrinsic device delay (τ) determines the device switching speed and is given by $\tau = CV/I$, where C is the total gate capacitance per micron transistor width, V is the power supply voltage (V_{dd}), and I is the saturation drive current per micron transistor width (I_{dsat}). Due to higher I_{dsat} and low C_{gg} the intrinsic delay will be very low and fast device switching can be achieved. Extremely low device delay (~0.003 ps) can be achieved with L_g=21nm device at L_{un}=10nm. Fig 4b shows I_{on}/I_{off} ratio variation with underlap length for multiple gate length devices. I_{on}/I_{off} ratio for this device is not very impressive due to higher I_{off} value, which in turn is attributed to higher leakage current. Maximum attainable I_{on}/I_{off} ratio value is $5.4x10^3$ for L_g=21nm and L_{un}=10nm.

5. Conclusions

Performance investigation of AlInN/GaN underlap DG MOSFETs is done for major device metrics like DIBL, SS, I_{on}/I_{off}, and delay for wide range of underlap and gate lengths. Impressive drain current density of ~3.6mA/μm is obtained for device with L_g=18nm and L_{un}=0nm. DIBL dependence on underlap length is more upto 5nm and becomes less for longer underlap. The SS performance is degraded because the buried channel is away from gate dielectric interface. Inspite of higher I_{on}, the I_{on}/I_{off} ratio is low due to higher I_{off} (due to high leakage). Extremely low intrinsic delay(~0.003ps) are achieved, due to higher mobility and velocity of carrier in the buried channel. The results show that there is a need to optimize the I_{off} and SS values for specific logic design. AlInN/GaN underlap DG MOSFET shows excellent promise to substitute present MOSFET for future high speed applications.

6. Acknowledgements

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7. References

[1] M. Alomari et al., "InAlN/GaN MOSHEMT With Self-Aligned Thermally Generated Oxide Recess," IEEE Electron Device Letters, vol. 30, no. 11, 2009, pp. 1131-1133.

[2] A. Dadgar, F. Schulze, and A. Diez, "High-sheet-charge – carrier-density AlInN ⁄ GaN field-effect transistors on Si (111)," Applied Physics Letters, vol. 85, no. 22, 2004, pp. 5400-5402.

[3] V. Adivarahan, J. Yang, A. Koudymov, G. Simin, and M. A. Khan, "Stable CW Operation of Field-Plated GaN-AlGaN MOSHFETs at 19 W/mm," IEEE Electron Device Letters, vol. 26, no. 8, 2005, pp. 535-537.

[4] C. Liu, et al., "Enhanced device performance of AlGaN/GaN HEMTs using HfO2 high-k dielectric for surface passivation and gate oxide," Semiconductor Science and Technology, vol. 22, 2007, pp. 522-527.

[5] M. Marso et al., "Origin of Improved RF Performance of AlGaN/GaN MOSHFETs Compared to HFETs," IEEE Transactions on Electron Devices, vol. 53, no. 7, 2006, pp. 1517-1523.

[6] M. A. Khan, X. Hu, et al., "AlGaN/GaN metal – oxide – semiconductor heterostructure field-effect transistors on SiC substrates," Applied Physics Letters, vol. 77, 2000, pp. 1339-1341.

[7] V. Adivarahan et al., "Submicron Gate SiN3/AlGaN /GaN - Metal-Insulator-Semiconductor Heterostructure Field Effect Transistor," IEEE Electron Device Letters, vol. 24, no. 9, 2003, pp. 541-543.

[8] G. Ji, H.-G. Liu, et al., "Physical modeling based on hydrodynamic simulation for the design of InGaAs/InP double heterojunction bipolar transistors ," Chinese Physics B, vol. 21, no. 5, 2012, pp. 058501-1 - 058501-1.