Analytical Drain Current Model for Symmetrical Gate Underlap DGMOSFET

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ABSTRACT
The drain current model of symmetrical Underlap DGMOSFET is evaluated for subthreshold region. Model data is verified with simulation data for validation of the proposed model. For validation the drain current is evaluated with respect to gate to source potential. The drain current is calculated with variation of gate length, underlap length and silicon body thickness. As the gate length and underlap length increases, the drain current decreases and as silicon body thickness increases, increase of drain current is observed.

General Terms
Semiconductor Devices, MOSFET Modelling.

Keywords
Drain current, Ultrathin body, Virtual source, Underlap DGMOSFET

1. INTRODUCTION
DOUBLE GATE (DG) MOSFET is a candidate which reduces short channel effects (SCEs) and gives better scalability and performances [1].The DG MOSFET has been made known very good electrostatic gate control over the channel, permitting gate length scaling down to 10 nm [2].Gate underlap of source/drain has a vital importance over lightly or undoped channel double-gate MOSFETs [3,4]. Gate underlap or non-overlap has more advantages over double-gate MOSFETs in subthreshold region such as it reduces gate edge direct tunneling leakage, gate sidewall fringe capacitance and also reduces SCE due to increase in effective channel length, ensuring improved circuit performance. Gate underlap DGMOSFET can be used in subthreshold circuit for ultra-low power consumption with low to medium frequency [5].

The current modeling of gate underlap DGMOSFET is necessary to know the drive capability of the transistor. Asymmetrical gate underlap modeling was given by[6], still symmetrical current modeling is to be investigated for subthreshold regime. Underlap DG devices functioned at small current intensities are predominantly suitable for ULV analog/RF applications as gain and speed of devices can be considerably enriched [7].

2. THE SUBTHRESHOLD CURRENT MODEL
For weak inversion region, the 2D Poisson's equation of gate underlap DGMOSFET (as shown in Fig.1) for three regions (I, II and III) are given by

$$\frac{\partial^2 \psi_i(x,y)}{\partial x^2} + \frac{\partial^2 \psi_i(x,y)}{\partial y^2} = \frac{qN_a}{\varepsilon_{Si}} \quad (1)$$

Where $\Psi_i(x, y)$ is the potential variation in three regions (for i=I, II and III) along x and y direction, q is the electronic charge, N_a is doping concentration along the channel and ε_{Si} is permittivity of silicon. Fig.1 interprets the separation of the three regions. The potentials of three regions are considered as parabolic is given by [6, 8]

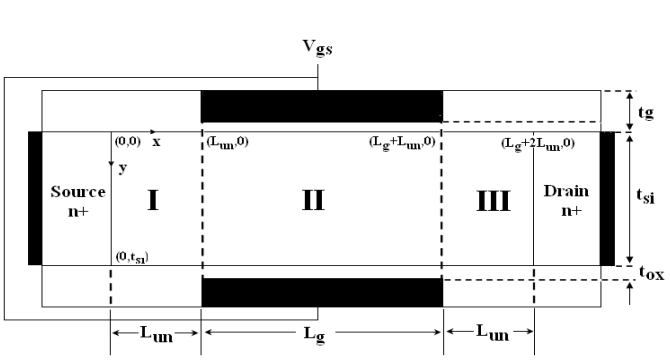
$$\psi_i(x,y) = \alpha_{i1}(x) + \alpha_{i2}(x)y + \alpha_{i3}(x)y^2 \quad (2)$$

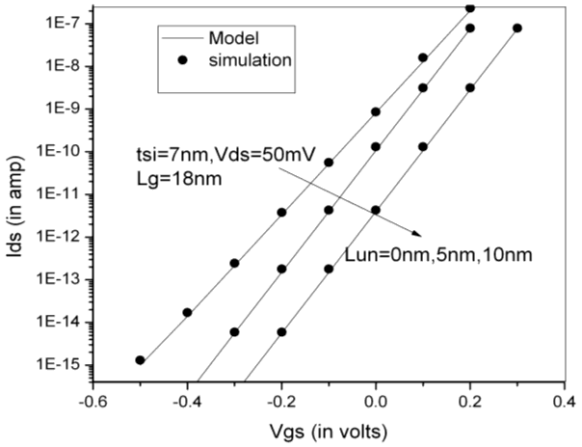
$\alpha_{i1}(x)$, $\alpha_{i2}(x)$ and $\alpha_{i3}(x)$ are the coefficients to be evaluated by proper boundary conditions. Since inner fringing field from the gate side wall affect the current conduction, to avoid tough mathematical burden we considered a minimum surface potential model i.e. virtual source. The surface potential model was derived [8] for three regions. We investigated the minimum surface potential occur at region-II (Gate overlap region).The surface potential of region –II is given by [8]

$$\psi_{s2}(x,y) = Ce^{(x-L_{un})/\lambda} + De^{-(x-L_{un})/\lambda} - \frac{qN_a\lambda^2}{\varepsilon_{si}} + V_{gs} - \phi_{ms} \quad (3)$$

where L_{un} is underlap length, V_{gs} is gate to source potential ,ϕ_{ms} is difference of work function between metal and semiconductor, the coefficient C and D can be calculated from[8] and natural length λ is given by $\lambda = \sqrt{\frac{\varepsilon_{si}t_{ox}t_{si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}t_{si}}{4\varepsilon_{si}t_{ox}}\right)}$, Where t_{si} and t_{ox} is thickness of body and oxide and ϵ_{ox} is oxide permittivity. The minimum surface potential point x can be calculated from $\frac{\partial \psi_{s2}(x,y)}{\partial x} = 0$, Substituting the value of x in (3) we have minimum surface potential

$$\psi_{s2_{\min}}(x) = 2\sqrt{CD} - \frac{qN_a\lambda^2}{\varepsilon_{si}} + V_{gs} - \phi_{ms} \qquad (4)$$

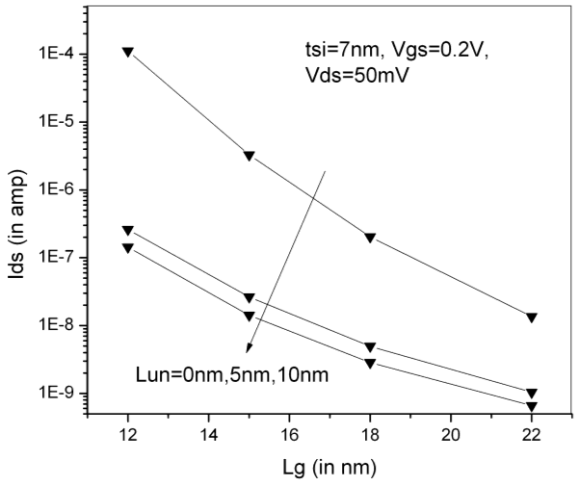


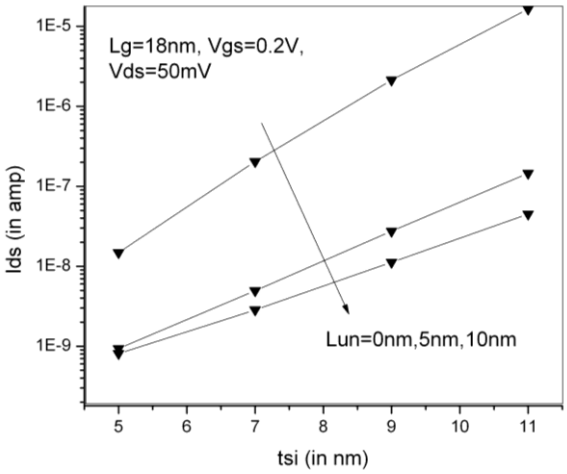


(a) **(b)**

Fig1 (a): Schematic of an underlap DG MOSFET considered for model development. Regions I and III are underlap regions. Device body (regions I, II, and III) is undoped. (L_g= gate length, L_{un}= gate underlap, t_{ox}=gate-oxide thickness, t_{si}= silicon thickness, t_g= gate thickness).

Fig1 (b): Drain to source current versus Gate to source potential in subthreshold region for varying underlap length. The underlap length L_{un} is varied from 0 to 10nm in steps of 5nm. (L_g=18nm, t_{si}=7nm, t_{ox}=1.5nm, V_{ds}= 50 mV).





(a) **(b)**

Fig2 (a): Drain current versus Gate length in subthreshold region for varying underlap length. The underlap length L_{un} is varied from 0 to 10nm in steps of 5nm. (t_{si}=7nm, t_{ox}=1.5nm,V_{gs}=0.2V, V_{ds}= 50 mV).

Fig2 (b): Drain current versus silicon body thickness in subthreshold region for varying underlap length. The underlap length L_{un} is varied from 0 to 10nm in steps of 5nm. (L_g=18nm, t_{ox}=1.5nm,V_{gs}=0.2V, V_{ds}= 50 mV).

The minimum body potential in symmetric Gate underlap DGMOSFET [8] is given by

$$\psi_{2_{\min}}(x, \tfrac{t_{si}}{2}) = \psi_{s2_{\min}}(x)\left(1 + \frac{\varepsilon_{ox}t_{si}}{4\varepsilon_{si}t_{ox}}\right) - (V_{gs} - \phi_{ms})\left(\frac{\varepsilon_{ox}t_{si}}{4\varepsilon_{si}t_{ox}}\right) \qquad (5)$$

The current conduction in Gate underlap DGMOSFET is diffusion dominated and the drain to source current is given by[6]

$$I_{ds} = \frac{2wq\mu_{eff}v_t n_i^2}{N_a L_e}\left(1 - e^{V_{ds}/v_t}\right)\int_0^{t_{si}/2} e^{\frac{\psi_{2\min}\left(x, t_{si}/2\right)}{v_t}} dy \qquad (6)$$

Where μ_{eff} is effective mobility, L_e=L_g+2*L_{un} is effective channel length and L_g is gate length, v_t=kT/q is thermal voltage, n_i is intrinsic carrier concentration and V_{ds} is drain to source potential.

3. RESULTS AND DISCUSSION

Fig1 (b) shows plot of drain current verses gate to source potential of Gate underlap DGMOSFET for varying of underlap length from 0 to 10nm in subthreshold regime. This shows the validation of our model with sentaurus simulation results. The current decreases as underlap length increases, since increase in the parasitic resistances.

Fig2 (a) shows the drain current verses gate length with varying L_{un}. As the gate length increases the drain current decreases due to increase in effective channel. The effect of drain current shows in same plot by both varying gate length and underlap length.

Fig2 (b) shows the drain current verses silicon body thickness with varying underlap length. If silicon body thickness increases then carrier concentration increases. Hence drain current increases with increasing silicon body thickness. This plot also shows the variation of drain current with both changing of silicon body thickness and underlap length.

4. CONCLUSIONS

The current model of Gate underlap DGMOSFET validated with the simulation by using sentaurus tool. We have investigated the variation of drain current with variation of thickness of silicon body, gate length and underlap length (non overlap gate length).When underlap length increases, effective channel length increases that increase the parasitic resistance , hence conduction of current decreases. Since the length is in Nano scale, current conduction takes place with very low value which may useful for switching circuit.

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6. REFERENCES

[1] Kranti, T., M. Chung, and J.-P. Raskin, "Analysis of static and dynamic performance of short channel double gate SOI MOSFETs for improved cut-off frequency," Jpn. J. Appl. Phys. , vol. 44, no. 4B, 2005, pp. 2340-2346.

[2] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S.P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies,"Proc. IEEE, vol. 89, Mar. 2001, pp. 259–288.

[3] J. G. Fossum, M. M. Chowdhury, V. P. Trivedi, T. J. King, Y. K. Choi, J. An, and B. Yu, "Physical insights on design and modeling of nanoscale FinFETs," inIEDM Tech. Dig. , 2003, pp. 29.1.1–29.1.4.

[4] V. Trivedi, J. G. Fossum, and M. M. Chowdhury, "Nanoscale FinFETs with gate-source/drain underlap," IEEE Trans. Electron Devices, vol. 52, no. 1, Jan. 2005, pp. 56–62.V.

[5] H. Soeleman, K. Roy, and B. C. Paul, "Robust sub-threshold logic for ultra-low power operation,"IEEE Trans. Very Large Scale Integr. (VLSI) Syst. , vol. 9, no. 1,Feb. 2001, pp. 90–99.

[6] R. Vaddi, R. P. Agarwal, and S. Dasgupta, "Analytical modeling of subthreshold current and subthreshold swing of an underlap DGMOSFET with tied–independent gate and symmetric–asymmetric options," *Microelectronics Journal*, vol. 42, no. 5, May 2011, pp. 798-807.

[7] Kranti and G. A. Armstrong, "High Tolerance to Gate Misalignment in Low Voltage Gate-Underlap Double Gate MOSFETs," vol. 29, no. 5, 2008, pp. 503-505.

[8] Bansal, S. Member, and K. Roy, "Analytical Subthreshold Potential Distribution Model for Gate Underlap Double-Gate MOS Transistors," vol. 54, no. 7, 2007, pp. 1793-1798.