Two New CMOS Schmitt Trigger Circuits based on Current Sink and Pseudo Logic Structures

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ABSTRACT
At the outset, a couple of new CMOS Schmitt triggers are introduced using Current Sink and Pseudo Logic structures and their characteristics are evaluated both analytically and numerically. The hysteresis curves of the proposed Schmitt triggers are also presented. The Schmitt triggers enlisted are most sought after for low-voltage and high-speed applications. The performances of the proposed new Schmitt triggers are examined using PSPICE and the model parameters of a 0.18 µm CMOS process. Current Sink and Pseudo Logic structures are suitable for VLSI implementation. Simulation results are presented.

Keywords
CMOS, Schmitt Trigger, pulse squaring, hysteresis, current sink, pseudo.

1. INTRODUCTION
Schmitt trigger circuits are widely used in many analog and digital circuits. It is a well known fact that CMOS Schmitt triggers are circuits possessing a property of converting a varying voltage into a stable logical signal (one or zero) [1]. They have been extensively used to reduce the sensitivity to noises and disturbances. Some of their applications include square/triangular, saw tooth waveform generation, amplitude modulation, frequency modulation, pulse width modulation, Voltage Controlled Oscillators (VCOs) and in instrumentation applications as well [2].

The main difference between Schmitt triggers and comparators is attributed to DC transfer characteristics while comparator exhibits only one switching threshold, where as Schmitt trigger presents different switching thresholds for positive-going and negative-going input signals. This characteristic is otherwise called hysteresis [1].

In recent years, several approaches have been put forth for the study and implementation of the Schmitt trigger. The conventional Schmitt trigger circuit was implemented using four MOS transistors, three of enhancement type and one of depletion type [3]. This circuit can be activated by using conventional CMOS technology, with the addition of one ion-implantation step to make the depletion device. Static power consumption could exist with this circuit. Schmitt trigger circuits which were presented in [4], also use four MOS transistors; three of them are of the same type, p or n, and one of the opposite type, n or p. However, all transistors are of enhancement type, and can be organized by using conventional CMOS technology. The noise immunity of the CMOS Schmitt trigger [4] is very high, typically greater than 50% of the supply voltage. A Schmitt trigger circuit with standard CMOS logic structures along with positive feedback is reported [5]. This circuit is coupled with two CMOS logic structures and an extra feedback transistor, which always guarantees the hysteresis of the circuit and offers higher switching speed compared to the conventional Schmitt triggers, but this speed is limited by the slew rate of the internal node of the circuit. A novel CMOS Schmitt trigger with regulated hysteresis [6] uses three transistor pairs and a control voltage in the regenerative feedback networks. This circuit demands an extra transistor pair unlike conventional circuits and ends up with more power consumption.

In this paper, we have proposed two new Schmitt trigger circuits based on current sink and pseudo logic structures for operating at 2 *V* and implemented in CMOS technology. The current sink logic structure is a common gate configuration using an n-channel transistor with gate connected to a fixed bias supply. This structure achieves higher gain than active load inverters. The pseudo structure employs ratioed logic such that the pull down transistors are about four times as strong as the pull up. The remaining sections of the paper are structured as follows. The proposed circuits and their description are presented in section II. Measured results and layouts are included in section III. Finally, a conclusion is inducted in section IV.

2. PROPOSED CIRCUITS AND DESCRIPTION

2.1 CMOS current sink logic structures based Schmitt trigger

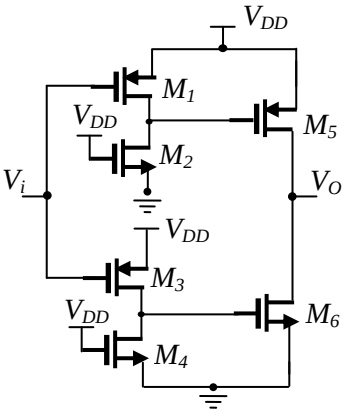

Fig. 1 Current Sink logic structures based Schmitt trigger

The proposed Schmitt trigger circuit based on current sink logic structures and its input/output waveforms are depicted in Fig 1 and 2, respectively.

Figure 1 illustrates Schmitt trigger circuit based on current sink logic structures. The circuit consists of two CMOS current sink logic structures (M_1-M_2 and M_3-M_4) and two output transistors (M_5-M_6). When the input waveform voltage $V_i \geq V_{tn}$ (=0.7 V), transistors M_1, M_3 are off and transistors M_2, M_4 are on. As a result, transistor M_5 is on and transistor M_6 is off and the output voltage goes high. This point is called UTP. When $V_i \leq V_{tn}$ (=0.7 V), transistors M_1, M_2, M_3 and M_4 are on. As a result, transistor M_5 is off and transistor M_6 is on and the output voltage goes low. This point is called LTP. The cycle repeats and generates square waveform as shown in the fig.2

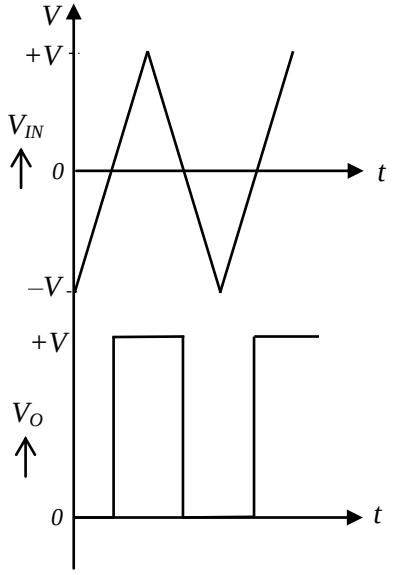

Fig. 2 Input/output waveforms of the proposed trigger circuits

2.2 CMOS pseudo logic structures based Schmitt trigger

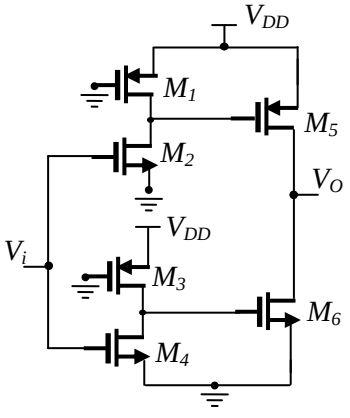

Fig. 3 Pseudo logic structures based Schmitt trigger

Figure 3 illustrates Schmitt trigger circuit based on pseudo logic structures. The circuit consists of two CMOS pseudo logic structure (M_1-M_2 and M_3-M_4) and two output transistors (M_5-M_6). When the input waveform voltage $V_i \geq V_{tn}$ (=0.7 V), transistors M_1, M_2, M_3 and M_4 are on. As a result, transistor M_5 is on and transistor M_6 is off and the output voltage goes high. This point is called UTP. When $V_i \leq V_{tn}$ (=0.7 V), transistors M_1, M_3 are on and transistors M_2, M_4 are off. As a result, transistor M_5 is off and transistor M_6 is on and the output voltage goes low. This point is called LTP. The cycle repeats and generates square waveform as shown in the fig. 2.

3. SIMULATION RESULTS AND LAYOUTS

The proposed circuits are designed and analyzed using Cadence gpdk 180 nm CMOS technology. The current sink logic structures based Schmitt trigger circuit shown in figure. 1 is simulated and its input and output results are shown in Fig. 4.

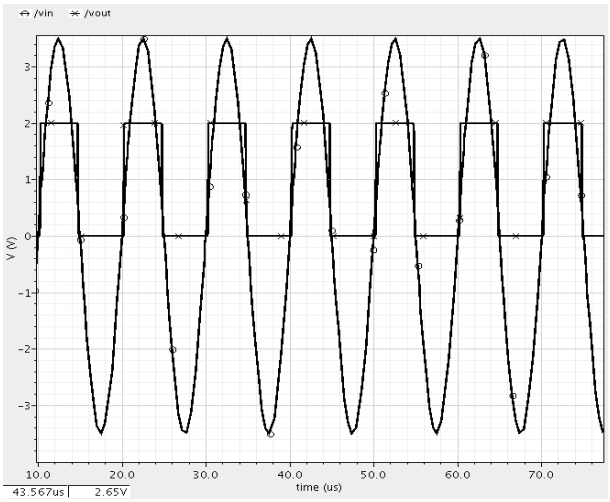

Fig. 4 Input/Output waveforms of the proposed circuit of Fig.1

The circuit in Fig. 1 was tested for temperature stability ranging from –150°C to +150°C and the simulation profile produced to be less than 0.056% variation in the case of square waveform. Figure 5 presents the temperature sensitivity of the proposed configuration of Fig. 1.

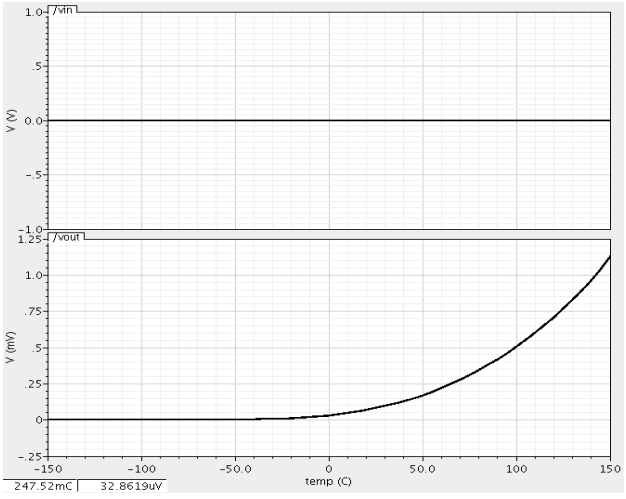

Fig. 5 Temperature sensitivity characteristics of Fig.1 (above: input sine wave and below: output square wave)

Simulated propagation delay is 4.347 µs. The transfer curve of the circuit in Fig. 1 is shown in Fig. 6.

The Schmitt trigger circuit shown in Fig. 3 is simulated and its input and output results are shown in Fig 7.

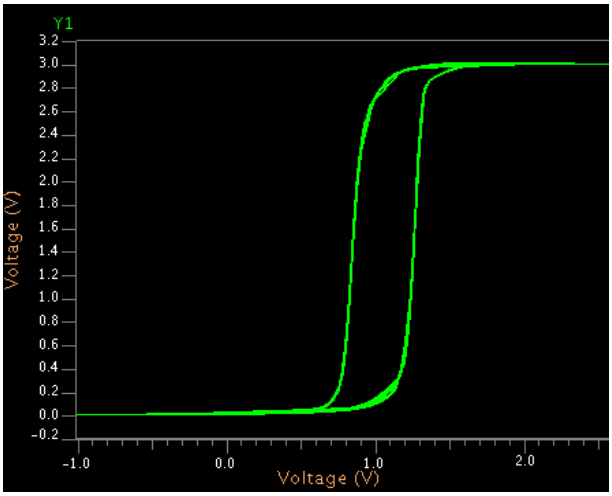

Fig. 6 Hysteresis curve of current sink logic structures based Schmitt trigger

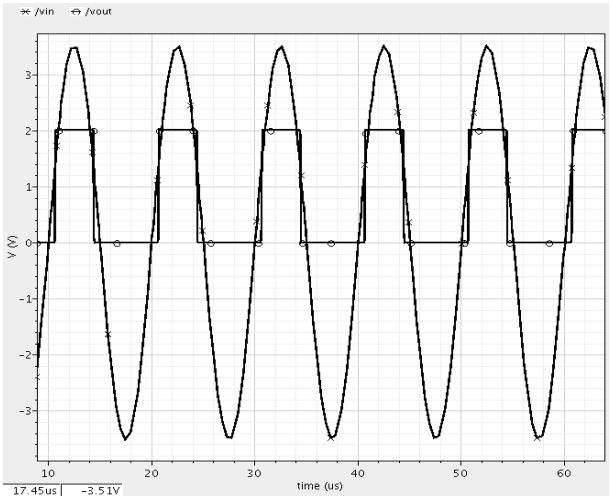

Fig. 7 Input/Output waveforms of the proposed circuit of Fig. 3

The circuit in Fig. 3 was tested for temperature stability ranging from –150°C to +150°C and the simulation profile produced to be less than 0.0004% variation in the case of square waveform. Figure 8 presents the temperature sensitivity of the proposed configuration of Fig. 3. Simulated propagation delay is 3.983 µs. The transfer curve of the circuit in Fig. 3 is shown in Fig. 9. Figures 6 and 9 are plotted using TSMC 180 nm CMOS technology with +3 V supply voltage.

The Schmitt trigger layouts are laid out with optimized sizing and spacing in compliance to the design rules of gpdk-180 nm CMOS process. The layout of the current sink logic structures based Schmitt trigger circuit is shown in Fig. 10 and the overall area occupied by it is 82.78 µm^2. The layout of the pseudo logic structures based Schmitt trigger circuit is shown in Fig. 11 and the overall area occupied by it is 84.88 µm^2.

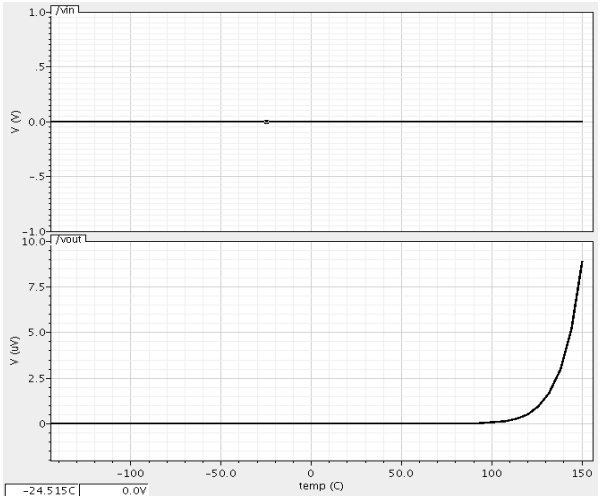

Fig. 8 Temperature sensitivity characteristics of the proposed circuit of Fig.3 (above: input sine wave and below: output square wave)

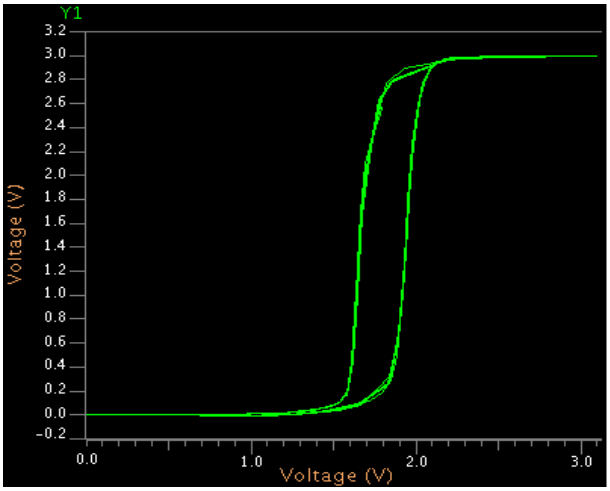

Fig. 9 Hysteresis curve of pseudo logic structures based Schmitt trigger

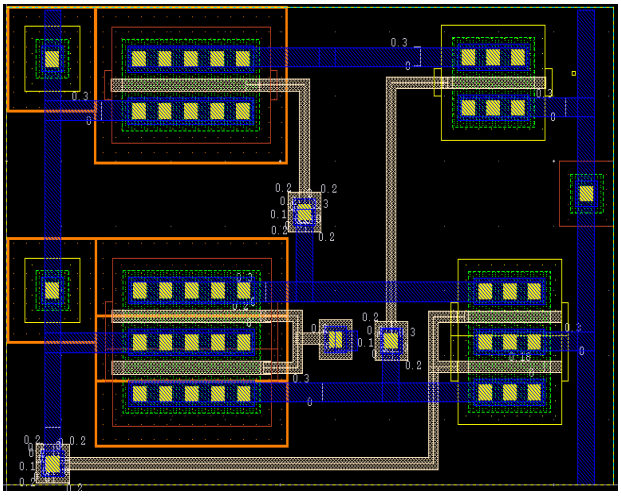

Fig. 10 Layout of current sink logic structures based Schmitt trigger

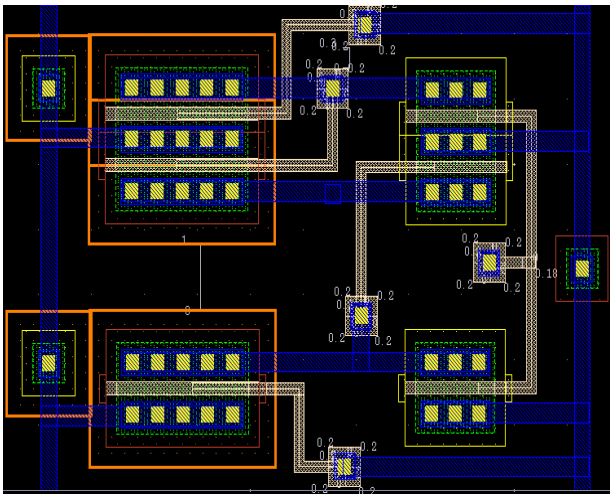

Fig. 11 Layout of pseudo logic structures based Schmitt trigger

The MOS level device dimensions used for simulation are included in Table-1.

Table 1. Aspect ratios

S.No	Schmitt Triggers	P-MOS (W/L) µm	N-MOS (W/L) µm
1.	Current sink logic structure	2.5/0.2	0.4/0.18
2.	Pseudo logic structure	2.5/0.2	1.5/0.18

4. CONCLUSION

Two new CMOS current-mode Schmitt triggers based on current sink and pseudo logic structures have been proposed in this paper. Based on the simulation results, the pseudo inverter based Schmitt trigger structure significantly outperforms the conventional Schmitt trigger on the propagation delay. The advantage of the current sink inverter based Schmitt trigger circuit is that even on the application of low voltage peaks; it was able to provide normal outputs because of the ability of the current sink inverter to achieve higher voltage gain than active load logic structures. The operation of the Schmitt trigger circuits has been examined using the simulation results.

5. REFERENCES

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