FPGA Realization of Transformer Impulse Fault Classification Scheme based on DWT and LVQ Neural Network

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ABSTRACT
Impulse test is a routine test for transformers and is performed to assess their winding insulation strength. If any fault occur during impulse test, the winding current contain typical signature depending on the nature and type of the faults. Among the various impulse faults the series fault or shunt fault that may occur in the winding needs special attention since it results in heavy damage. This work is dedicated to detection and classification of such faults based on a simulation study conducted on the lumped parameter model of a specially designed 6.6kV voltage transformer winding. The neutral currents have been recorded with series fault/shunt fault introduced in the ten sections of the winding model simulated using circuit simulation package. These current records are discrete wavelet transformed using the db5 analysis filter bank. The statistical features extracted from the third level approximation are considered for discriminating the defined faults and are classified by training a Learning Vector Quantization (LVQ) network. The clustering of the extracted discrimination features is done using possibilistic fuzzy c means (PFCM) algorithm to obtain voronoi/initial weight vectors required for training the LVQ network. The impulse fault classification achieved with this scheme is satisfactory with 95% accuracy. This scheme is developed using MATLAB. The hardware realization of this scheme is carried out using Xilinx System generator for DSP in Xilinx SPARTAN6 FPGA.

Keywords
Transformer, Impulse faults, DWT, PFCM, LVQ Neural network, FPGA.

1. INTRODUCTION
Transformer is vital equipment in a power industry and hence requires great care from various stages such as design, testing, installation and operation. Recent record suggests, about 70% to 80% of transformer failure are due to insulation failure of the transformer. One of the tests carried out on a transformer after assembly is the lightning impulse test which is a routine test for the assessment of the integrity of its winding insulation strength to surge over voltages and is performed as indicated in standards such as IEC 60076 Part IV [1]. Earlier methods for fault diagnosis during impulse test have been related to observation of oscilloscopic recording of the neutral currents at reduced and full voltage level [2]. This procedure requires significant human expertise and knowledge for proper judgment of insulation condition. The transfer function method exists as an improved assessment technique that involves frequency domain approach [3]. Applications of short time Fourier transform (STFT) and wavelet transform (WT) has already been demonstrated for impulse fault detection [4]. The wavelet transform is an efficient and powerful tool to extract the discriminating time and frequency features from neutral current records of transformers subjected to impulse test [5-10] with good resolution in both time and frequency whereas the Fourier transform could provide only frequency domain information. Recently wavelet has been widely used in various fault detection schemes along with fuzzy systems [11-13], and artificial neural network (ANN) [14-15].

Recent developments in FPGA technology have made them suitable for developing a prototype for hardware realization of the fault classification scheme. A review of the state of the art FPGA technology, design/development tools including system level programming is available in [16]. A method of hardware realization of DWT analyzers has been shown for fault classification [17-20]. FPGA prototyping of classification schemes has also been presented [21-22]. The above mentioned research ideas motivated us to develop a hardware realization scheme for impulse fault detection and classification of the presence of series/shunt faults in any section of the winding of a transformer. In this work the hardware realization of the developed scheme is implemented in Xilinx SPARTAN 6 FPGA using Xilinx system generator for DSP.

2. PROBLEM FORMULATION
The lumped parameter model of a specially designed 6.6kV voltage transformer winding that is considered as the device under test (DUT) is subjected to simulation study. Circuit simulation is carried out using pspice orcad software to obtain the neutral current records under no fault and different series/shunt fault conditions. The objective is to implement a feature extraction strategy for fault discrimination based on DWT analysis filter bank using MATLAB/SIMULINK DSP system toolbox. The mean and variance of the third level approximation are considered as the fault discrimination features. To cluster these features using PFCM clustering algorithm and then to define various fault groups (Table 1). A fault classification task is to be implemented using LVQ neural network that needs to be trained with these cluster centers as initial/voronoi weights. The hardware realization of this impulse fault classification scheme, comprising of the DWT analysis filter bank, the statistical feature extraction logic and the trained LVQ neural network has to be achieved using Xilinx system generator for DSP.

Table 1: List of acronyms representing various fault groups

Acronyms	Faults
NF	No-fault
SEFG1	Series fault in sections 1,2 &10
SEFG2	Series fault in sections 3 and 9
SEFG3	Series fault in sections 4,5,6,7 & 8
SHFG1	Shunt fault at line-end sections (1-3)
SHFG2	Shunt fault at mid-winding sections (4-6)
SHFG3	Shunt fault at neutral-end sections (7-9)

3. SIMULATION OF IMPULSE FAULTS

The simulation work is carried out with the lumped parameter model of the DUT as shown in Figure 1. The entire length of the winding is divided into ten sections. The model parameters namely self inductances (L1 to L10), series capacitances (Cs1 to Cs10), shunt capacitances (Cg1 to Cg10) and also the mutual inductances between sections are determined through calculation using formulae [23] based on the geometry of the winding. The series resistances (R1 to R10) are determined through measurement. The circuit simulation of the lumped parameter model with parameter values determined as above is carried out using Pspice orcad. A low voltage impulse similar to standard lightning impulse (LI) of 1.2/50μs and 1V amplitude as shown in Figure 2 is applied to one end of the winding and current through the other end under no fault and various simulated fault conditions is recorded for the analysis. A series fault is simulated by placing a short across a section and a shunt fault is simulated by placing a short across a section end and ground.

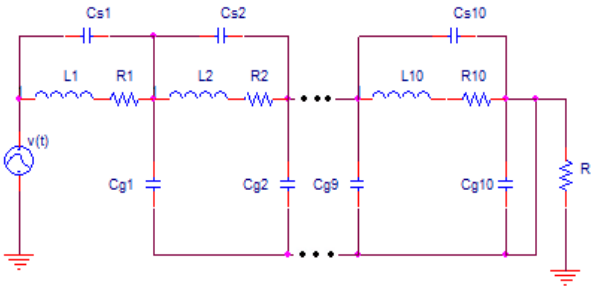

Figure 1: Lumped parameter model of the DUT

The winding currents are computed with the sampling time of 0.1μs for a total time of 1ms. The time domain records under no fault, series fault in section 1 and shunt fault in section 5 and their frequency domain plots are shown in Figure 3 and Figure 4 respectively.

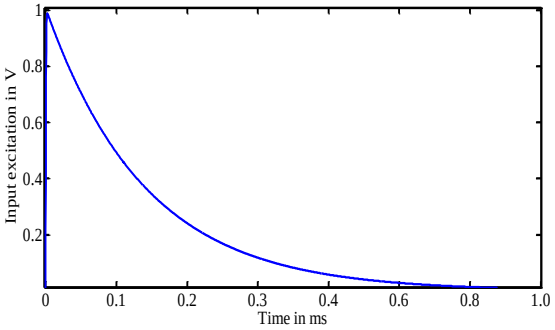

Figure 2: Input L1 excitation

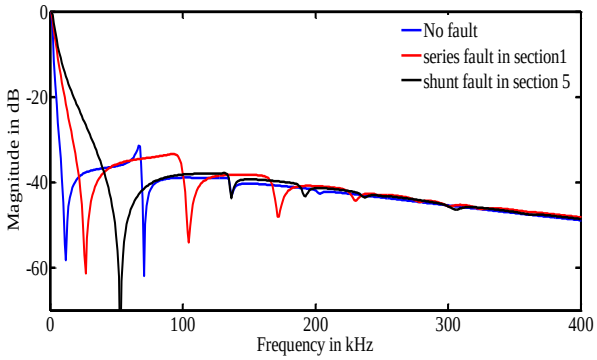

Figure 3: Winding current in time domain under no fault and with series/shunt faults

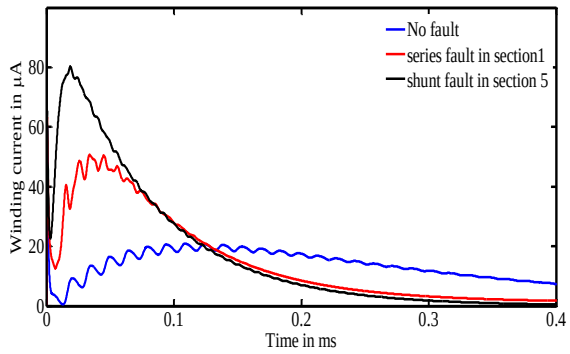

Figure 4: Winding current in frequency domain under no fault and with series/shunt faults

4. DWT FOR IMPULSE FAULT DETECTION

A non stationary signal is well represented in time scale domain using wavelet transform. It applies a basic filtering process the signal in order to obtain the low frequency and high-frequency components. A single level DWT implementation is shown in Figure 5. The first level decomposition produces approximation coefficients cA1, and detail coefficients cD1. These vectors are obtained by convolving *S* with the low-pass filter for approximation, and with that of the high-pass filter for detail. In the case of multi-level DWT, the next step splits the approximation coefficients cA1 in two parts using the same scheme, replacing *S* by cA1 producing cA2 and cD2, and so on.

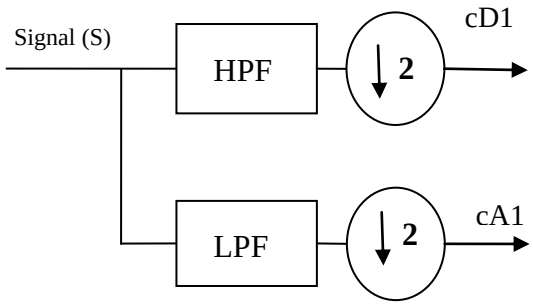

Figure 5: single step DWT

As daubechies wavelet function is widely used for the identification of impulse faults, daubechies *'db5'* is chosen in this work. The direct-form FIR filter has been used to implement the DWT decomposition filtering process. The coefficients of the low pass and high pass filters for the db5 wavelet are shown in Table 2. The number of levels of decomposition is selected based on the nature of the signal, or on the basis of a suitable criterion.

Table 2: Coefficients of db5 wavelet decomposition filters

Lo_D	Hi_D
0.003	-0.1601
-0.0126	0.6038
-0.0062	-0.7243
0.0776	0.1348
-0.0322	0.2423
-0.2423	-0.0322
0.1384	-0.0776
0.7243	-0.0062
0.6038	0.0126
0.1601	0.0033

The sampling frequency of the winding currents computed through simulation is 10MHz. The frequency domain analysis of the winding currents show that the dominant resonant frequencies of the DUT lie within 300 kHz. The DWT analysis filter bank with three levels of decomposition is constructed using MATLAB/DSP system toolbox. Here the discrimination features are extracted based on the third level approximation coefficients. The detail coefficients of the signal at level 1, 2, 3 and the approximation coefficients of the signal at level 3 under no-fault and few defined faults conditions are shown in Figure 7, 8, and 9 respectively.

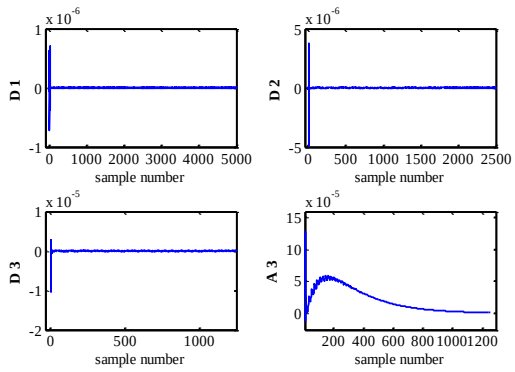

Figure 7: Detail and approximation coefficients of winding current under no fault condition

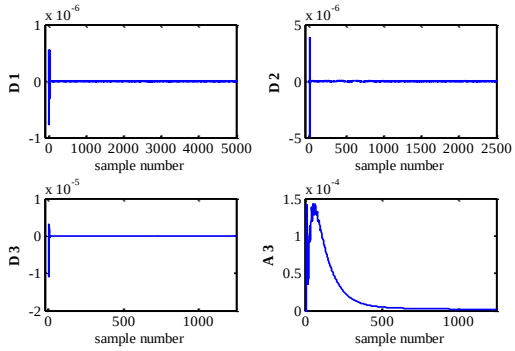

Figure 8: Detail and approximation coefficients of winding current with series fault at section 1

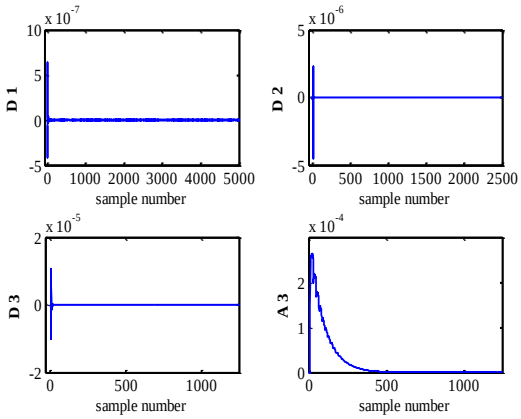

Figure 9: Detail and approximation coefficients of winding current with shunt fault at section 5

The statistical features namely mean and variance are extracted for the no fault and the various fault conditions and are given in Table 3. These features have clear discrimination among the no fault and the various defined faults. This encouraged us to design and implement an automated impulse fault detection and classification scheme based on FPGA.

Table 3: Statistical features extracted for no fault and different fault cases

Fault	Mean(*e^{-5})	Variance(*e^{-9})
Nf	2.047	2.934
sf1	1.904	1.139
sf2	1.903	1.211
sf3	1.902	1.277
sf4	1.900	1.327
sf5	1.900	1.351
sf6	1.900	1.348
sf7	1.900	1.360
sf8	1.902	1.32
sf9	1.904	1.275
sf10	1.907	1.219
shf1	2.088	2.525
shf2	2.077	2.468
shf3	2.066	2.837
shf4	2.052	2.285
shf5	2.034	2.160
shf6	2.012	2.015
shf7	1.984	1.841
shf8	1.947	1.608
shf9	1.907	1.219

5. IMPLEMENTATION OF DWT FOR FEATURE EXTRACTION

The designed DWT analysis filter bank is implemented in Xilinx system generator for DSP as shown in Figure 10. The logic required for computing the statistical features namely mean and variance from the third level approximation of the winding current is shown in Figure 11. The coefficients of the analysis filters based on the db5 wavelet are chosen as indicated in Table 2 while implementing the feature extraction strategy.

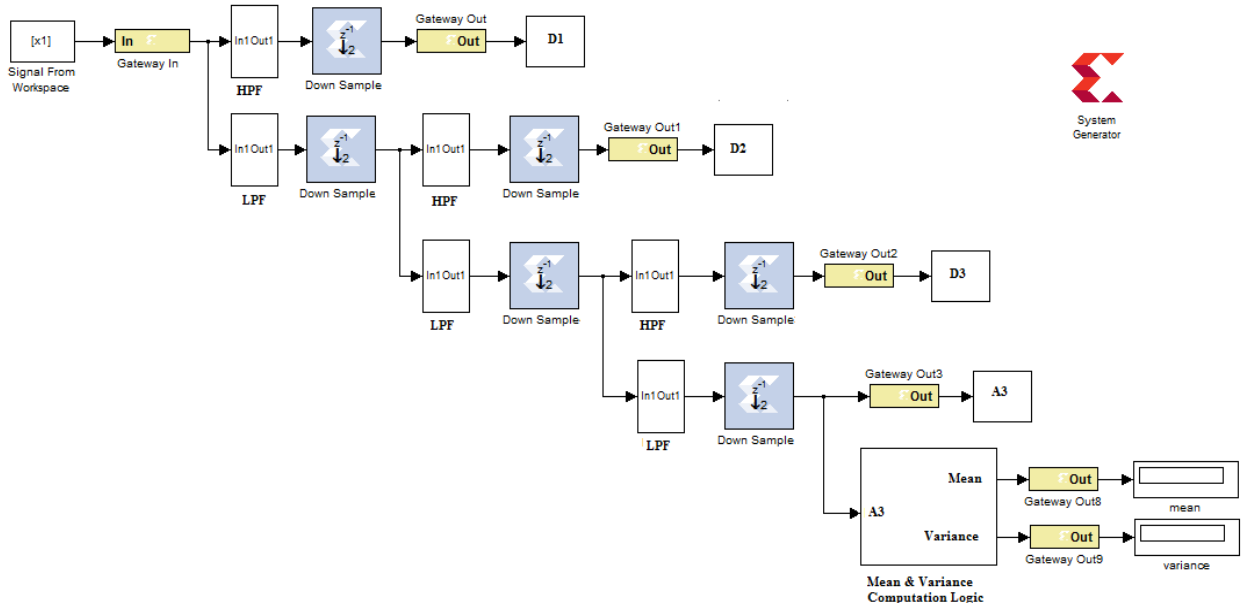

Figure 10: DWT based feature extraction scheme implementation using Xilinx system generator for DSP

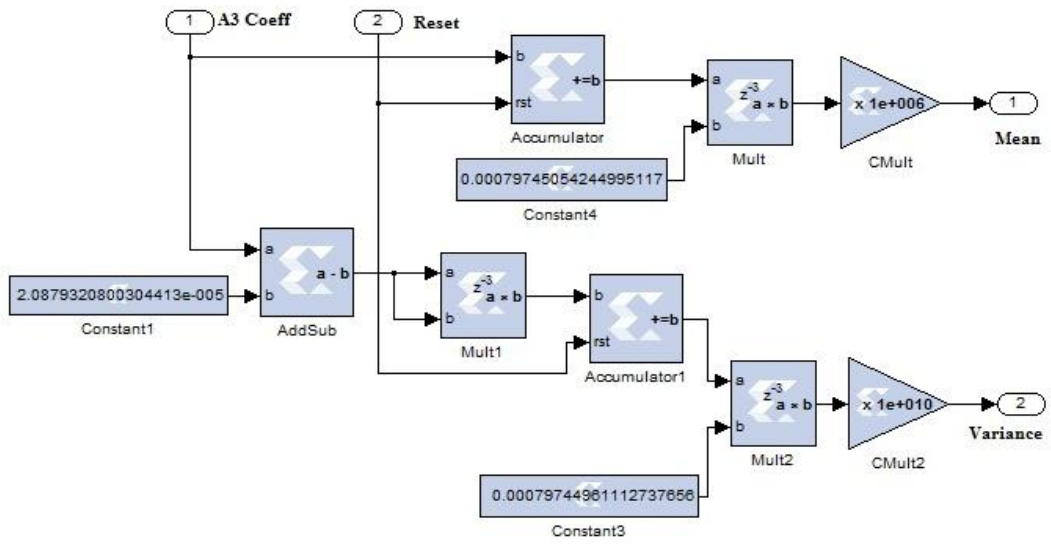

Figure 11: Mean and variance computation subsystem

6. LVQ NEURAL NETWORK FOR FAULT CLASSIFICATION

LVQ networks can be applied to multi-class classification problems. Recently training algorithms for LVQ network have been developed which adapt a parameterized distance measure as this becomes a key issue. LVQ network comprises of a competitive layer followed by a linear layer as shown in Figure 12. Let $\{w_j\}_{j=1}^{l}$ denote the set of voronoi vectors, and let $\{x_i\}_{i=1}^{N}$ denote the set of input vectors. The LVQ algorithm proceeds as follows [24]:

1. If the voronoi vector w_c is closest to the input vector x_i and both of them associated with the same class label, then voronoi vector w_c is adjusted as, $w_c(n+1) = w_c(n) + \alpha_n[x_i - w_c(n)]$ where $0 < \alpha_n < 1$.
2. On the other hand voronoi vector w_c is adjusted as, $w_c(n+1) = w_c(n) - \alpha_n[x_i - w_c(n)]$
3. The other Voronoi vectors are not modified.

where α_n is the learning rate that decreases with the number of iterations/epochs of training.

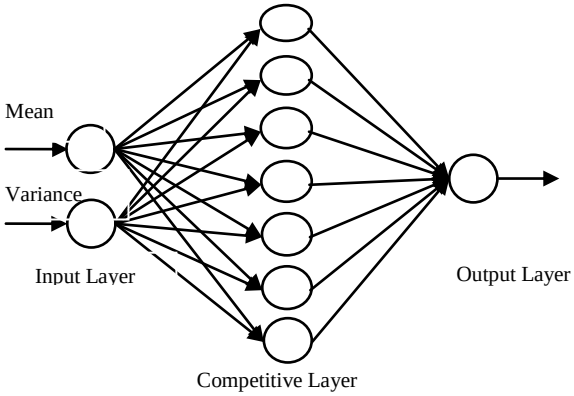

Figure 12: LVQ neural network architecture for fault classification

The statistical discrimination features extracted from third level approximation coefficients of the winding currents recorded under no fault and the 19 different fault conditions as given in Table 3 are used to train and test the neural network. To train the LVQ network the initial weights/voronoi vectors are required. The extracted features are clustered into seven groups using PFCM clustering algorithm whose centers are considered as initial weights/voronoi vectors. Out of the 20 data set 13 of them falling under seven different fault classes are considered for training the LVQ network and the remaining data are used as test data. The LVQ network is implemented using MATLAB code. The impulse fault classification results are satisfactory with 95% accuracy.

7. FPGA REALIZATION OF THE FAULT CLASSIFICATION SCHEME

The simulink model for implementing the trained LVQ neural network is developed using xilinx system generator blockset as shown in Figure 13. The input to the LVQ neural network is fed from the ROMs that stores the extracted features. The competitive layer is implemented with adders and multiplier blocks to compute the Euclidean distance. The MINIMUM IDENTIFIER block computes the minimum out of the seven computed Euclidean distance values. The subsystem following this block is the fault class identifier block which

determines the class to which the input data belongs to. The inputs and the response of the simulink model of LVQ network obtained in the scopes during simulation are shown in Figure 14 (a) and (b) respectively. Later the inputs to the LVQ network are fed from the already constructed feature extraction scheme comprising of DWT analysis filter bank, mean and variance computation block. The entire model shown in Figure 15 is thus simulated and the possibility of hardware realization is verified.

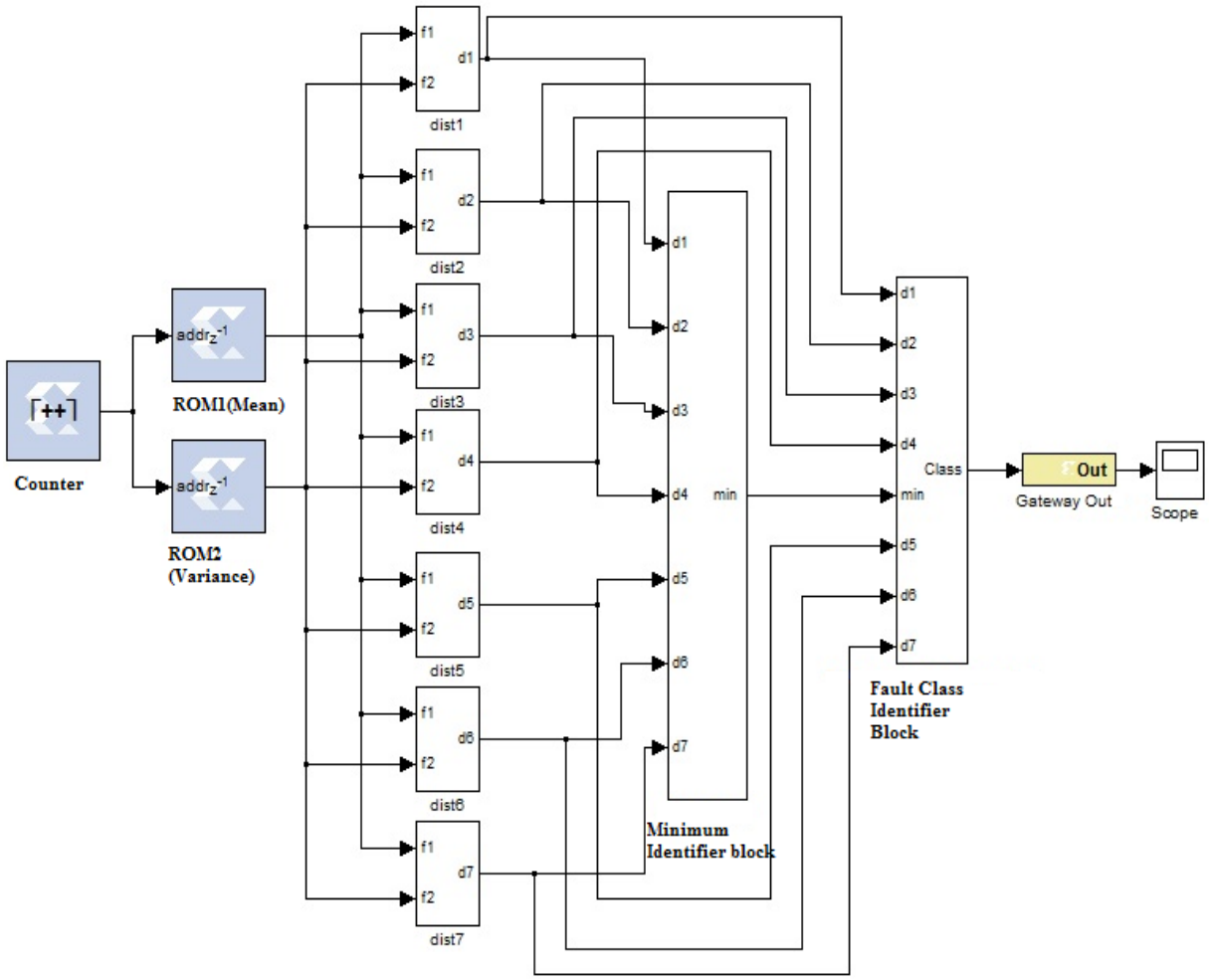

Figure 13: LVQ neural network implemented using Xilinx system generator toolbox

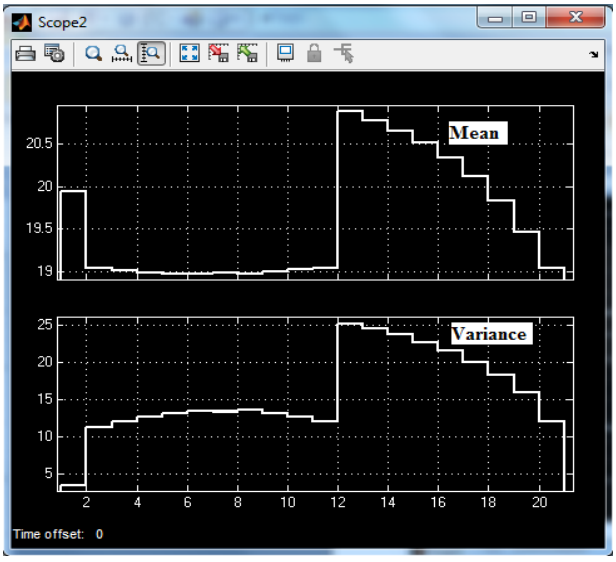

Figure 14 (a): Scope waveforms of inputs during simulation (Mean and Variance)

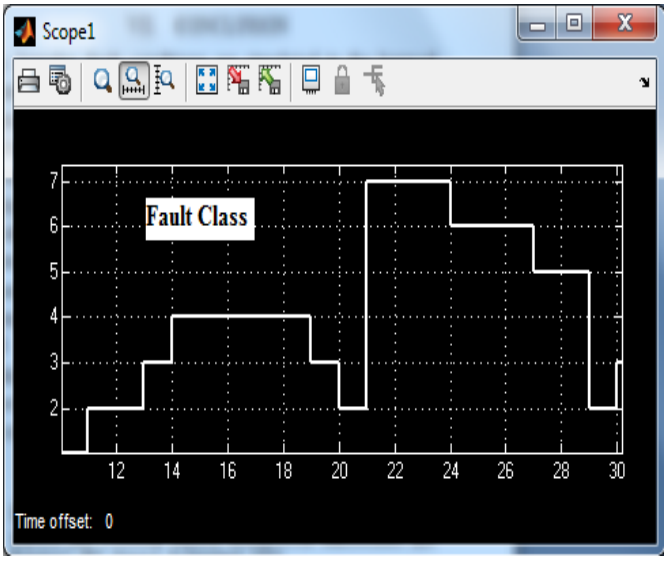

Figure 14 (b): Scope waveforms of output during simulation (Fault Class)

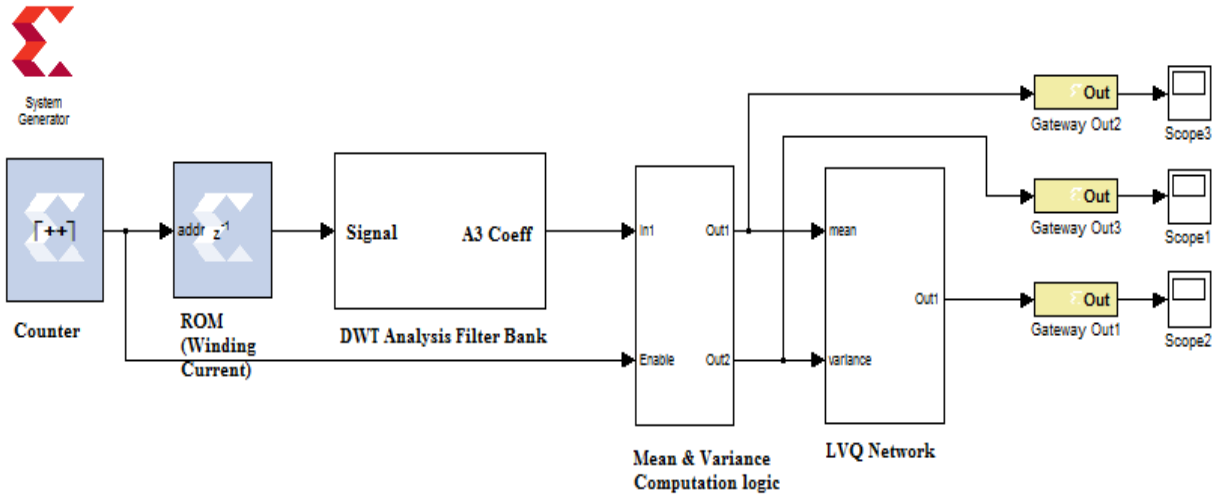

Figure 15: Fault classification scheme implemented using Xilinx system generator toolbox

The general purpose SPARTAN6 FPGA kit that has XC6SLX25-3FTG256 IC and developed by Xilinx Inc. is employed for implementation. The device utilization summary is given in Table 4.

Table 4. Device utilization summary for the implemented impulse fault classification scheme

Logic utilization	Used	Available	Utilized
Slices	1,610	184,304	1%
LUTs	3,088	92,150	3%
Registers	1,610	184,304	1%
DSP48A1S	137	180	76%
Bonded IOBs	132	540	24%
Flip-flops	1,609	23,038	6.98%
Clock period	18.718ns		
Max frequency	53.425MHZ		

8. CONCLUSION

The impulse fault conditions are simulated in the lumped parameter model of the DUT using pspice orcad. The winding neutral currents which are non stationary in nature are analyzed using the DWT analysis filter bank. The statistical features extracted from the third level approximation that contains the frequency range of interest has promising level of discrimination among the defined faults. The PFCM is a good clustering algorithm to perform classification tasks as it gives more importance to typicality. The designed LVQ network has performed well with 95% classification accuracy. The hardware realization can be extended to carry out on-line impulse fault detection and classification by incorporating the logic required for training of the LVQ network.

9. REFERENCES

[1] IEC 60076 – Part IV. (2002). Power transformers. Guide to the lightning impulse and switching impulse testing-Power transformers and Reactors. IEC. Geneva. Switzerland.

[2] Chakravorti, S., Dey, D.,and Chatterjee, B. (2013).Recent Trends in the Condition Monitoring of Transformers. Power Systems. Springer_Verlag. London.

[3] Malewski, R., and Poulin,B. (1988). Impulse testing of power transformer using the transfer function method. IEEE Transactions on Power Delivery. Vol. 3. 476-489.

[4] Satish,L. (1998). Short time Fourier and Wavelet transform for fault detection in power transformers during impulse tests. IEEE proc.sci.meas.technol. vol.145.NO.2. 77-84.

[5] Purkait,P., Chakravorti,S. (2002). Time and frequency domain analyses based expert system for impulse fault diagnosis in transformers. IEEE Transaction on dielectric and electrical insulation. vol.9. no.3. 433-443.

[6] Santhi,S., Jayashankar,V., Jagadeesh Kumar, V. (2008). Time frequency analysis method for the detection of winding deformation in transformers during short citcuit test. Instrumentation and Measurement Technology Conference proceedings. Victoria. Vancouver Island. Canada.May(12-15).

[7] Rao,M.R,.singh,B.P. (2001). Detection and localization of interturn fault in the HV winding of a power transformer using wavelets. IEEE transactions on dielectrics and electrical insulation, Vol 8. 652-657.

[8] Purkait,P., Chakrovorti,S. (2002). Pattern classification of Impulse faults in transformer by wavelet analysis. IEEE Trans. On Dielectrics and Electrical Insulation.vol.9. No.4.

[9] Mujtahid Ansari,M., Patil Bhushan Prataprao., Dr.Beg,M. A. (2013) Application of Signal Analysis for Fault Diagnosis in Transformer by Discrete Wavelet Transform. International Journal of Engineering Research & Technology (IJERT). Vol. 2 Issue 2.

[10] Prema Kumar, N., Amarnath, J., Shrivastava,K. D., Singh,B.P. (2005). Identification of Winding Faults in Power Transformers by Low Voltage Impulse Test and

Neutral Current Method using Wavelet Transform Approach. IEEE Trans. On Electrical Insulation and Dielectric Phenomena.

[11] Omar A.S.Youssef. (2004). Applications of fuzzy-logic wavelet-based techniques for transformers Inrush currents identification and ique for power system faults classfication.IEEE Conf. on Power systems and exposition. vol. 1. pp 553-55.

[12] Vanamadevi N, Santhi S. (2013). Impulse Fault Detection and Classification in power transformers with wavelet and fuzzy based technique. Springer -Recent advancements in System Modeling applications - Lecture Notes in Electrical Engineering. Vol 188. pp. 261-273.

[13] Hossam A. Nabwey, E. A. Rady, A.M. Kozae, A. N. Ebady., Fault Diagnosis of Power Transformer Based on Fuzzy Logic, Rough Set theory and Inclusion Degree Theory.The Online Journal on Power and Energy Engineering (OJPEE).Vol. 1. No.2.

[14] Vanamadevi.N,Arivamudhan.M,Santhi.S. (2008). Detection and Classification of Impulse Faults in transformer using Wavelet Transform and Artificial Neural Network. Proceedings of IEEE. ICSET 2008. Nov 24-27.

[15] Paraskar,SR.,Beg,M.A.,.Dhole,G.M. (2011). Discrimination between Inrush and Fault in Transformer: ANN Approach. International Journal of Advancements in Technology. Vol 2, No 2.

[16] Eric Monmasson and Marcian.N.Cirstea. (2007). FPGA design methodology for industrial control systems-A review. IEEE transactions on industrial electronics, vol.54. No.4.

[17] Mohammed Bahoura and Hassan Ezzaidi. (2010). Real-Time Implementation of Discrete Wavelet Transform on FPGA. ICSP Proceedings. 191-194.

[18] Cabal-Yepez, E., and Osornio-Rios,R.A. (2009). FPGA-based Online Induction Motor Multiple-fault Detection with Fused FFT and Wavelet Analysis. International conference on Reconfigurable computing and FPGAs.101-106.

[19] Bahoura, M., and Ezzaidi,H. (2009). FPGA-implementation of a sequential adaptive noise canceller using Xilinx System Generator International Conference on Microelectronic. pp.213-216.

[20] Gavrincea Ciprian., Tisan Alin., Doiga Stefan., Buchman Attila., FPGA- based discrete Wavelet transform design using MatLab/Simulink. International Symposium for Design and Technology of Electronic Packages, 13th Edition. Baiamare. Romania.

[21] Mohamed boubaker.,Khaled ben khalifa.,Bernard girau.,Mohamed dogui and Mohamed hedi bedoui., (2008). On-line arithmetic based reprogrammable hardware implementation of LVQ neural network for alertness classification. IJCSNS International Journal of computer science and network security. vol.8 No.3.

[22] Simi P.Valsan and Shanti Swarup, K. (2009). High speed fault classification in power lines:Theory and FPGA based implementation. IEEE Transactions on industrial electronics. vol.56.No.5.

[23] Grover Fredrick W. (1946) Inductance calculations-working formulas and tables. Dover Publications Inc. New York

[24] Simon Haykin. (2006). Neural Networks. A comprehensive foundation. Second Edition. Pretice – Hall. India.