90Nm – CMOS based Low-Power 256/257 Dual Modulus Percale

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ABSTRACT
CMOS refers to both a particular style of digital circuitry design, and the family of processes used to implement that circuitry on integrated circuits (chips).CMOS circuitry in VLSI dissipates less power and is denser than other implementations having the same functionality. As this advantages has grown and become more important,CMOS processes and variants for VLSI have come to dominate, so that vast majority of modern integrated circuit manufacturing in on VLSI technology processes.. In today's wireless communication systems, requires objectives like maximum frequency with low power consumption, small size and low fabrication cost. A key circuit use in modern communication is Dual Modulus Prescaler.The layout of DMP which is develop by us is a modified design of high performance DMP.This is optimum design for use in industries at 90nm VLSI technology.This report is a brief study of high performance DMP on 90nm VLSI technology to achieve objectives as mentioned above.

A divide-by 256/257 dual-modulus prescaler have been fabricated in a 90-nm CMOS process. The synchronous divide-by-4/5 divider uses source coupled logic (SCL) D flip-flops with a resistive load to achieve the 17.2-GHz maximum operating frequency.
The prescaler requires 4.3 mA current from a 1.5-V supply.This circuit has the highest operating frequency and the lowest power consumption reported to date among CMOS dual-modulus prescalers that can operate at 10 GHz or higher. The prescaler also works up to 15.8 GHz with a 1.2-Vsupply and draws 3-mA current.

Keywords
VLSI Technology, 90nm, Microwind3.1, CMOS, Dual-Modulus Prescaler, source coupled logic, merged NAND function, Scaling, high performance.

1. INTRODUCTION
The field of complementary metal-oxide semiconductor (CMOS) integrated circuits has reached a level of maturity where it is now mainstream technology for higher integration density, low power consumption, high speed capability and low fabrication cost. These circuits are developed to pursue a high-speed prescaler.
A dual-modulus prescaler is one of the most critical building blocks in frequency synthesizers. The maximum operating frequency of prescaler sets the synthesizer maximum operating Frequency. Because of these, the design of low-power high-frequency divide-by N/N+ 1 dual modulus prescaler is critical and challenging.
To date, the highest operating frequencies of prescalers implemented in GaAs and SiGe bipolar technologies have reached 27 GHz [1] and 36GHz [2]. Compared with these, the prescalers fabricated in CMOS processes usually operate at lower frequencies. The highest reported operating frequency for CMOS prescalers is 15GHz[3],[4]. The circuit has been fabricated in a 130-nm technology and consumes relatively high power (115mW). Extra feedback networks were used in [5] to increase the operating frequency to 14GHz in a 0.18-um CMOS process. A phase-shifting prescaler switches among signals with varying phases to achieve two or more divide ratios. The highest operating frequency for phase shifting prescalers [6] is 13 GHz and consumes 41mW of power.
This paper presents a low-voltage low-power 17-GHz 256/257 dual-modulus prescaler. The circuit has been fabricated in a 90-nm CMOS process. The prescaler draws 4.3 mA current from a 1.5-V supply. This is the highest frequency and consumes the lowest power among the reported CMOS dual modulus prescalers operating at frequencies higher than 10 GHz.

2 . CIRCUIT DESIGN
The dual-modulus prescaler consists of a synchronous divide-by-4/5 circuit and an asynchronous divide-by64 as shown in Fig. 1. The total divide ratio is 256 and *257* when the modulus control, MC is set to low and high, respectively.

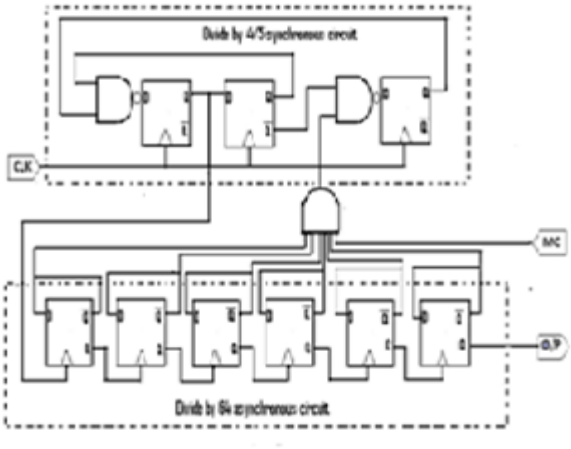

Fig 1: 256 / 257 prescaler block diagram.

A. Synchronous Counter

In this prescaler, the synchronous divide-by-4/5 circuit is the most critical part because it operates at the highest frequency. The divide-by-4/5 circuit consists of three differential D-flip-flops and 2 NAND gates to implement the modulus selection. The first two flip-flops are connected as a divide-by-4 circuit while the third flip-flop adds an extra clock period delay for the divide-by-5 operation. Both the flip-flops and NAND gates are in the critical path. The longest RC delay associated with the path limits the prescaler maximum operating frequency. To reduce the propagation delay, the NAND gate and flip flop are merged together. To better balance the delays, the output of first flip-flop is chosen to drive the asynchronous divider.

Fig. 2 shows the schematic. of Source Coupled Logic (SCL) D flip-flop used in the divider-by-4/5 circuit. The transistor size and load resistance determine the maximum operation frequency. The differential input pair transistors switch output nodes. They add capacitive loads to the flip flops which drive them. The sizes of these transistors are set to be 1/5 of those for the CLK / CLKB transistors to increase operating frequency. The CLK / CLKB transistors are 1.2-um wide. The size of cross-coupled transistors is set to be 1/6

of the CLK transistor size, that is scaling. A 3-kΩ polysilicon

resistor without a silicide layer is used as the load. Not having a silicide layer increases the sheet resistance. This reduces the size and parasitic capacitance of resistors, which is critical for high frequency operation. Lowering the load resistance increases the switching speed and the power consumption. This at the same time decreases the voltage swing and can ultimately cause the asynchronous divider to fail.

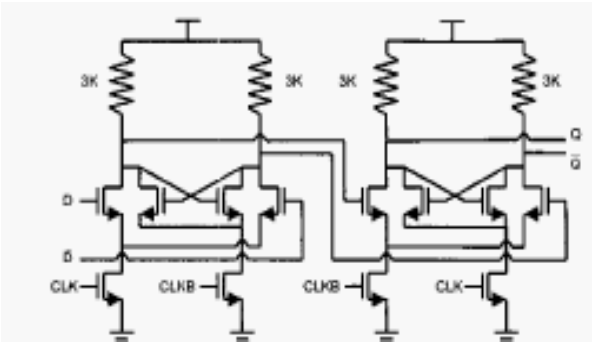

Fig 2: A Schematic of D flip-flop using source-coupled-logic (SCL) circuits.

Key differences between the prescaler reported in this Work and previously reported 15-GHz CMOS prescaler are the uses of 3-kΩ load resistors instead of 100Ω resistors and smaller transistors. As will be discussed, these lead to greater than 7X reduction of power consumption.

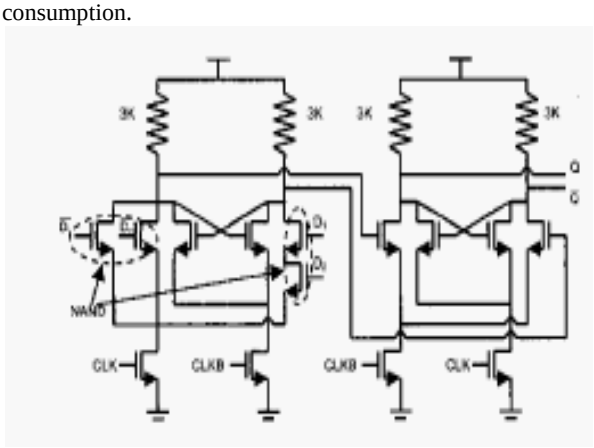

Fig. 3: A D flip-flop with merged NAND function.

The schematic of a D flip flop with a merged NAND gate is shown in Fig.3. The first latch contains four NMOS transistors to incorporate the NAND logic. This merging of NAND function increases the switching speed and reduces the power consumption.

In all the D flip-flops, the current sources between the sources of CLK/CLKB transistors and ground in the conventional SCL designs are omitted for low-voltage operation. A potential concern for this is the increased current spikes in the supply line. Fig. 4 shows the simulated transient supply current of synchronous divide by- 4/5 circuit with and without the current sources.Removing the current sources increases the current spikes but the changes are small.

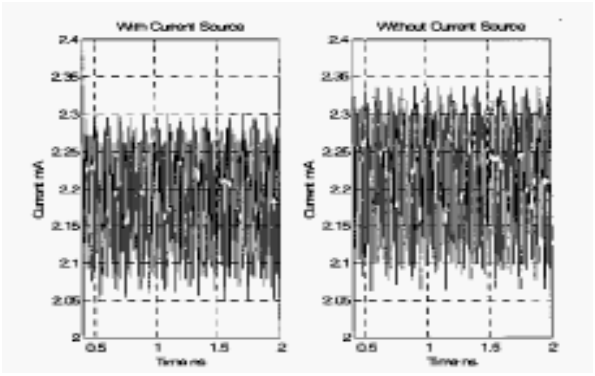

Fig 4: Simulated Supply Current of Divide by 4/5 circuit with and without current source transistors.

B. Asynchronous Counter

The asynchronous divide-by64 circuit is a 6-stage cascaded chain of divide-by-2 circuits as shown in Fig 1. Fig. 5 shows the schematic of a flip-flop. The gates of PMOS load transistors are grounded to increase the maximum operating frequency by operating the load transistor in linear region [7]. The connection between the synchronous divide-by-4/5 circuit and first stage of the asynchronous divider is through only one pair of CLK/CLKB transistors while the other pair of transistors below the cross-coupled pairs is connected to Vdd as shown in Fig. 5 [8]. This reduces the load capacitance added to the synchronous divider and increases the maximum operation frequency. The synchronous and asynchronous dividers are connected directly without using any buffers.

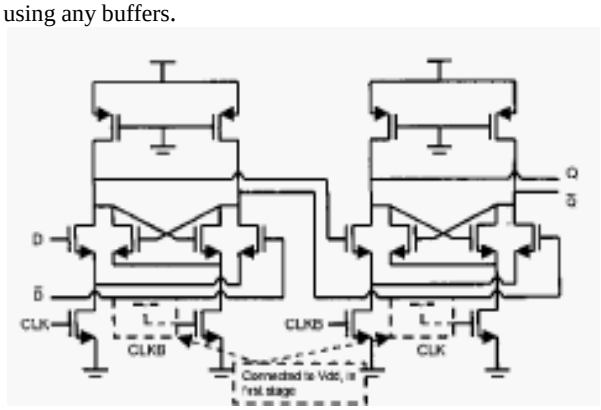

Fig 5: A D flip-flop in the asynchronous divide-by-64 circuit.Dashed lines show two clock transistors connected to Vdd in the first divide-by-2 stage.

3. Circuit IMPLEMENTATION AND MEASUREMENT RESULTS

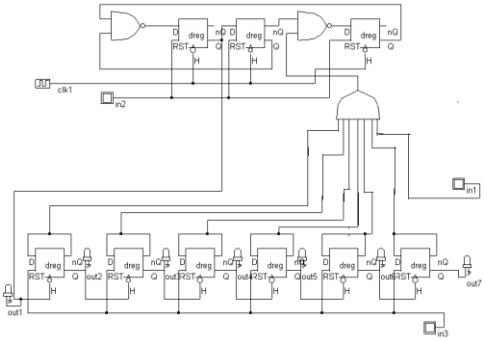

Fig 6 : Schematic Diagram of DMP in DSCH.

After obtaining logic diagram we have used DSCH software to verify functionality of logic diagram. DSCH is circuit level design tool. DSCH program is logic editor and simulator. DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started.

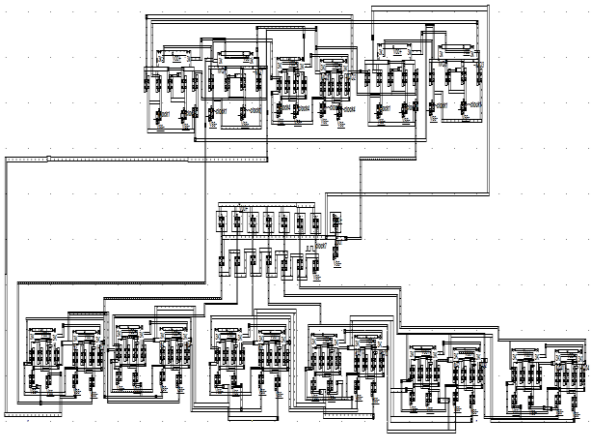

Fig 7: Layout of DMP in Microwind 3.1

This layout generated,requires less area compared to layout generated from DSCH also it is easy to understand.The Software microwind 3.1 is layout level design tool, used in paper allows us to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. It also includes all the commands for a mask editor as well as original tools never gathered before in a single module such as 2D and 3D process view, Verilog compiler, tutorial on MOS devices. You can gain or access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

Chip Size = 22.600um × 64.950um.

Area of single PMOS transistor = 1.32um^2

Area of single NMOS transistor = 0.54um^2

Total W/L ratio of layout = 0.500 ÷ 0.100

=128×5 = 640

Total area of layout = 1.32×08+0.54×120

= 75.36um^2.

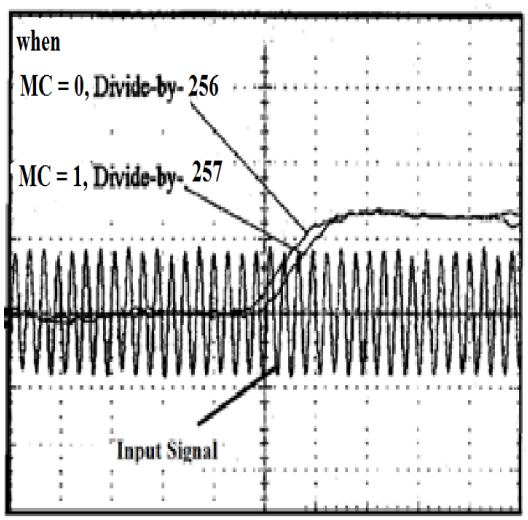

Fig 8: Measured waveforms of Dual Modulus Prescaler divide by 256 and 257.

Fig 8 shows the input waveform at 17.2GHz and the output waveform of this prescaler for 1.5v supply. The total divide ratio is 256 and *257* when the modulus control, MC is set to low and high, respectively. Table-1 Summarizes the performance of the Dual Modulus Prescaler as per the changing supply voltage. Table-2 Shows our test work.

Table 1.Summary of prescaler performance

Supply Voltage	1.5v	1.2v
Current	4.3mA	3.2mA
Power Consumption	6.45mW	3.84mW
Maximum input frequency	17.2GHz	15.8GHz
Chip Size	0.48mm X 0.53mm	0.48mm X 0.53mm
Technology	90-nm CMOS	90-nm CMOS

Table 2. Comparison with former works

Supply Voltage	1.5v
Current	4.3mA
Power Consumption	6.988mW
Maximum input frequency	17.2GHz
Chip Size	22.600um x 64.950um
Technology	90-nm CMOS
Simulation Time	499.58ns

4. CONCLUSION

This paper reported low- voltage low-power 17GHz 256/257 Dual –Modulus Prescaler implemented in a 90-nm CMOS-process. The prescaler requires only 4.3mA from a 1.5v supply. This circuit has the highest
Operating frequency and lowest power consumption among the CMOS-dual modulus prescaler which can operate at frequencies higher than 10GHz.
This paper highlights the design of Dual Modulus Prescaler. It is useful for, power optimization, reducing the propagation delay. It also describes several aspects of Dual Modulus Prescaler & CMOS circuit design, using Microwind 3.1 version tool.

5. ACKNOWLEDGMENTS

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6. REFERENCES

[l] S. Wada, T. Maeda, M. Tokushima, J. Yamazaki and M.lshikawa and M. Fujji, "A 27 /GHz /151 mW GaAs *256/258* dual-modulus prescaler IC with 0.1 um double-deck-shaped (DDS) gate E/D-HJFETs." *Dig. Papers* (GaAs *IC) Symp.*,Nov. 1998.

[2] H. Knap, M. Wurzer, T. F. Meister, .J. Bock and K. Aufinger, *"36* GHz dual-modulus prescaler in SiGe bipolar technology." *Dig. Papers 2002 IEEE RFIC Symp.*, June *2002*, pp. 239-242.

[3] H.-D. Wohtmuth, and D. Kehrer, "A 15 GHz *256/257* dual modulus prescaler in 120 nm CMOS." *European Solid- State Circuits Conference*, Sep. 2003, pp. 77 - 80.

[4] H.-D. Wohlmuth, and D. Kehrer, "A 17 GHz dual-Modulus prescaler in 120 nm CMOS." *Dig.Papers 2003 IEEE RFIC Symp.*, June 2003, pp. 479-482.

[5] D.-J. Yang, and K. K. *0*, "A 14-GHz *25612.57* Dual-Modulus Prescaler With Secondary Feedback and Its Application to a Monolithic CMOS 10.4-GHz Phase-Locked Loop." *IEEE* Trans. *Microwave Theory Tech.*, Feb.2004,PP.461-468

[6] M. Tiebout, C. Sandner, H.-D. Wohlmuth, N. D. Dalt, E. Thaller, "A Fully Integrated 13GHz AZ Fractional-N PLL in 0.13pm CMOS." *Dig. Papers 2004* ISSCC *Symp.*, Feb.2004PP.386-387

[7] C.-M. Hung, B. A. Floyd, and K. K. 0, "A fully integrated 5.35-GHz CMOS VCO and a prescaler." *Dig. Papers* 2000 *IEEE RFIC Symp.*, May *2000*, pp. 69-72.

[8I H. Wang, "A 1.8 V 3 mW 16.8GHz frequency divider in *0.25* pm CMOS." *Dig. Papers 2000 ISSCC Symp.*, Feb.2000,pp. 196-1 97.

[9] " Advanced CMOS Cell Design " by Estinne Sicard, Soni Delmas Bendhia.

[10] "Microwind User Manual"

[11] WWW.Microwind.org