# Implementation of Digital down Converter in **Communication System**

Snehal R. Gaikwad G.H.Raisoni College of Engineering, Nagpur

# ABSTRACT

This paper presents performance of NCO used in Digital Down Converter. Digital Down converter consists of NCO and CIC filter as key components; here the output of the CIC filter is the down sampled version of the input signal. As the sampling frequency at the initial stage is high to reduce the sampling frequency for the further processing, CIC filter is used. The NCO is an implementation of a direct digital frequency synthesizer (DDS) which produces a signal at the output with a specified frequency and phase (adjustable at run time).

# 1. INTRODUCTION

A fundamental part of many communications systems is Digital Down Conversion (DDC). A Digital down Converter is basically complex mixer, shifting the frequency band of interest Α. to baseband. The DDC is typically used to convert an RF signal down to baseband. It does this by digitizing at a high sample rate, and then using purely digital techniques to perform the data reduction.

Being digital gives many advantages, including:

Digital stability - not affected by temperature or manufacturing processes. With a DDC, if the system operates at all, it works perfectly - there's never any tuning or component tolerance to worry about.

Controllability - all aspects of the DDC are controlled  $\triangleright$ from software. The local oscillator can change frequency very rapidly indeed - in many cases a frequency change can take place on the next sample. Additionally, that frequency hop can be large – there is no settling time for the oscillator.

Size - A single ADC can feed many DDCs, a boon for multi-carrier applications. A single DDC can be

implemented in part of an FPGA device, so multiple channels can be implemented - or additional circuitry could also be added.

# 2. Major Components of Digital Down Converter

#### 2.1.1. Numerically Controlled Oscillator

A numerically controlled oscillator (NCO) synthesizes a discrete-time, discrete-valued representation of a sinusoidal waveform. It is an established method of generated periodic sinusoid signals whenever high frequency resolution, fast changes in frequency and phase, and high spectral purity of

the output signal is required. A major advantage of the NCO is that its output frequency, phase and amplitude can be precisely and rapidly manipulated under digital processor control. Other NCO attributes include the ability to tune with extremely fine frequency and phase resolution, and to rapidly hop between frequencies [5]. A direct digital synthesizer operates by storing the points of a waveform in digital format, and then recalling them to generate the waveform. The rate at which the

P.P.Rane G.H.Raisoni College of Engineering, Nagpur

synthesizer completes one waveform then determines the frequency [5], [6].



#### 1.1.1.1. Phase Accumulator

The phase accumulator shown consists of a j-bit frequency register which stores a digital phase increment value p followed by a j – bit full adder and a phase register. The phase increment value is entered into the frequency register. The operation of the phase accumulator can be considered by looking at the phase advances around a circle as shown in Fig.1. As the phase advances around the circle this corresponds to advances in the waveform, i.e. the greater the number corresponding to the phase, the greater the point is along the waveform [6]. By successively advancing the number corresponding to the phase it is possible to move further along the waveform cycle.

### 1.1.1.2. Phase to Amplitude Converter

Once the phase has been determined, it is necessary to convert this into a digital representation of the waveform. This is accomplished using a phase to waveform converter. This is a memory that stores a number corresponding to the voltage required for each value of phase on the waveform. The memory is either a read only memory (ROM) or programmable read only memory (PROM). This contains a vast number of points on the waveform. A very large number of points are required so that the phase accumulator can increment by a certain number of points to set the required frequency [5].

#### 2.1.2. CIC Filter

Cascaded integrator-comb, also called Hogenauer filters, are multi-rate filters that are used for realizing large sample rate conversions in digital systems. The main advantage of this filter is it does not use multipliers, and consists of only adders, subtractors and registers [2]. They are typically employed in applications that have a large excess sample rate. That is the system sample rate is much larger than the bandwidth occupied by the signal.

Characteristics of CIC Filters [3]

- Linear phase response;
- Utilize only delay and sum block (no multiplication);

• The integrator and comb structure are independent of rate changes (there is no need to reproject the filter on decimation/interpolation rate change).



### Fig. 2 CIC Structure

#### 2.1.2.1. Comb

A comb filter running at a low sampling rate fs/R, for a rate change of R is an odd symmetric filter described by

Y[n] = x[n] - x [n-RM](1) In the equation, M is a design parameter and is known as differential delay. M is usually limited to 1 or 2. The corresponding transfer function at fs is

Hc (z) =1-z-RM (2) The comb sections are combined with a rate changer. Using a technique for Multirate analysis of LTI systems the comb sections can be pushed through the rate changer and then become Y[n]=x[n]-x[n-M] (3)

By this three things are achieved:

1. Half of the filter has been slowed down and therefore efficiency is increased.

2. The numbers of delay elements required in the comb section have been reduced.

3. The integrator and comb stages are independent of rate changer.



Fig.3 Basic Comb structure

#### 2.1.2.2. Integrator

An integrator is a single pole IIR filter with a unity feedback coefficient given by

$$\begin{split} Y[n] =& y [n-1] + x[n] \quad (4) \\ \text{The transfer function for an integrator on the z-plane is} \\ \text{HI}(z) =& 1/(1-z-1) \quad (5) \end{split}$$

The basic structure of an integrator is as shown in figure 4.



Fig. 4 Basic Integrator Structure

2. RESULTS

Sampling Frequency: 60 MHz

#### Table 1: Parameters used for NCO module:

Parameter	Parameter Name	Data	Value
		Туре	
Frequency	FTW_WIDTH	integer	24
Tuning Word			
Phase Tuning	PHASE_WIDTH	integer	12
Word	_	-	
Output	AMPL_WIDTH	integer	16
Amplitude		_	
Word			

Table 2: VHDL simulation results are shown below:

Frequenc	FTW	FTW	Frequency	Actual
у		Actual	Generated	Frequency
Required				from
_				Simulation
750 KHz	25.6	26	762KHz	762KHz
1 MHz	34.133	34	996KHz	990.5KHz
2 MHz	68.266	68	1.99MHz	1.99MHz
5 MHz	170.66	171	5.00MHz	5.00MHz
10 MHz	341.33	341	9.99MHz	9.97MHz



Fig. 5

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Fig. 7





## 3. CONCLUSION

This paper deals with the progressive development of a Digital Down Converter for Communication system equipment. The DDC demodulates the ADC sampled data down from an IF signal to 0Hz. CIC filters often includes the re-samplers that interpolates or decimates the signal to achieve desired sample rate, depending upon the application decides.

# 4. FUTURE WORK

With a DDC, if the system operates at all, it will be an enabling technology for future multimode and reconfigurable satellite receivers.

# 5. REFERENCES

- Xilinx LogiCORE,"Digital Up Converter (DUC) v1.4", DS276 May 23, 2005 www.xilinx.com
- [2] Lattice Semiconductor Corporation, "The FPGA as a Flexible and Low-Cost Digital Solution for Wireless Base Stations", A Lattice Semiconductor White Paper, March 2007
- [3] Matthew P. Donadio, "CIC Filter Introduction", For Free Publication by Iowegian, m.p.donadio@ieee.org, 18 July 2000
- [4] Pavel KOVAR, "Generation of the Narrow Band
   Digital Modulated Signals Using Quadrature Digital Up
   Converter", RADIO ENGINEERING, VOL.12, NO. 1,
   APRIL 2003
- [5] Direct digital synthesis (DDS) http://www.radioelectronics. com/info/receivers/synth basics/dds.php
- [6] QAN19 Modulating Direct Digital Synthesizer in a quick logic

FPGAhttp://www.quicklogic.com/images/appnote19.pdf (Accessed on April 10, 2006)

- [7] Eva Murphy and Colm Slattery, "All about Direct Digital Synthesis", Analog dialogue 38-08, August 2004, http://www.analog.com/analogdailogue
- [8] Xilinx LogiCORE,"Multiply Accumulator v4.0", DS336 April 28, 2005 www.xilinx.com
- [9] Cyril Prasanna Raj P and Subash, "SASTech Journal", Vol 4. PP 33-39, September 2006
- [10] S. Signell, T. G. Kouyoumdjiev, K. H. Mossberg,
  "Design and Analysis of Bilinear Digital Ladder Filters", IEEE Trans. on Circuits and Systems, Vol. 43, No. 2., February 1996.
- [11] E. B. Hogenauer, "An economical class of digital filters for Decimation and interpolation *IEEE Trans. on Acoustics, Speech. And Signal Processing*, Vol. 29, pp. 155-162, April 1981.