Comparative Study of Different Low Power Designs of Braun Multiplier using Double Gate MOSFET at 45nm Technology

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ABSTRACT
As per the present scenario every device as well as circuits are to be implemented with low power techniques so as to withstand the power challenges. In an arithmetic circuit multiplier who has much significant role in association with addition and subtraction process is also to be designed with low power technique so as to reduce the overall power consumption by the circuit. In this paper a four bit Braun multiplier is designed with different low power techniques and the main component of it i.e. the full adder design is modified and implemented with double gate MOSFET and the second important component i.e. the AND gate is designed with three different low power techniques. All the designs are compared on the basis of power, delay and power delay product (PDP). The designs are implemented in Cadence Virtuoso Tool with 45nm technology for its validation.

General Terms
Double gate MOSFET, power, Power delay product, Low power.

Keywords
Braun multiplier, Double gate MOSFET, Sleepy keeper, Pass transistor logic

1. INTRODUCTION
In every arithmetic circuit addition and subtraction are the two important processes. But Multiplication has many significant roles in image processing, sound processing, DSP etc [1]. Multiplier is a parameter which concern with the speed of a processor. The power consumed by the multiplier is also directly influence the overall power consumption by the whole circuit. So it is necessary that the multiplier has been implemented with low power as well as high speed techniques [2] so as to reduce the overall power consumption by the circuit without affecting the processing speed. For implementing a multiplier two main circuits are full adder and AND gate. Previously the full adder was designed with 10T double gate MOSFETs [3]. The double gate MOSFET full adder design reduced the power consumption by the circuit appreciably as compare to the conventional full adder using CMOS transistors but still the static power as well as the dynamic power of double gate MOSFET full adder were too high. Hence a modified design of full adder using double gate MOSFET is proposed here. The second important parameter of multiplier i.e. the AND gate is also designed with low power techniques. Previously many low power and speed techniques were proposed such as pass transistor logic technique, sleep transistor approach, keeper technique etc. In this paper two new low power techniques for designing the AND gate are proposed. One is AND gate using double gate MOSFET and the other is AND gate using double gate MOSFET sleepy keeper technique. Then the four bit Braun multiplier is designed with the above mentioned power reduction techniques. The first design is implemented by taking double gate MOSFET full adder with pass transistor logic AND gate. The second design is implemented by taking double gate MOSFET full adder and AND gate using double gate MOSFET. The third design is implemented with double gate MOSFET full adder and AND gate using double gate MOSFET sleepy keeper technique. The power, delay and power delay product (PDP) generated by these above techniques are compared and tabulated. The above three designs of Braun multiplier are implemented in Cadence Virtuoso Tool in 45nm technology for its validation.

2. DOUBLE GATE MOSFET FULL ADDER DESIGN
Full adder is a basic building block of any arithmetic circuit. Its efficiency affects the total efficiency of the circuit. Hence it is necessary to design a low power full adder circuit in order to reduce the overall power consumption by the arithmetic circuit. Conventional CMOS full adder consumes much power in active mode of operation as well as in idle mode. So a new design of full adder was implemented using 10 numbers of double gate MOSFETs. The design was implemented with two XOR gates having four numbers of double gate MOSFETs and one double gate inverter [3]. But the design still had some power issue. So in this paper that design is little modified such that all the bodies of P-type double gate MOSFETs are connected to a voltage supply which is far less than the supply voltage value and all the bodies of N-type double gate MOSFETs are connected to another supply having voltage slightly greater than the ground potential. Here also the aspect ratio is considered as 3. The modified full adder design using double gate MOSFET is given in Figure 1In Figure 1, V1 and V2 are two different supply voltages. The value of V1 is very less than the supply voltage value and the value of V2 is slightly greater than the ground potential. Due to these two external voltage supplies the excess power consumption by the bodies are reduced

appreciably. The active power consumption in this structure of full adder is about 79% reduced than the previously designed full adder using double gate This design is mainly considered because it uses double gate MOSFETs which has better control over the channel. The area as well as power are reduced by a considerable value.

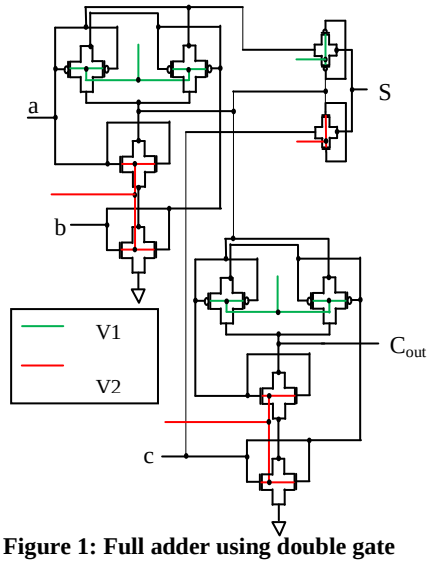


Figure 1: Full adder using double gate MOSFET

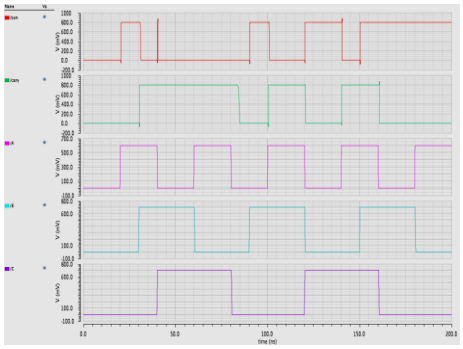


Figure 2: Output waveform of full adder

3. LOW POWER AND GATE DESIGNS

AND gate is the basic gate which multiply two bits of data. If A and B are two binary input bits then after passing through the AND gate the output will be $F = AB$. In the Braun multiplier the AND gate output is forwarded as one of the input to the full adder. Thus in order to reduce the overall power of the Braun multiplier the AND gate is required to be implemented by different low power MOSFETs[3].The output waveform of the modified full adder is shown in Figure 2.

techniques. In this paper three low power techniques are implemented in designing a AND gate. The first technique i.e. the pass transistor logic technique was previously proposed and a very popular technique for delay reduction. The second and the third techniques i.e. AND gate design using double gate MOSFET and AND gate design using double gate MOSFET sleepy keeper approach are proposed here. The details of these three low power and high speed techniques are briefly described in the following subsections.

3.1 AND gate design using pass transistor logic

The existing pass transistor logic is the best substitute of complementary MOSFET in terms of delay reduction, area reduction and improved speed. In pass transistor logic the primary inputs are allowed to drive not only the gate terminal but also the source/drain terminal of the MOSFET unlike the complementary MOSFET in which the primary inputs are only to drive the gate terminal [8]. So the number of transistors used are reduced hence reducing area as well as delay. The implemented AND gate design using pass transistor logic is given in Figure 3.

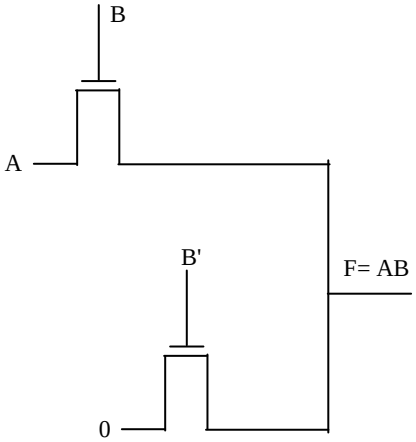


Figure 3: AND gate using pass transistor logic

In this paper the first design of Braun multiplier is implemented using this above pass transistor logic along with the double gate MOSFET full adder circuit in 45nm technology with a supply voltage of 0.8v.

3.2 Proposed design of AND gate using double gate MOSFET

Double gate MOSFET structure is emerging as the most prominent technology for low power circuit designs. The double-gate MOSFET has a channel of scaled width and to manage that channel, gates are provided to both the sides [4]. The two types of gates namely the Front gate and Back gate in this device can be independently driven for the purpose of reduction in power consumption and improve the performance of the device [5] Double gate MOSFET devices are otherwise known as scalable silicon transistors because of its tremendous control over the short-channel effects in the double-gate structure [6, 7]. The AND gate using double gate MOSFET is given in Figure 4.

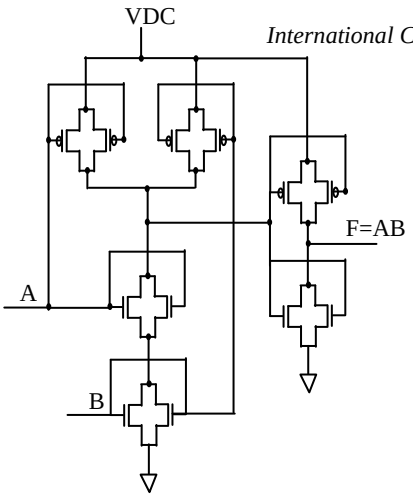


Figure 4: AND gate using double gate MOSFET

The above AND gate is implemented using the tied symmetric double gate MOSFET structure where both gates are connected with same supply voltage. The second design of Braun multiplier is implemented with this technique in association with double gate MOSFET full adder in 45nm technology and with supply voltage of 0.8V.

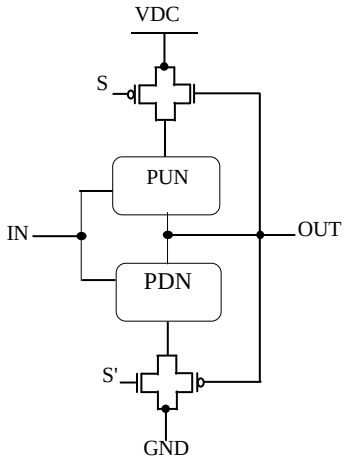


Figure 5: Sleepy keeper technique

As the PMOS is not proficient at passing ground as well as NMOS is also not so proficient at passing supply voltage. In order to maintain the 1 value (provided that 1value has already been recorded) this approach uses the NMOS transistor which hold the 1 value in sleep mode and is connected to the supply voltage. Hence in sleep mode of operation this NMOS transistor is the only source to the pull up network. Similarly to maintain the 0 value in sleep mode (provided that 0 value is previously recorded) this method uses the PMOS transistor to maintain this output 0 value and is connected in parallel to the NMOS sleeptransistor. The supply voltage can be reduced in order to maintain the logic state. In this paper the third design of Braun multiplier is implemented by using this sleepykeeper approach in combination with double gate MOSFET. The design is implemented in 45nm technology.

3.3 Proposed AND gate design using double gate MOSFET sleepy keeper technique

The sleepy keeper approach is a combination of two approaches, the sleep approach and the keeper approach [2].In sleep approach one sleep PMOS transistor is placed between supply voltage and pull up network and one sleep NMOS transistor is positioned between pull down network and ground. These additional sleep transistors cut the power in order to turned off the circuit. These sleep transistors are activated when the circuit is in operational mode and deactivated when the circuit is in idle mode. The only disadvantage of this method is that the output will be in floating value after sleep mode and the output states are destructive. In sleepy keeper approach [9] as shown in Figure 5 another NMOS keeper transistor is connected in parallel with the PMOS sleep transistor which is also connected between supply voltage and pull up network. And at the down part, an extra PMOS keeper transistor is connected in parallel to the NMOS sleep transistor which is also connected between pull down network and ground.

4. THE BRAUN MULTIPLIER

Multiplication is the process of adding a number (multiplicand) with itself for a number of times as provided by another number (multiplier) to produce the result i.e. product.. Braun multiplier is a simple parallel multiplier also known as carry save array multiplier [10]. The design of *N*-bit Braun multiplier consists of N^2 AND gates and $N * (N - 1)$ full adder blocks. Suppose **X** is a multiplicand of *N* bit and **Y** is a multiplier of *N* bit then the result of this multiplication is *2*N* which let be represented as $\boldsymbol{P_{0\text{-}7}}$. The multiplication process is given below.

Suppose $X = X1X2X3X4$

and $Y = Y1Y2Y3Y4$

then $X * Y = P = P7P6P5P4P3P2P1P0$

where *P7* is the MSB and *P0* is the LSB.In this Braun multiplier each product output is generated parallel with the AND gate. Each partial product (shown in Figure 7) is added with the sum of partial product which has earlier obtained by the row of adders.

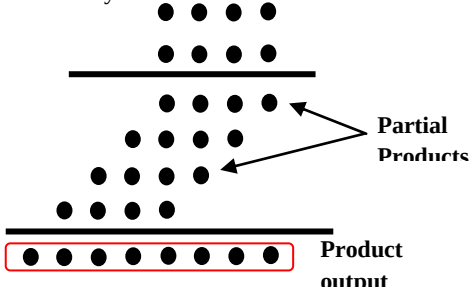


Figure 7: Multiplication process

The $\mathbf{C_{out}}$ is shifted a bit to the left or right and later added to **S** which is originated by the first adder and the recently generated partial product. The normal Braun multiplier is very effective with the operands of less than 16bit size in terms of the speed, power and area. In this paper that

Designs	Power (uW)	Delay (ns)	PDP (pWs)
Braun multiplier using pass transistor logic	14	20.09	0.281
Braun multiplier using Double gate MOSFET technique	8.617	30.16	0.259
Braun multiplier using Double gate MOSFET sleepy keeper technique	8.413	19.85	0.166

tabulated in the following section.

5. SIMULATION RESULTS AND DISCUSSIONS

In this paper the design of Braun multiplier is implemented using double gate MOSFET full adder blocks and different low power designed AND gate array as described in section 3. The simulation result of Braun multiplier is shown below in Figure 8.

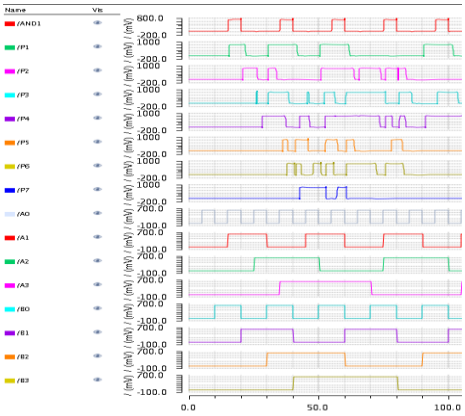


Figure 8: Braun multiplier output waveform

The concerned circuits are designed in Cadence Virtuoso Tool at 45nm technology with the supply voltage of 0.8V.

6. CONCLUSION

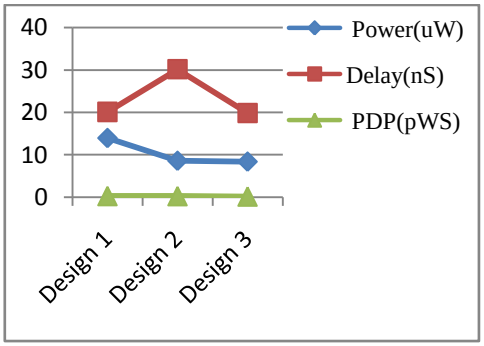
In this paper the Braun multiplier is designed with full adder using double gate MOSFET and three types of low power technique in order to reduce the power consumption, delay and power delay product. The results are tabulated and analysed for the three designs. The third design which is implemented with double gate MOSFET full adder and an array of AND gate using double gate MOSFET sleepy keeper technique shows an improved reduction in power dissipation, delay and power delay product. The three low power and high speed designs of Braun multiplier are implemented in Cadence virtuoso tool and in 45nm technology.

simple Braun multiplier is implemented using double gate MOSFET full adder blocks and three types of low power reduction techniques. And the results in terms of power, delay and power delay product (PDP) of these three designsarempare

The power, delay and the power delay product (PDP) are tabulated in Table 1.

Table 1. Average power dissipation, Delay and PDP results for different designs of Braun multipliers

From the Table 1 it is observed that the third design of Braun multiplier which is implemented with double gate MOSFET sleepy keeper technique gives better performance in term of reduced power, delay and power delay product (PDP) as compare to the first two designs which are implemented with pass transistor logic and simple double gate MOSFET techniques. The above table is also plotted and shown in Graph 1.



Graph 1. Comparison graph of the three above designs in terms of power, delay and PDP

7. ACKNOWLEDGMENTS

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